Latest Gated Mode Tests at HLL
Phase 2 Module W37_IF and W46_IF

Gated Mode with Final Chip Set

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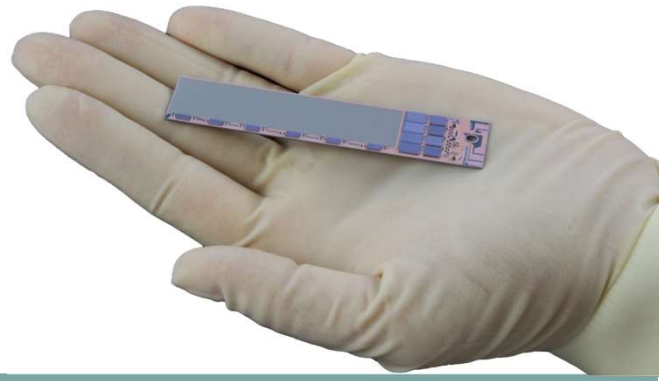
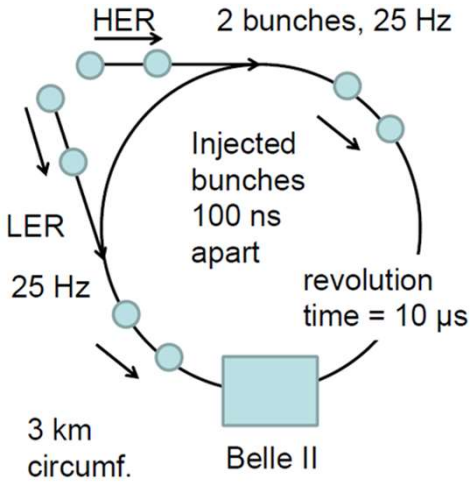
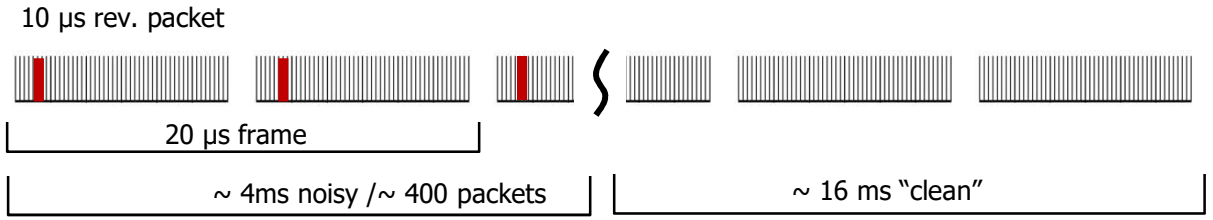


SuperKEKB Injection Scheme – Need of Electronic Shutter



10µs packets with 2503 bunches , 200 ns gap in-between (TDR)



- continuous injection → ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
- DEPFET integrates two trains, these noisy bunches would blank the frames → 20% loss of data

- the best solution: gate the DEPFET during the passage of the noisy bunches
- ~100ns gate, with some rise and fall times, twice per frame → 2x2µs of 20 µs blind
- assuming 4 ms relaxation time (not clear), ~200 consecutive frames with gate cycles

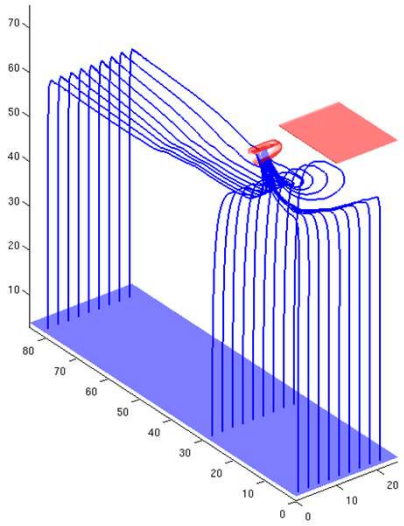
- DEPFET operation mode during gating: DEPFET off, Clear active (Vgs=3 .. 5V, Vclear=16 .. 20V)

DEPFET Gated Mode Operation

Switching to gated mode:

» DHE receives signal from acc., sends "veto" → DHPT switches to gated sequence → controls Switcher

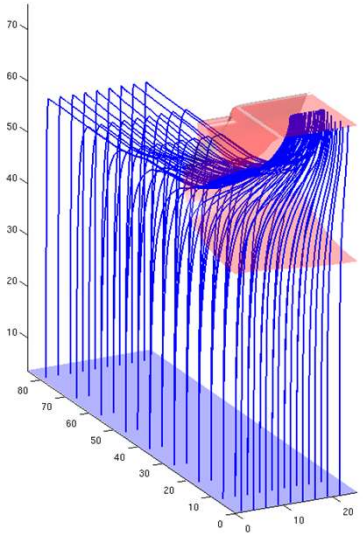
» DCD operation mode remains untouched



Normal charge collection

» Vgs=4V, Vclear=5V

» all signal charge collected in internal gate



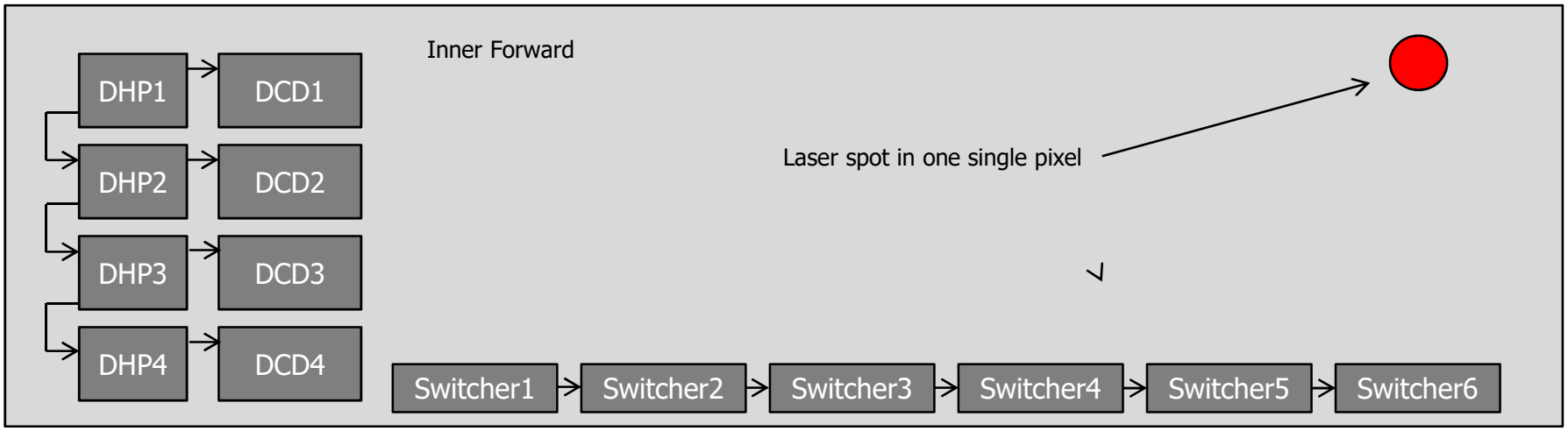
Gated mode

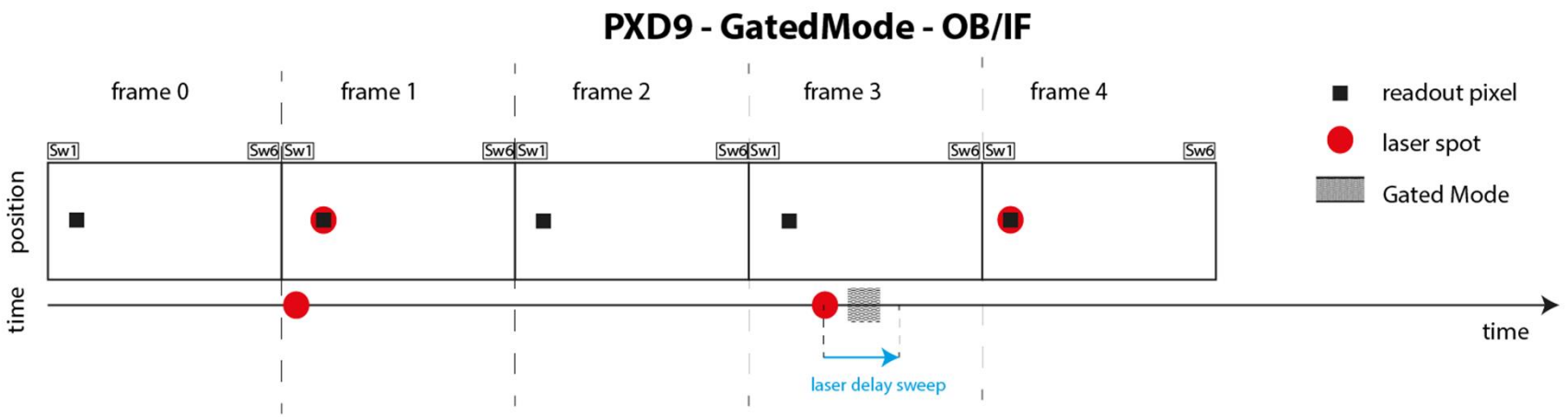
» Vgs=4V, Vclear=20V

» all signal charge dumped to *Clear*

Challenge: switch all *Clear* contacts in the matrix from ~5V → ~20V
shown on small matrix, but as expected, it's more difficult on large modules

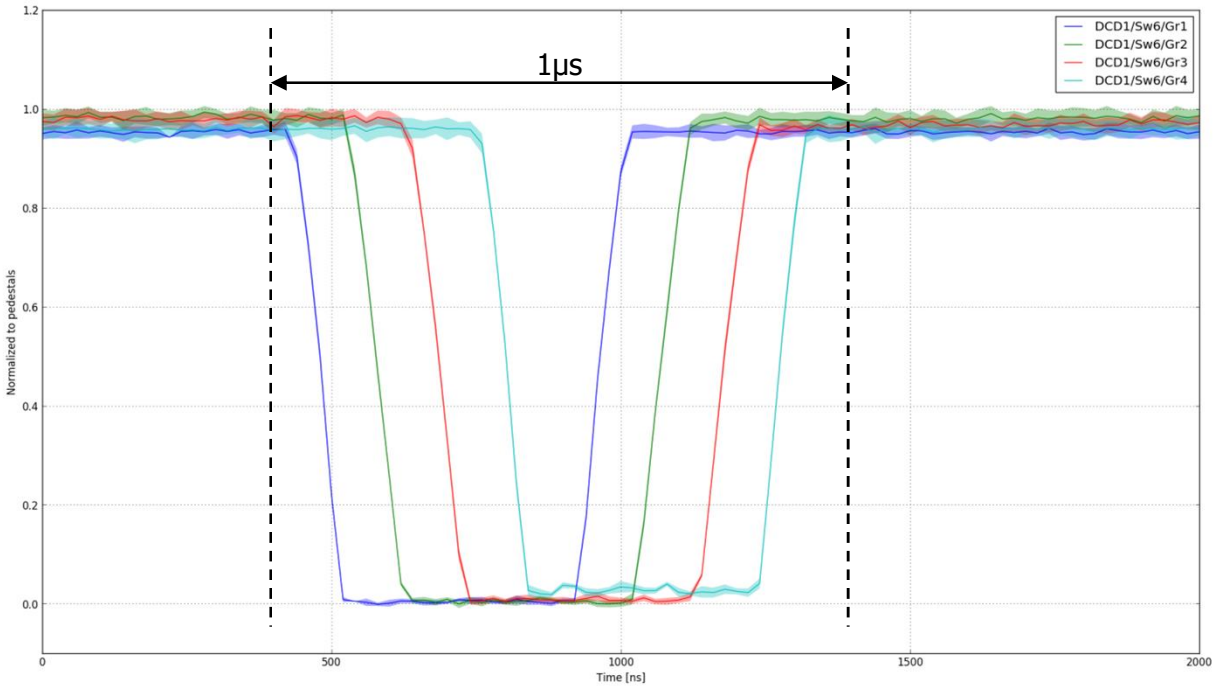
Gated Mode Laser Tests





frame 0: pedestals
frame 1: pixel shows signal of the laser impinging in frame 1 (right before the pixel is read)
frame 2: pixel shows Clear efficiency
frame 3: pixel shows pedestal value; gated mode is switched on ; laser is impinging
frame 4: pixel shows signal (charge conservation & junk charge prevention), depending on timing of laser

Gated Mode Laser Tests

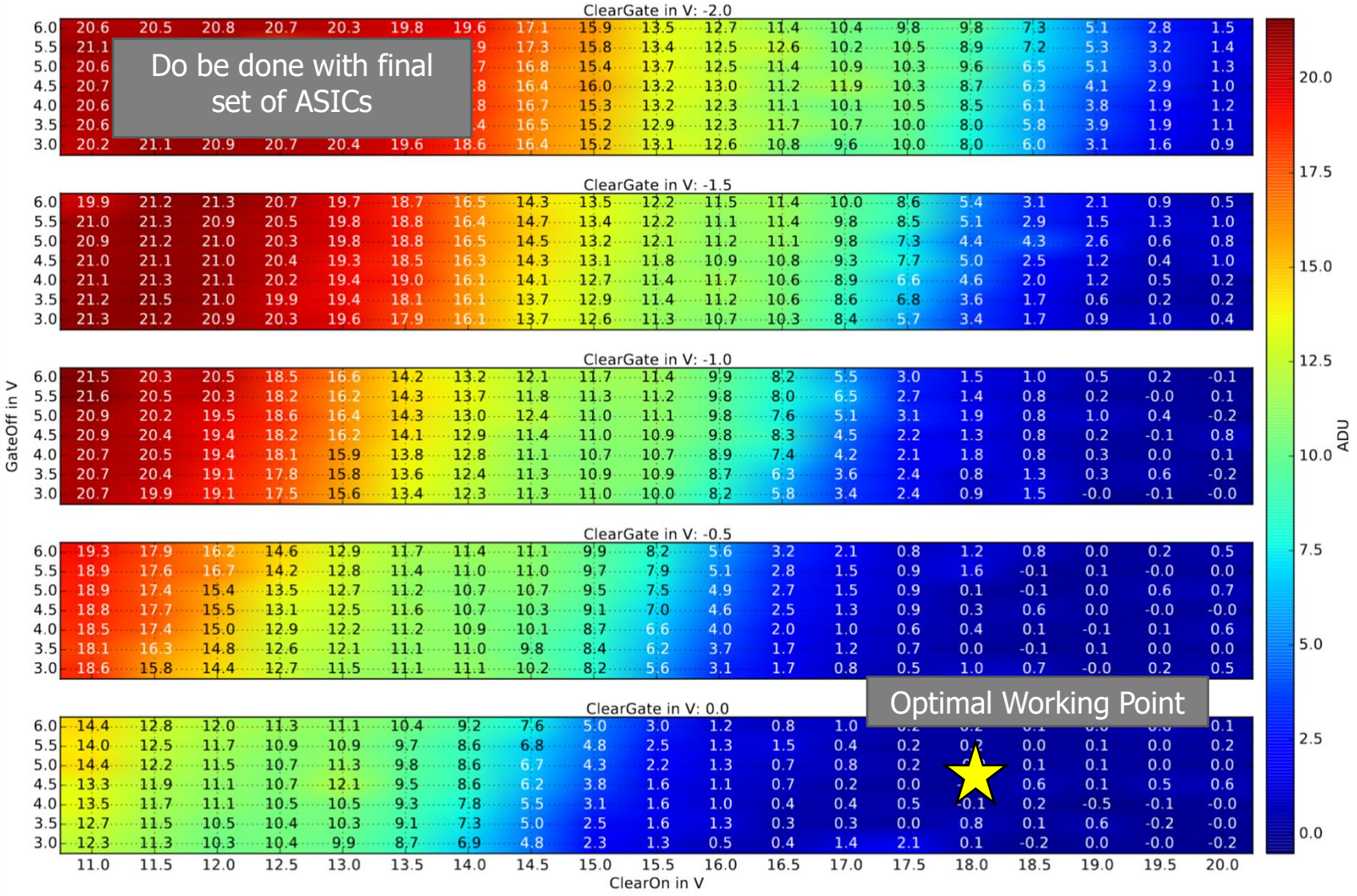


Plot shows the normalized signal charge which is created by the laser before, during and after the Gated Mode.
X-axis shows the timing of the laser.

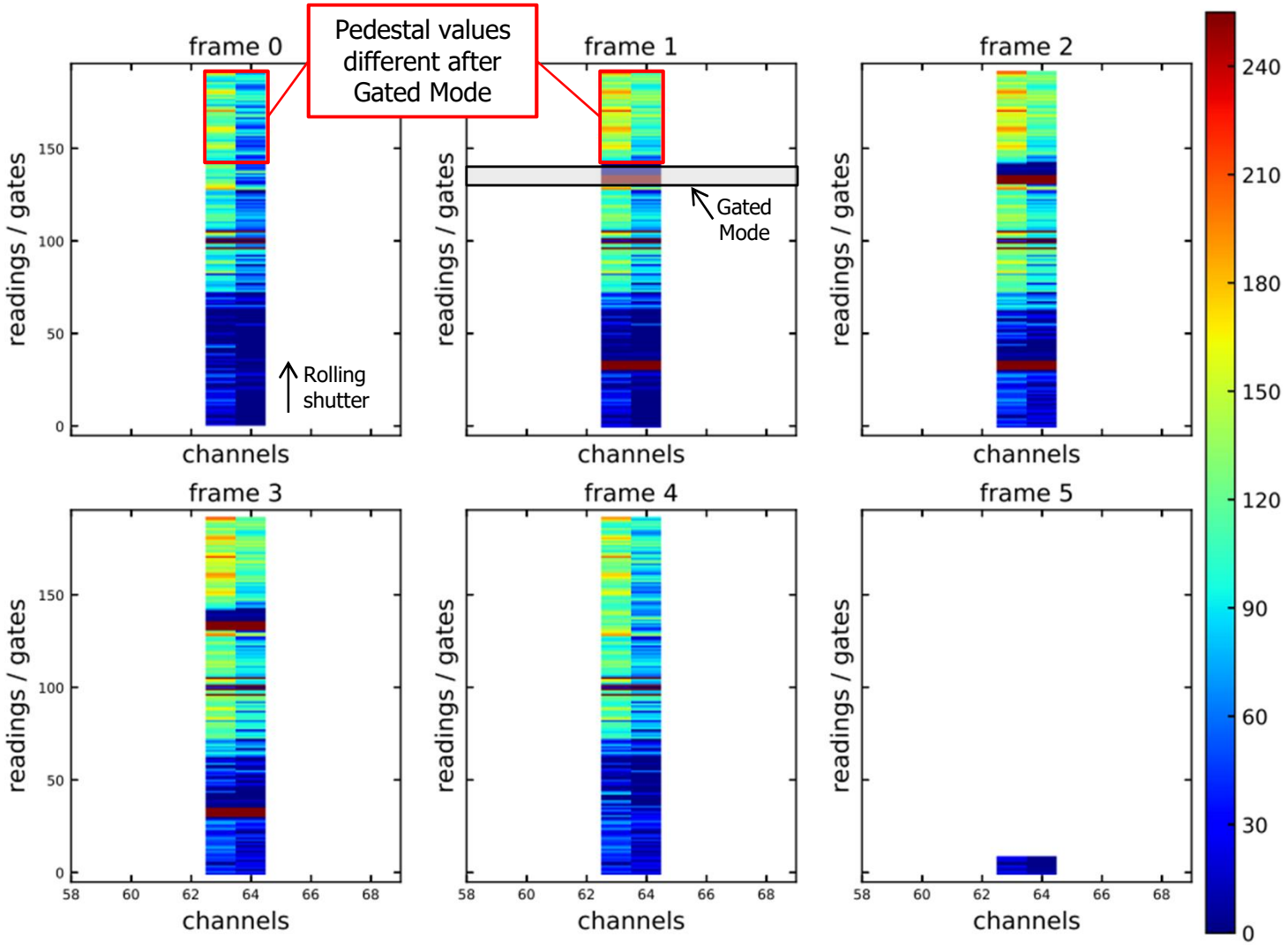
- New gated mode sequence (since DHPT1.2b does not execute memory address 512 twice)
- Gated Mode with Read-out shields the four tested areas (last switcher, all channel groups)
- Basic verification of the Gated Mode with final ASICs and at nominal frequency: ok
- Voltage scans and measurements with respect to the pedestal oscillation after GM still necessary
- Since W37_IF is used for Phase II, W46_IF is installed @ HLL
- Necessary measurements to be done in the next two weeks

Voltage Scan – W30_OB1 (not final ASICs)

Example: Junk Charge Prevention



Pedestal Oscillations (2 x GM in Frames 1, Frame 2 and Frame 3)



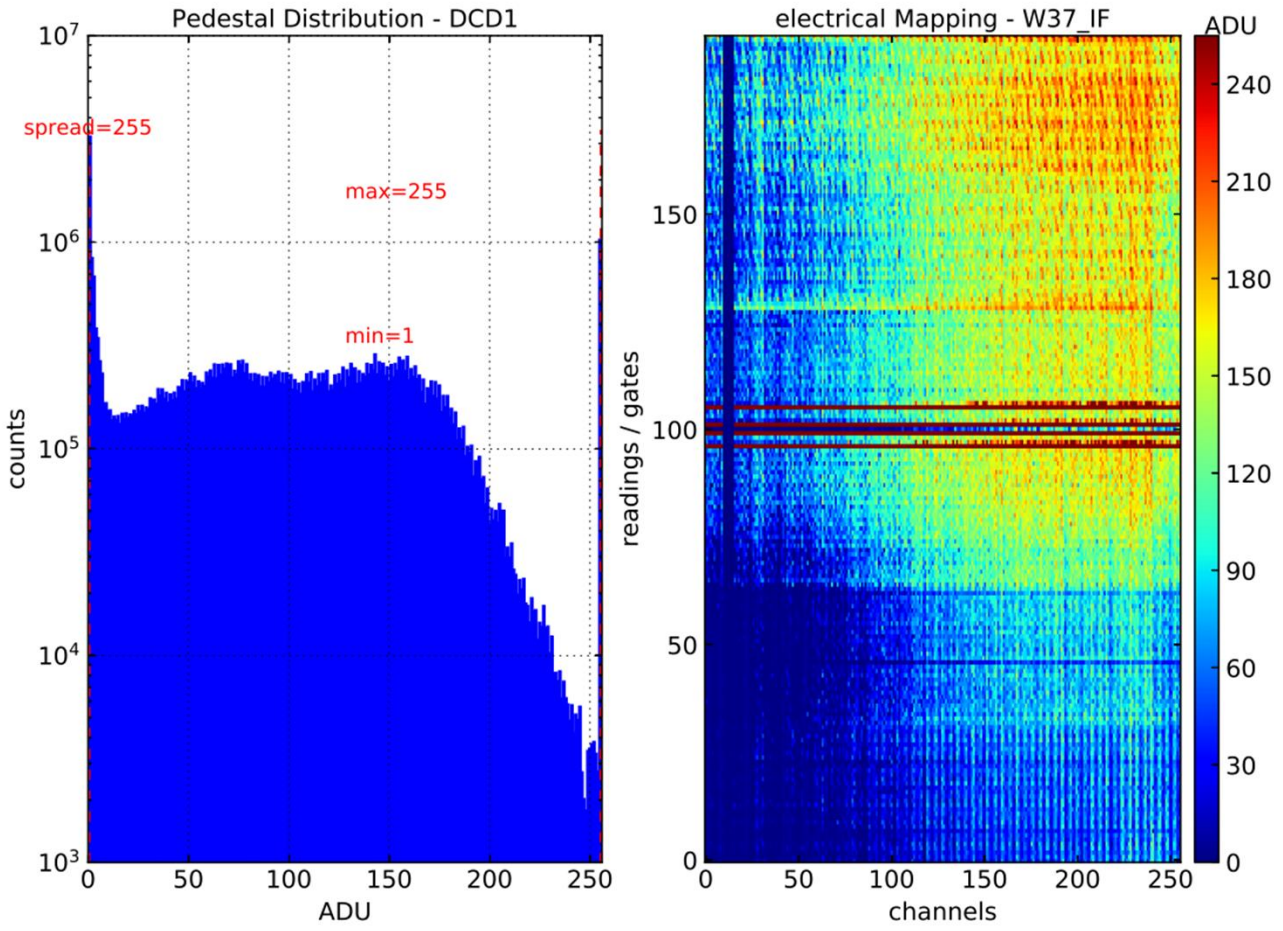
- No analog common mode correction applied
- **Investigation on the pedestal oscillation after GM still necessary**

Status & Summary

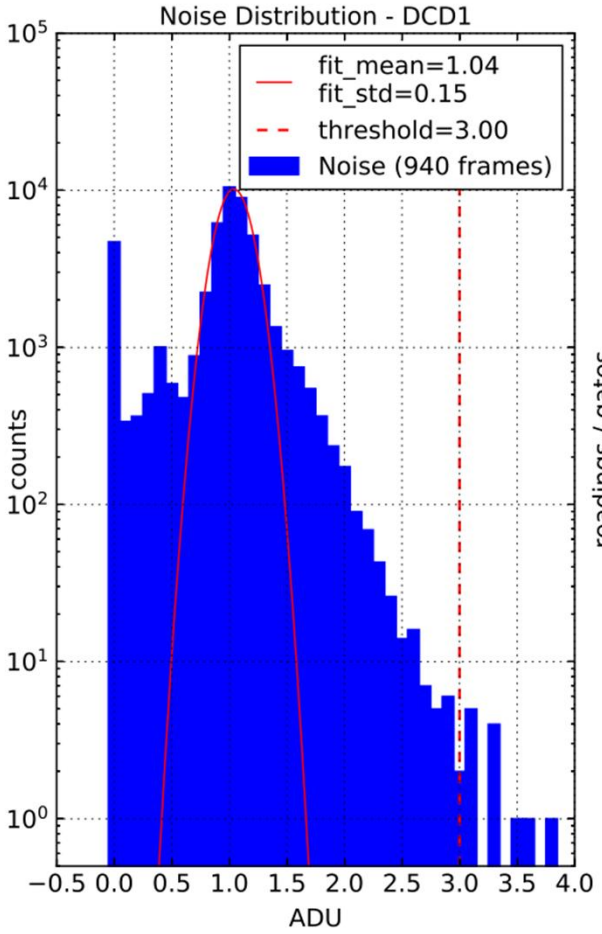
- Gated Mode tests of the final hardware (module with final set of ASICs and final services) not yet complete
  - Basic Gated Mode functionality demonstrated with W37_IF (now Phase II)
  - PXD dead time due to the Gated Mode and Pedestal Oscillations not yet measured with final set of ASICs
  - W46_F installed at HLL to complete the GM Tests: voltage scans and pedestal oscillations
- Results of the Gated Mode testing could be presented together with results/status of the Module Testing

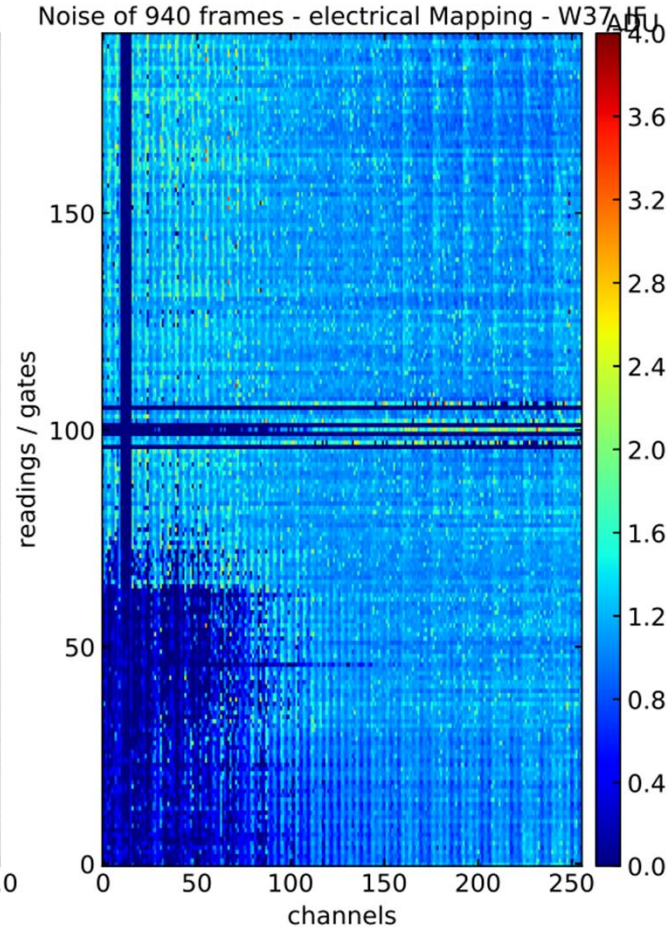
Back-up

W37_IF different VNSubIn DCD1

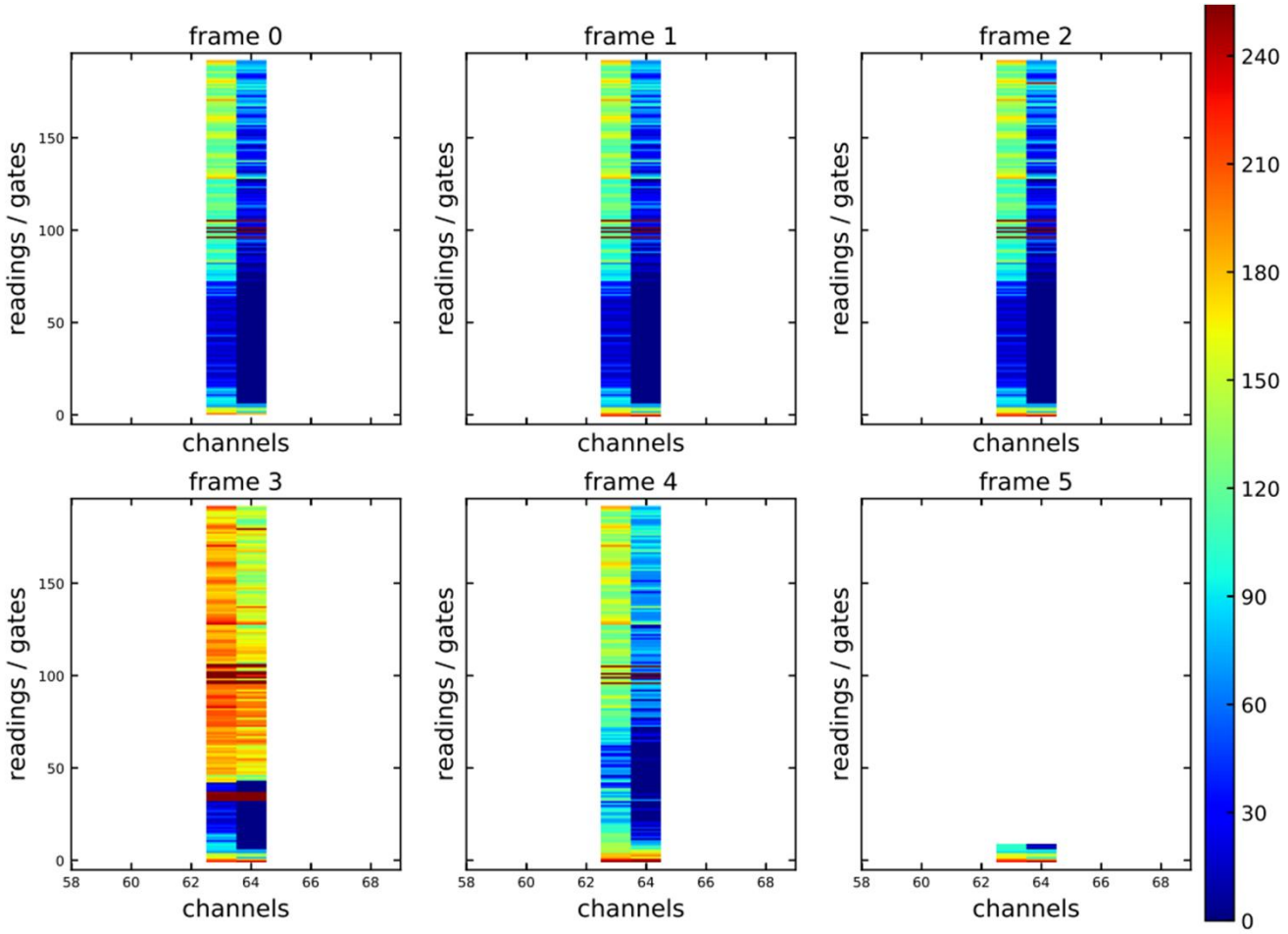


W37_IF Noise DCD1



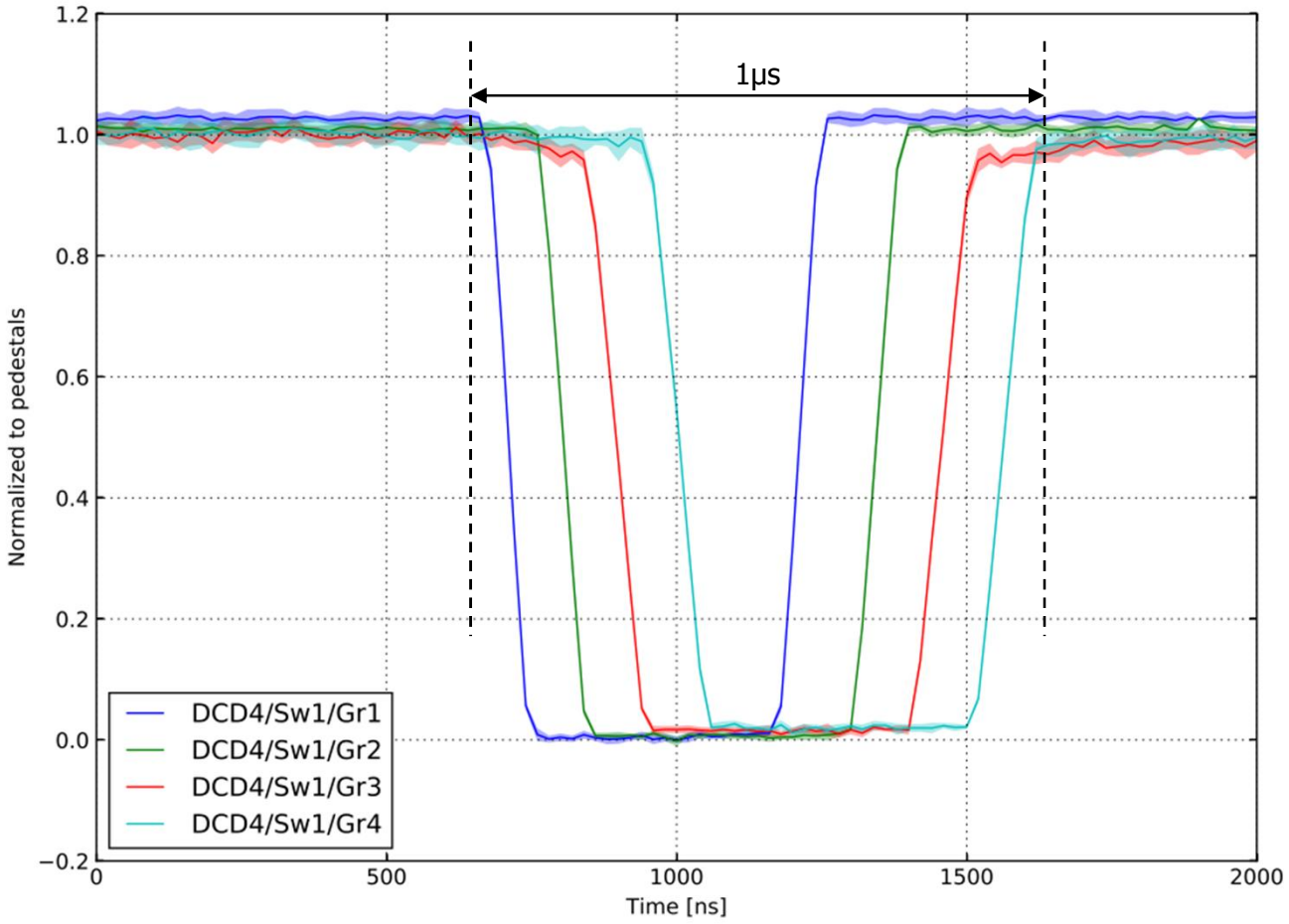


W37_IF Gated Mode during Frame 3



- Long Gated mode timing (Frame3)
- Different pedestals during GM frame

W31_OF1 (PXD9 Pilot Run)



Pedestal Oscillation W31_OF1