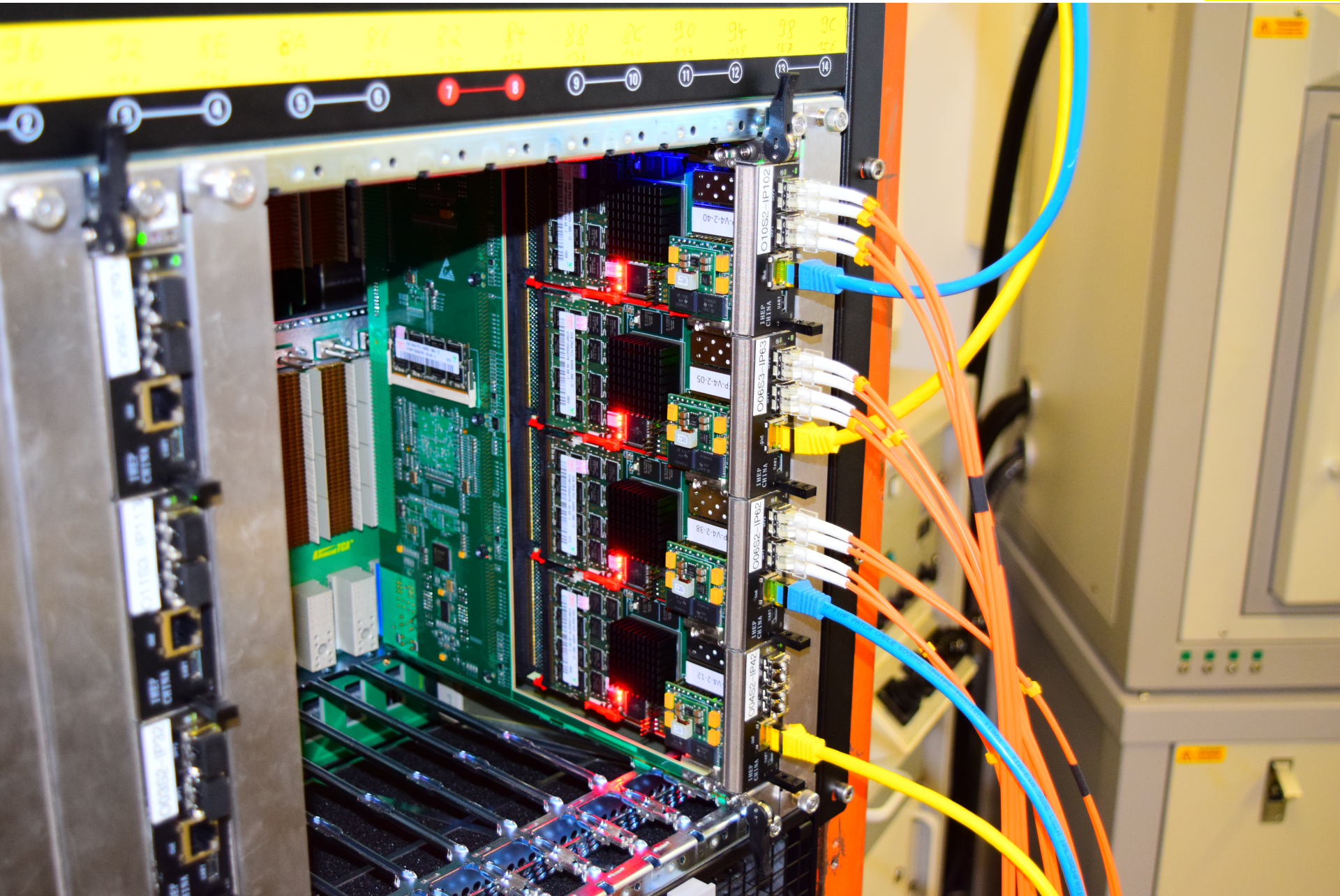
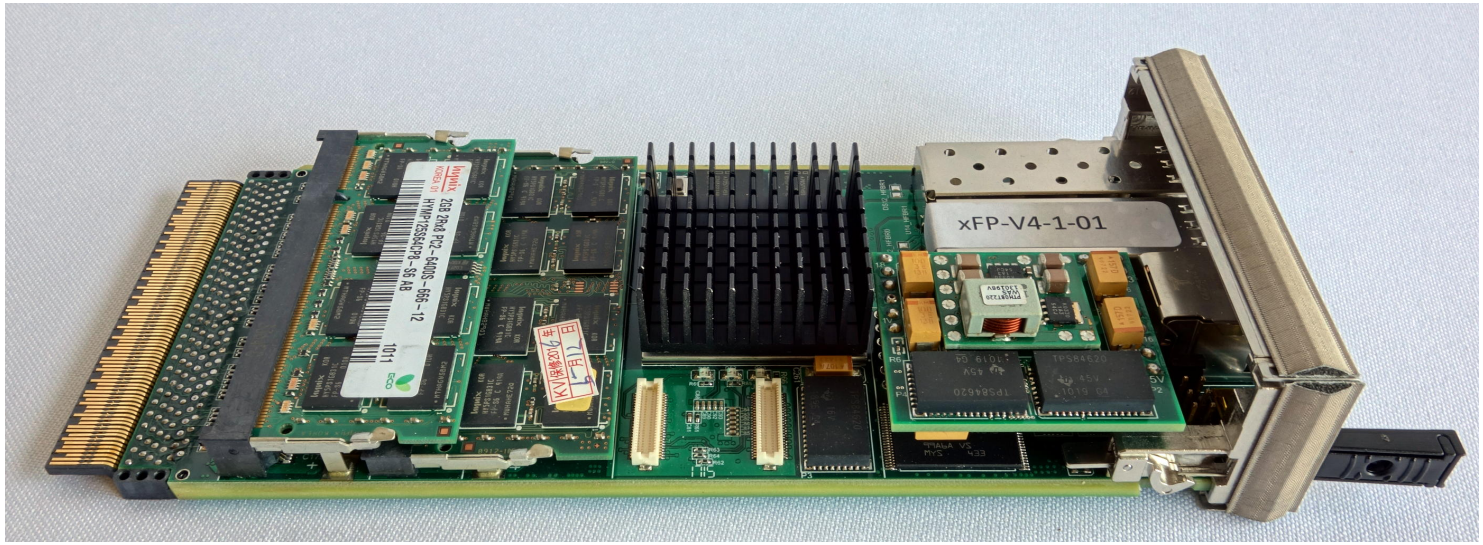
PXD Pre-Meeting : ONSEN Update



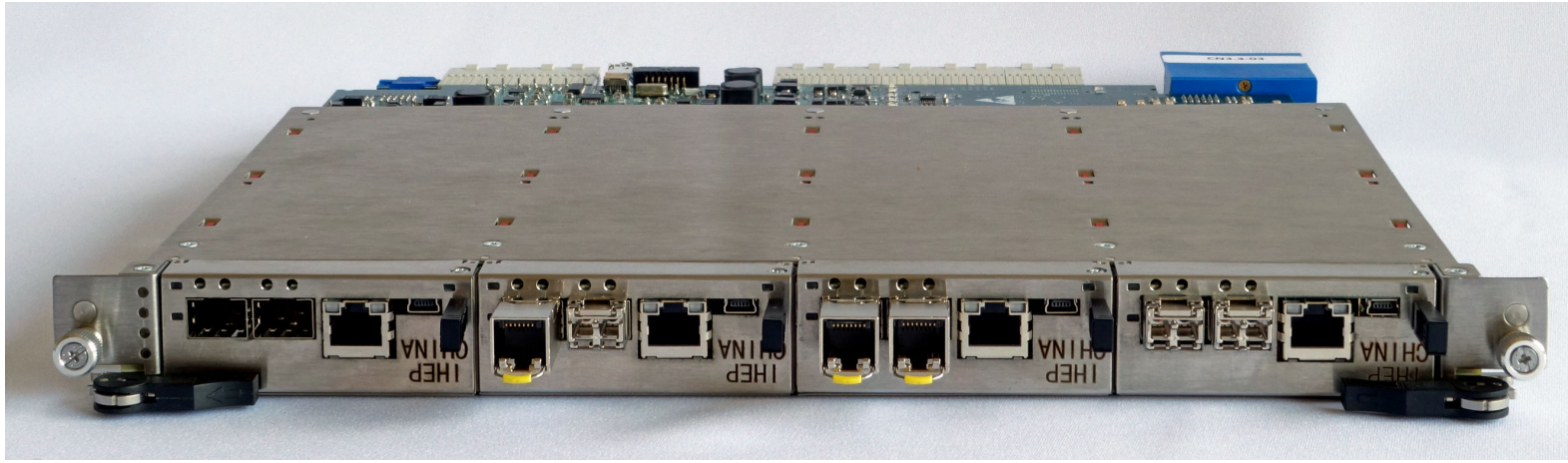
Overview of ONSEN

- Hardware
- Firmware / Software Development
- Phase 2 Preparations
- Full Rate Test
- Plans

Hardware



xFP card
v4.0
Nov. `14



CNCB
v3.3
May `15

Hardware Upgrade

- **First stage:** upgrade CNCB (but remain compatible with current xFP)
- **FPGA:** Change to Xilinx UltraScale architecture

	Virtex-4 FX60 (CNCB)	Virtex-5 FX70T (xFP)	Kintex UltraScale 060 (Upgrade)
Registers	50k	44k	663k
LUTs	50k × 4-input	44k × 6-input	332k × 6-input
DSP Slices	128	128	2760
BRAM	4 Mb	5 Mb	38 Mb
MGT	16 × 6.5 Gbps	16 × 6.5 Gbps	32 × 16.3 Gbps
CPU	PPC405	PPC440	-

CN_V4 Design ongoing, nearly finished

Jingzhou ZHAO, Zhen-An LIU, Wenxuan
GONG Trigger Lab, IHEP, Beijing

Setup

Phase 2

1 Merger node for HLT and DATCON

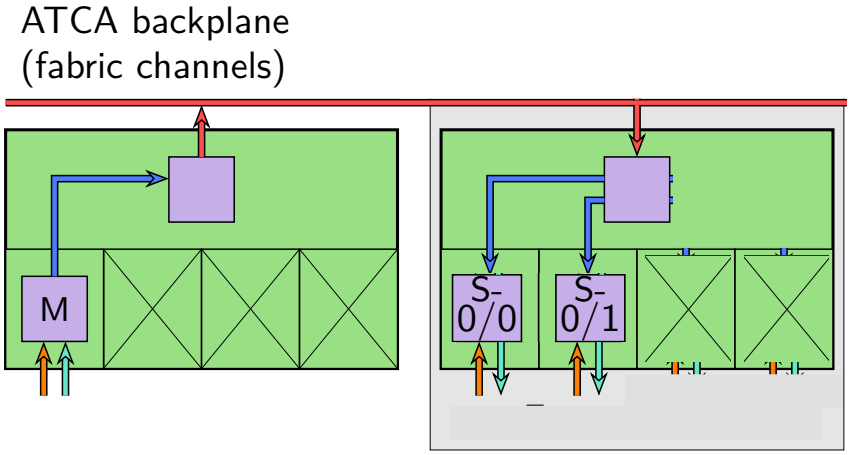
2 Selector nodes for ROI selection

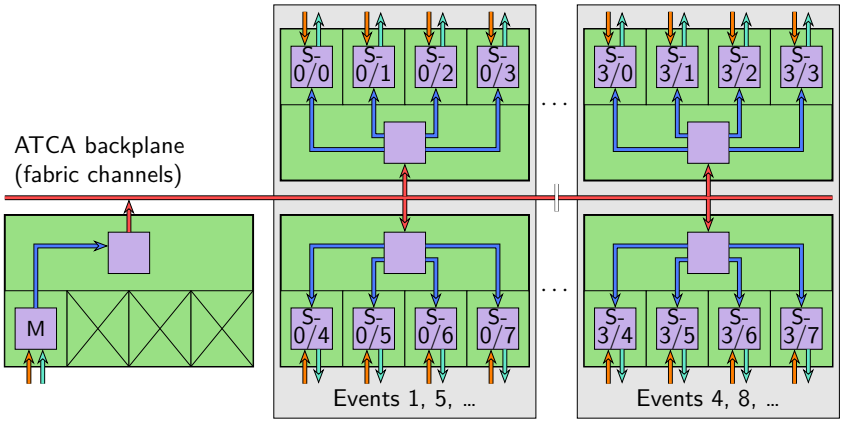
Phase 3

1 Merger node for HLT and DATCON

32 Selector nodes for ROI selection

- incl. event distribution

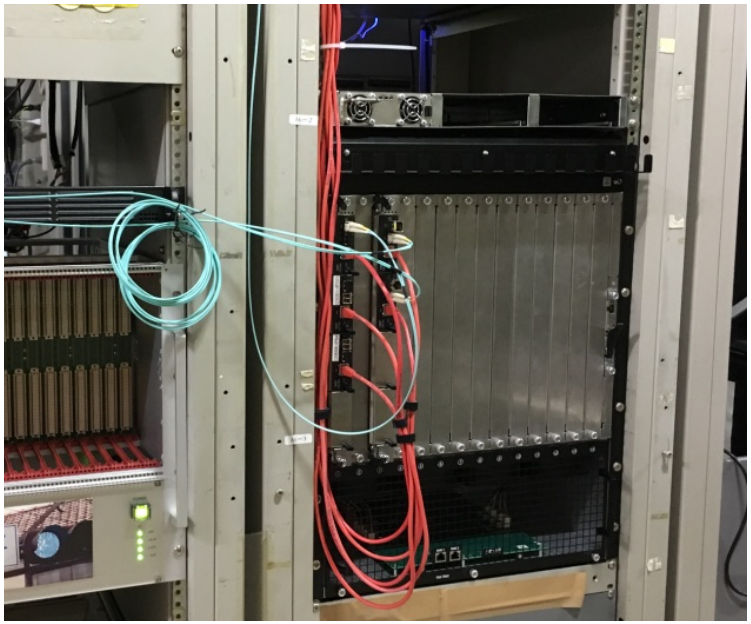




ATCA Shelf Setup

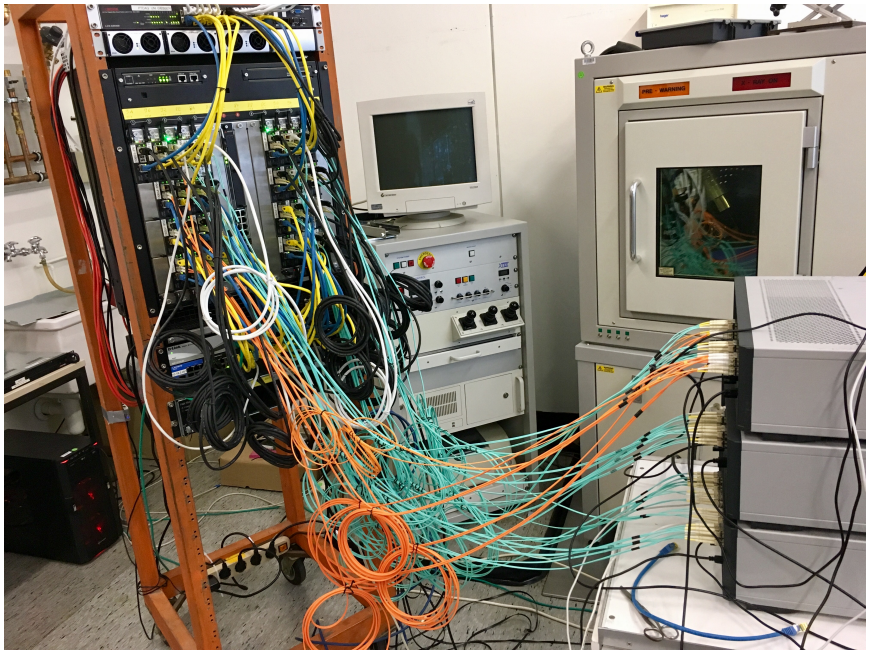
Phase 2

Picture of current setup at KEK



Phase 3

Picture of Full ONSEN Test



FW/SW Development

- Several firmware improvements and bugfixing
  - better handling of bad incoming data
  - huge internal update of filter process
  - update of epics connectivity
  - higher level of automation

- Less time required for flash or reset procedures

FW/SW Development

- Nearly all errors of previous beam test could be reproduced and cleared
- Implementation of version management into firmware and software (accessible via EPICS)
- ONSEN emulator allows verification of output

- Lab test in Giessen result excepted behavior and shows performance improvement

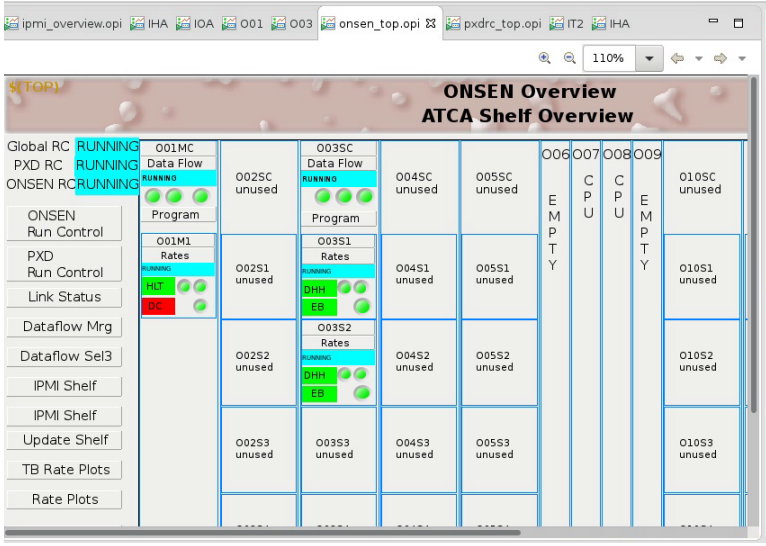
Phase 2 Preparations

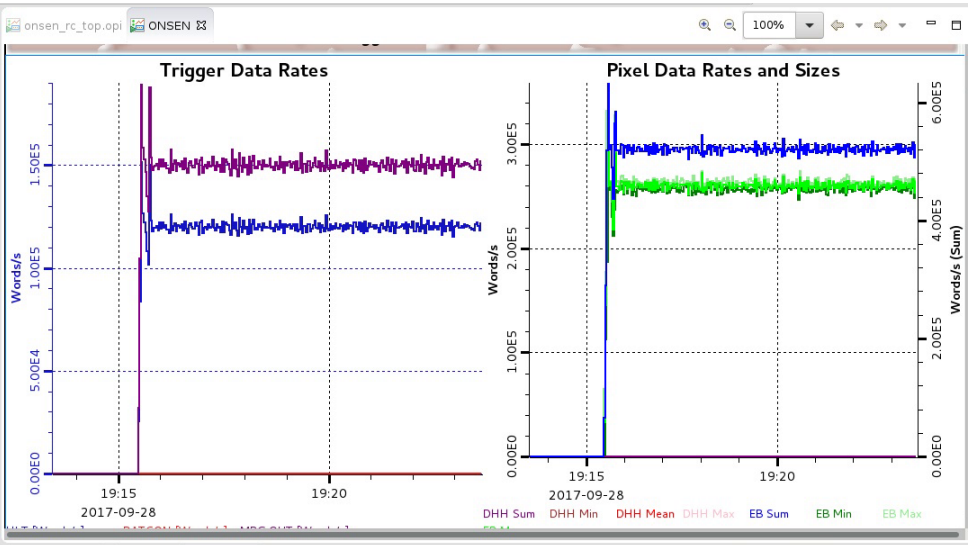
- ONSEN was moved in Tsukuba Hall from B3 to E-Hut and connected successfully to HLT, EB, DHH and DATCON (cabling, etc…)✔
- 1 CNCN & 4 xFP cards as spare brought to KEK ✔
- Update of firmware and minor adjustments due to a different shelf configuration✔
- Integration in Global RunControl ✔

Phase 2 Preparations

- DAQ Tests with HLT and EB successful ✔
- DAQ Tests including DHH
- DAQ Tests including DATCON

} planned for coming weeks





Full Rate Test

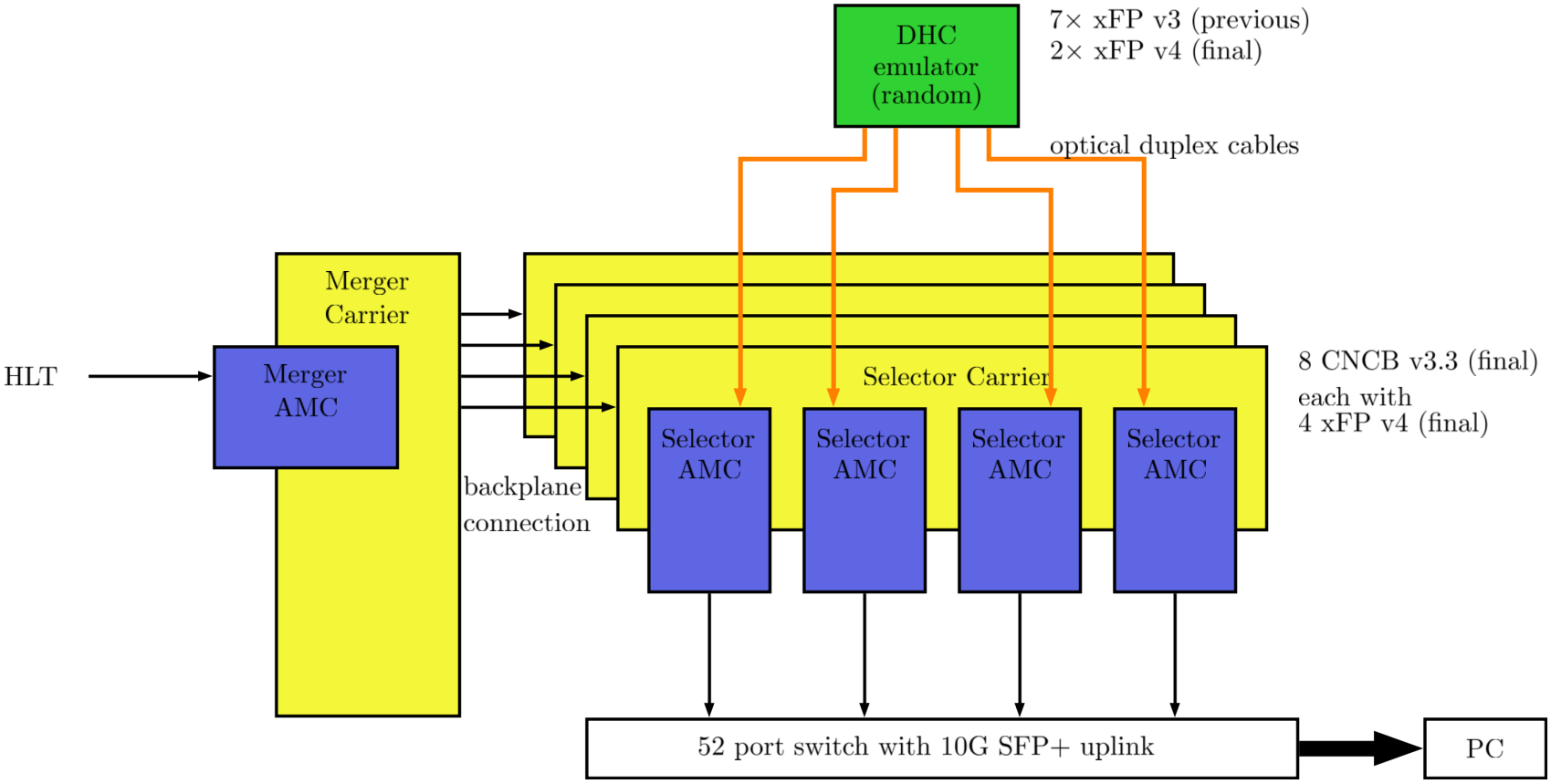
- ONSEN is prepared and set up at KEK
- Hardware is in final state and runs quite well
  - one voltage was fluctuating due to different capacitors -> fixed now
  - some xFP cards have flash problems and are already shipped to IHEP for repair -> ongoing
- Is ONSEN hardware and firmware ready to handle proposed data rate?

Full Rate Test

- For each AMC ~ 550 MB/s input per DHC link
  - ¼ of final trigger rate (7.5 kHz)
    32 cards in total: 17.6 GB/s
- 7.5 kHz trigger rate of HLT
  - Rejection factor of 2/3
  - Simplified ROI distribution atm.

Full Rate Test

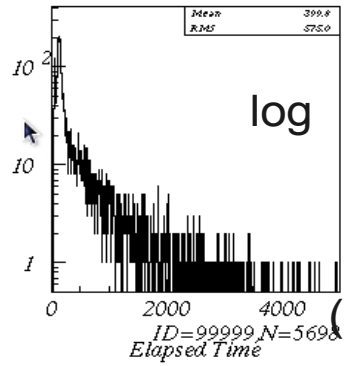
- Schematic setup



Used Data

- ROI generated by software on local PC with different patterns
  - Send all 0/1
  - Accept 1/3/10
- DHC data with 5 DHE each with 4 DHP
  - 3% occupancy at 6.25 Gbps line rate
  - Random row-column-adc combinations
- Synchronized: HLT & DHC emu

Workshop on PXD-DAQ (2010)
https://indico.mpp.mpg.de/event/797/



3.2GHz
Intel Xeon,
e-time / core.

Test results

- 3 weeks testing and finalizing software
- No connection interrupts (backplane and ext.)
- No buffer overflows (level ~73%)
  - Trigger delay: constant 1 second
  - with poisson (peak 0.2 s, tail up to 5 s): ~30%
- No framing errors / data format errors
  - Same performance with CRC erros (tested)
- Multiple start/stop without cold start
- Stable temperature in ATCA shelf (FPGA:~60C)

Test results

- Several small runs, storing binary output data on SSD for cross check
- Two long runs over weekend (→ /dev/null)

- Maximum trigger rate at 8kHz (limited by DHC aurora line rate): ~595 MB/s
- Send all with reduced data rate of 600 Hz and no rejection factor

Future plans

- ROI distribution for phase 3
- Rest of hardware for phase 3 will be shipped to KEK after PERSY
- backup solution of ONSEN<->EB connection
  - data bonding via C-RORC (PCIe card)
- Update of hardware
  - used FPGA is not available anymore