



Test reports from MPP

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DEPFET Lab 04.10.2017



Module checks before glueing

- **DHPT high speed (HS) Links**
short scan (to have a reference for later)
 - bias 200 to 250, step 5 ~15 min
 - bias_d 100 to 150, step 5
 - delay 0
- **Delays** ~15 min
- **ADCs optimization using small parameter space** ~14 h (night scan)
- **Pedestal/noise (1k frames)** ~10 min
- **2-bit offset (delay and current source optimization)** ~ 15 min
- **Pedestal/noise (1k frames)** ~10 min
- **DCD analog common mode correction (ACMC)** ~1 min
- **Pedestal/noise (1k frames)** ~10 min
- **Source measurement different regions** ~ ? min/h
 - Threshold 5
 - Verify shape of the spectra
 - SNR in different regions
 - Adjust VNSubIn / Use ACMC



W47_IB: hs_link, delays, pedestals, adc_curves, sample_point_curve, offsets, pedestal & noise, APMC, source scan (currently ongoing)

W02_IB: hs_link, delays, pedestals, adc_curves, offsets, pedestals & noise, APMC, source ✓

W47_IF: hs_link, delays, pedestals, adc_curves, offsets, pedestals & noise, APMC,

W44_IF: under test

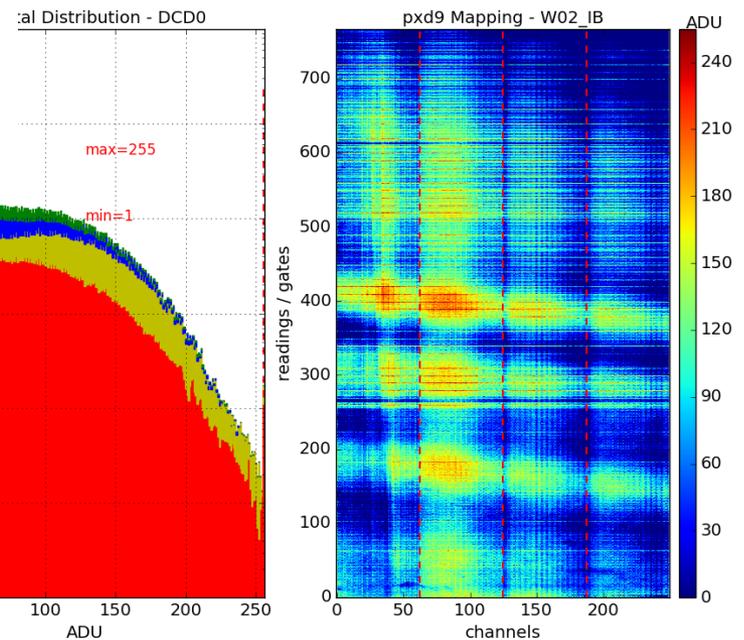
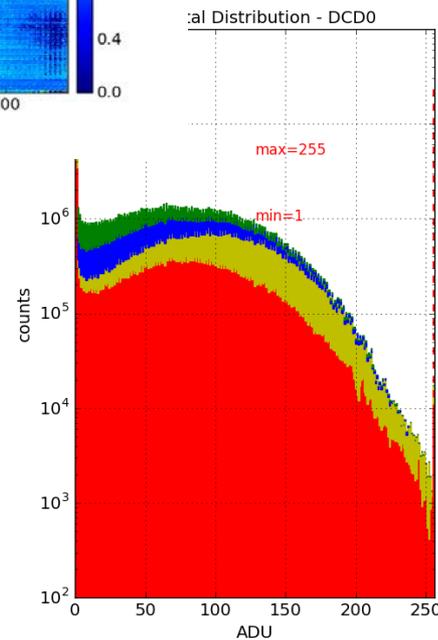
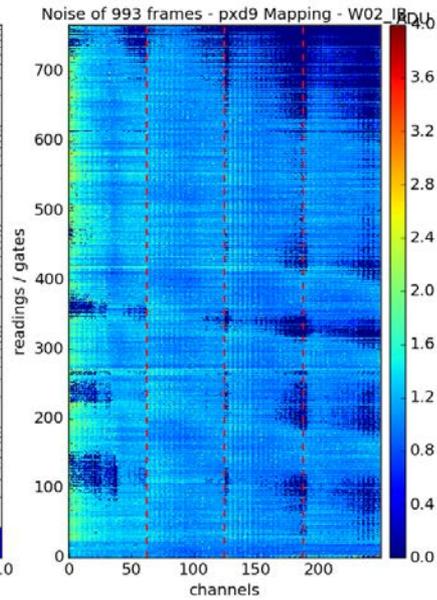
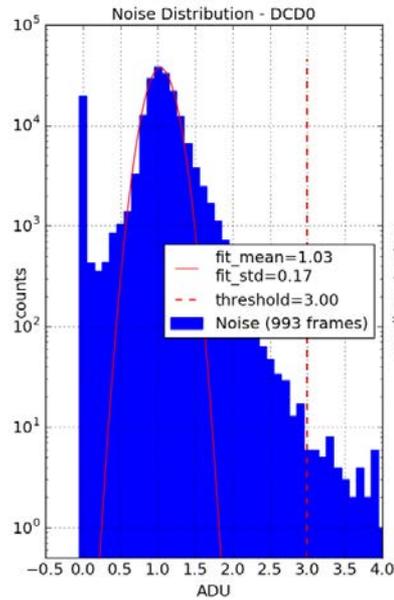
W46_IF. HLL for rings and GM



W02_IB

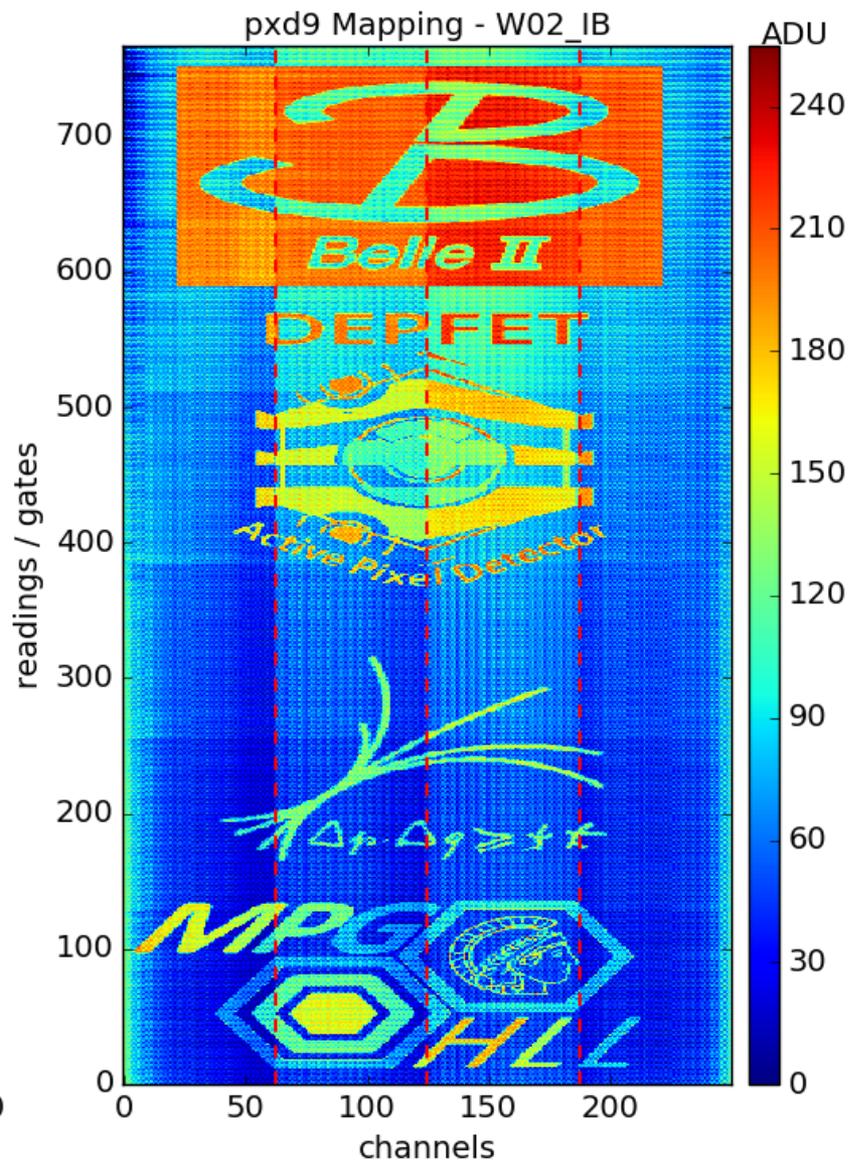
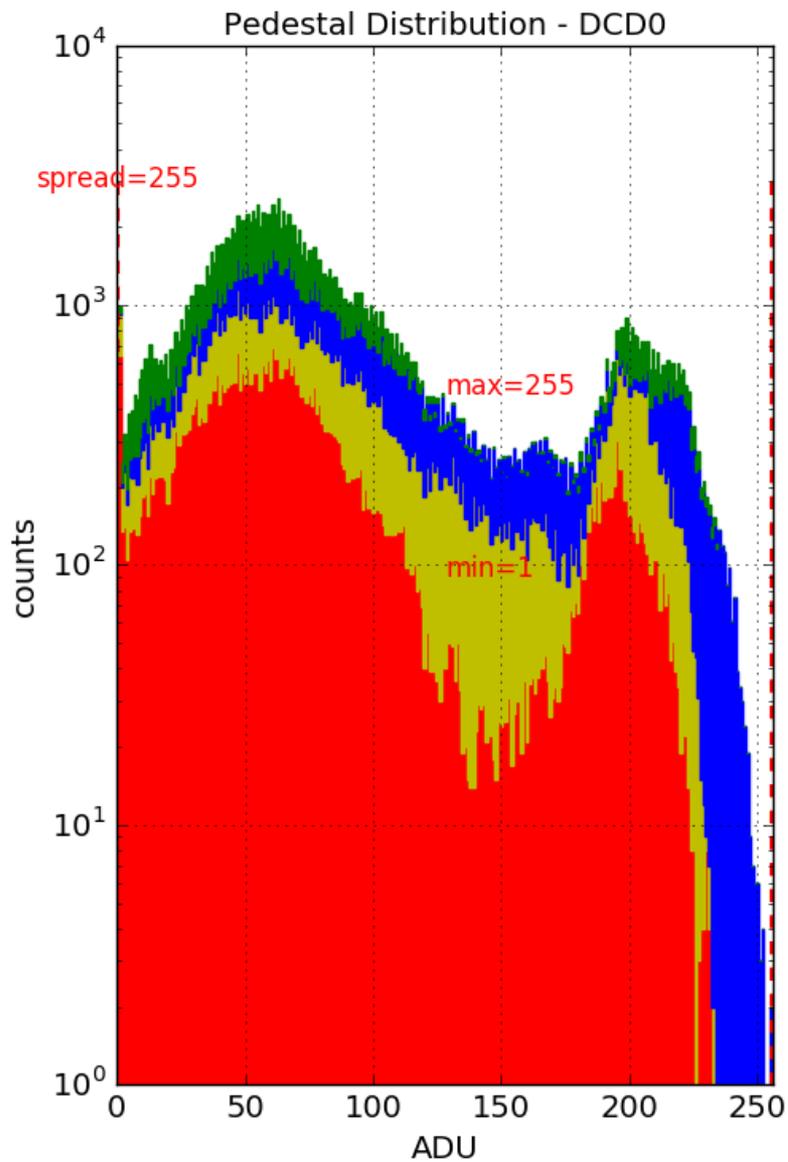


W02_IB – pedestals without offsets, without ACMC



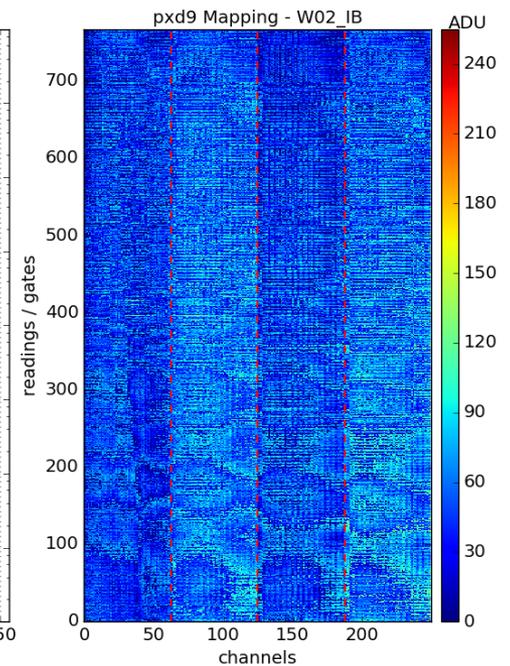
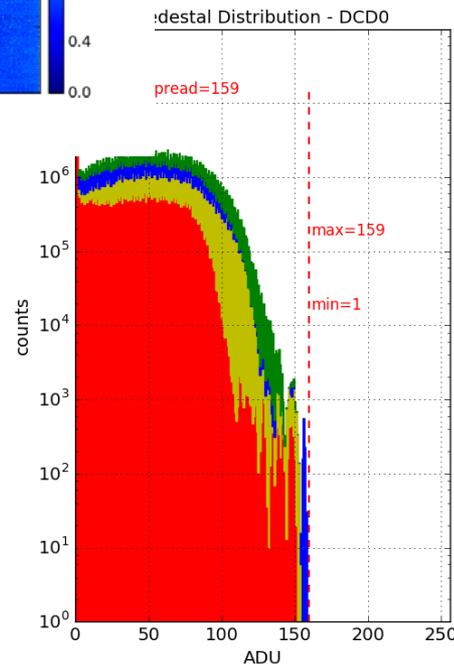
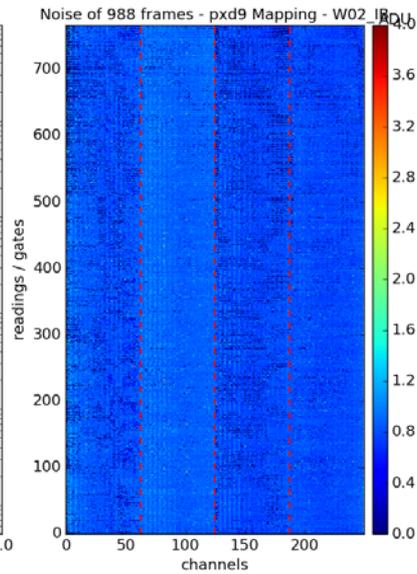
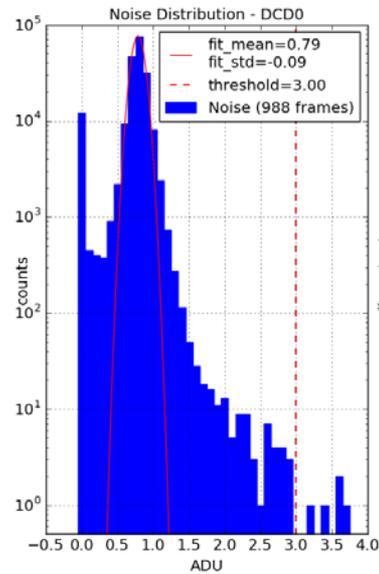


W02_IB – offset delays





W02_IB – pedestals with offsets, with ACMC

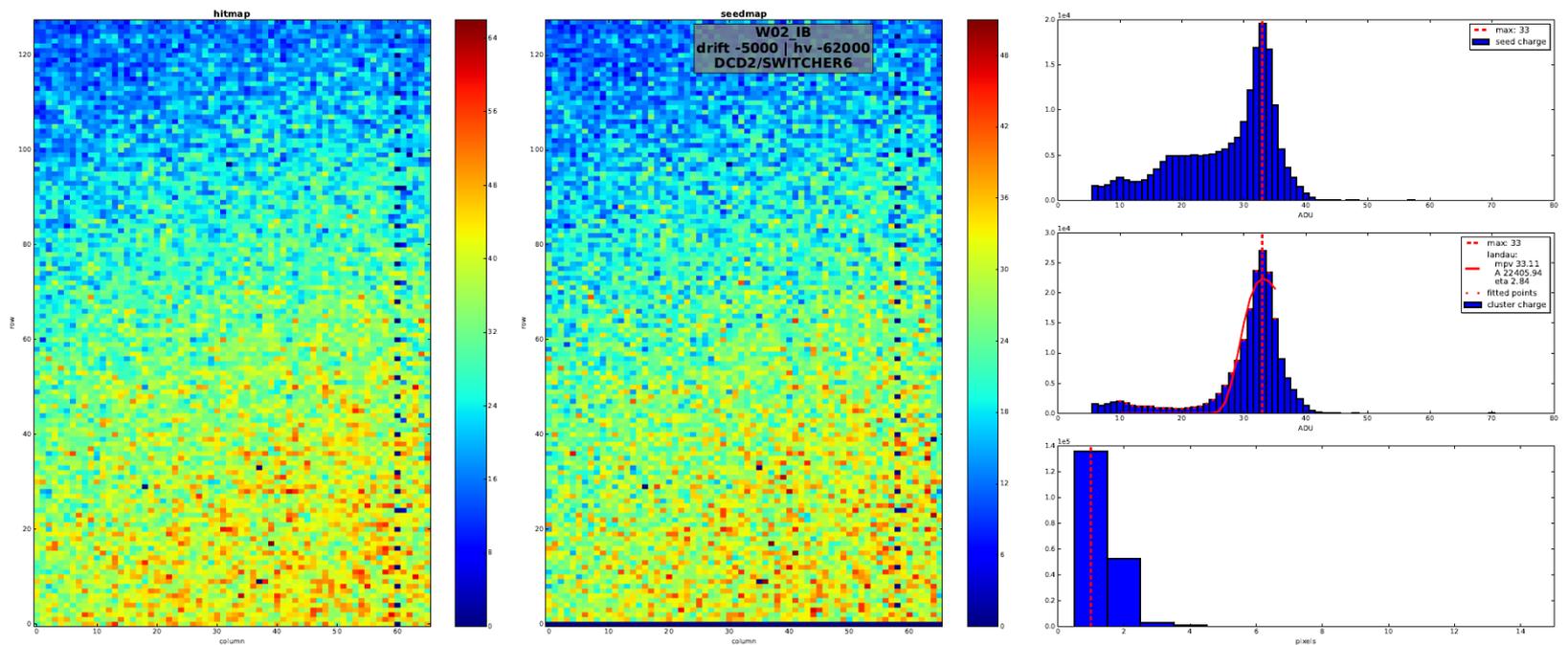




W02_IB - source

Measurement done

Analysis currently ongoing



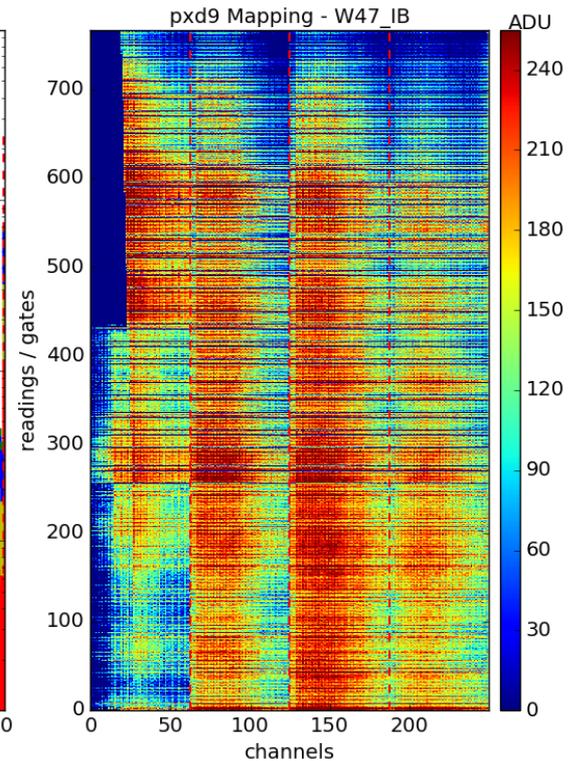
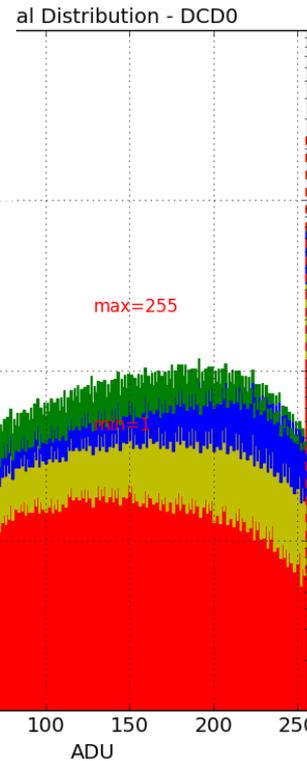
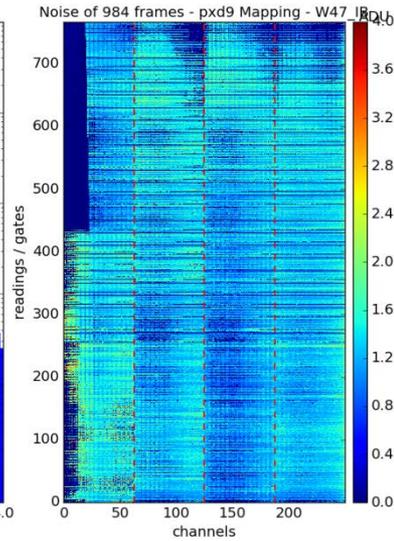
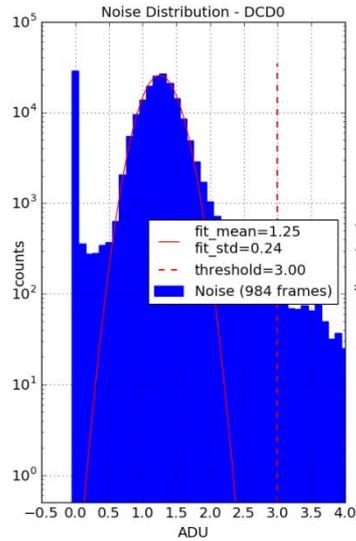
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W47_IB

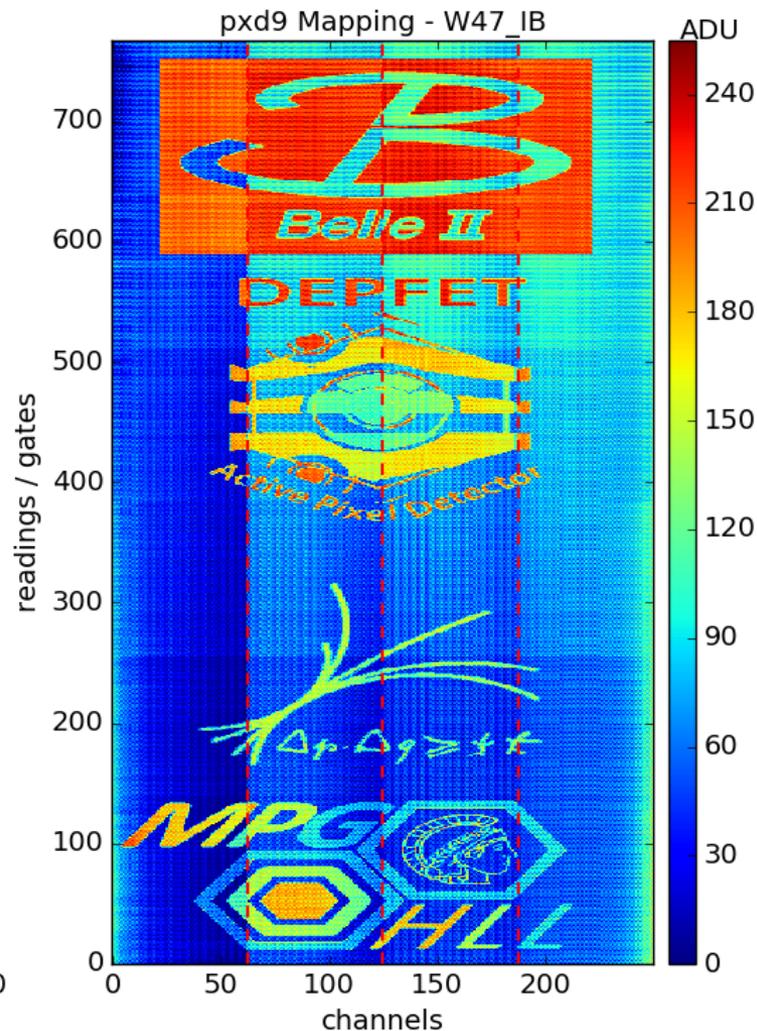
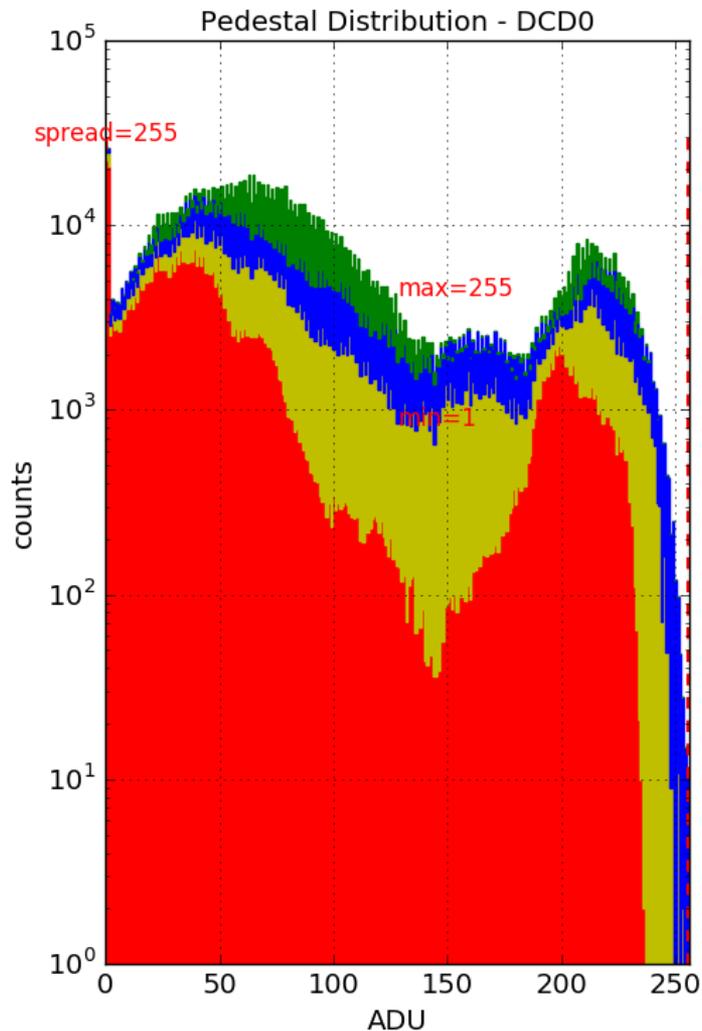


W47_IB – pedestals without offsets, without ACMC



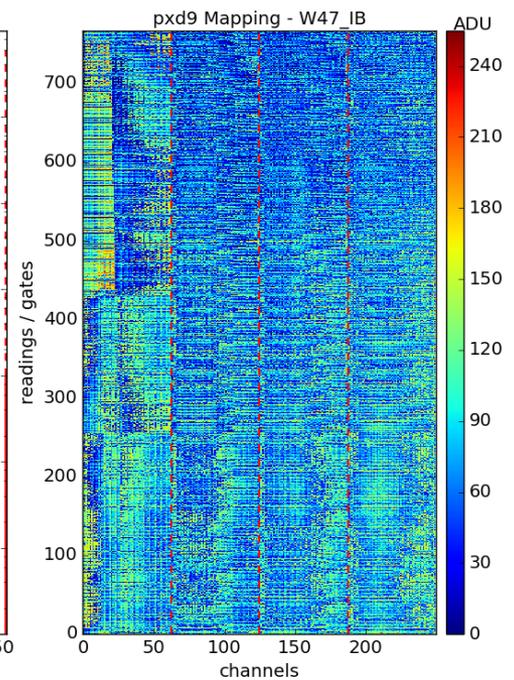
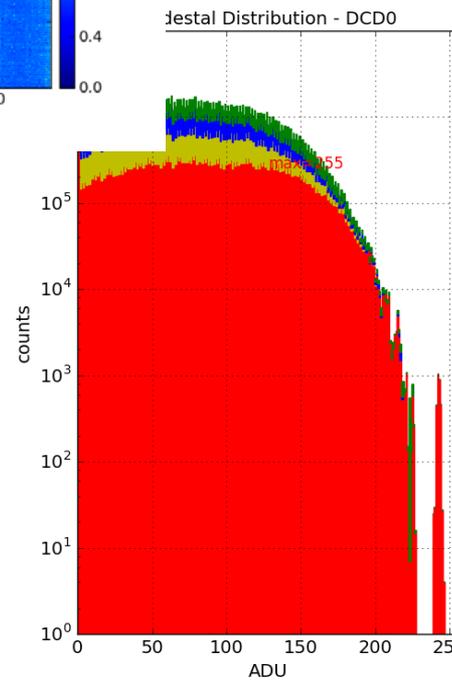
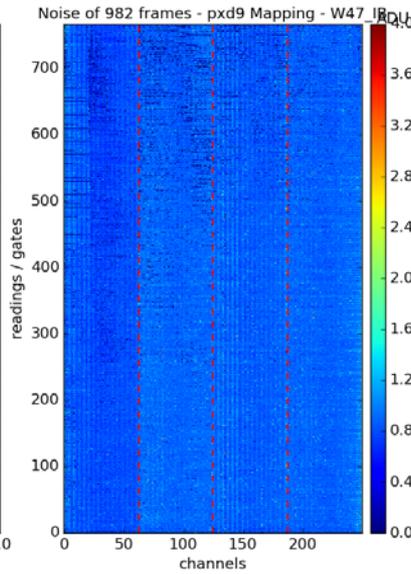
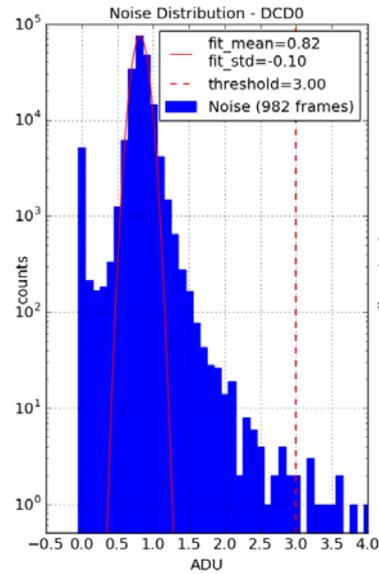


W47_IB – offset delays





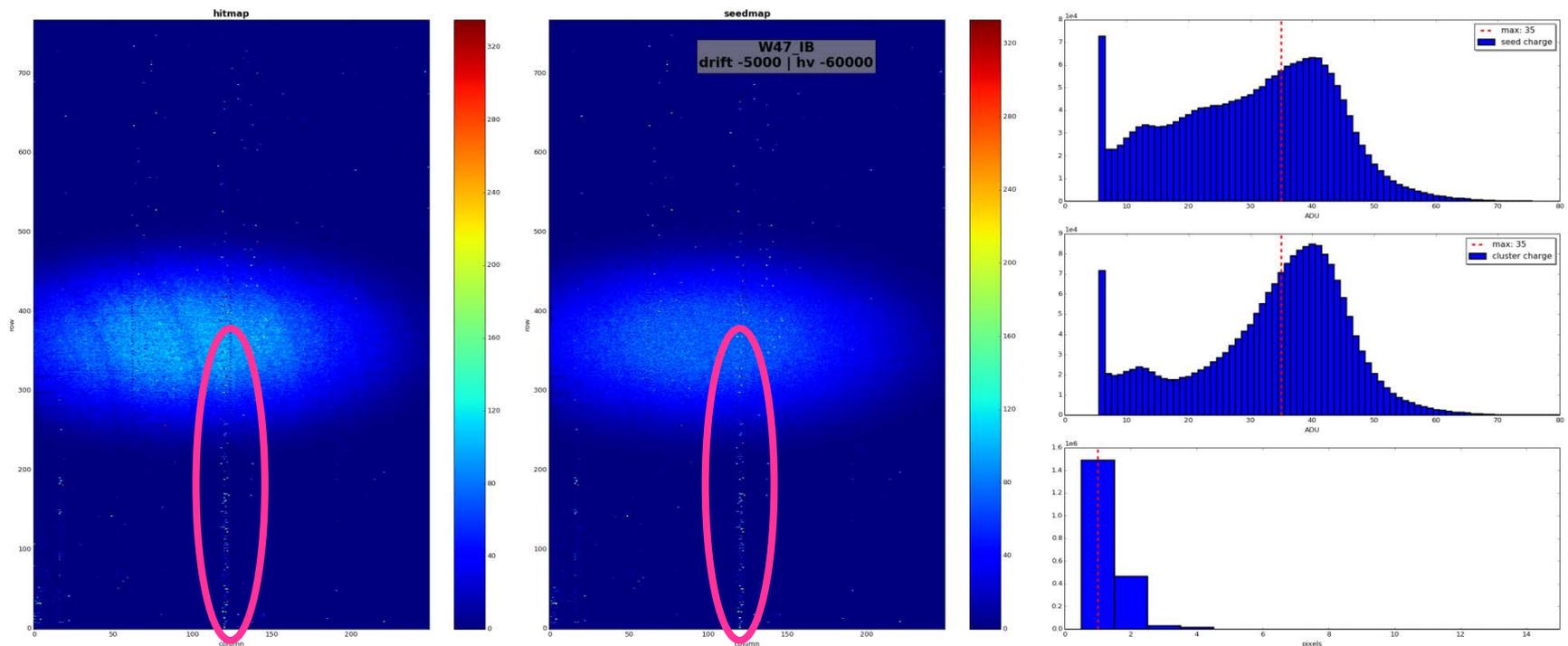
W47_IB – pedestals with offsets, with ACMC





W47_IB - source

Measurement currently ongoing & some noisy pixel



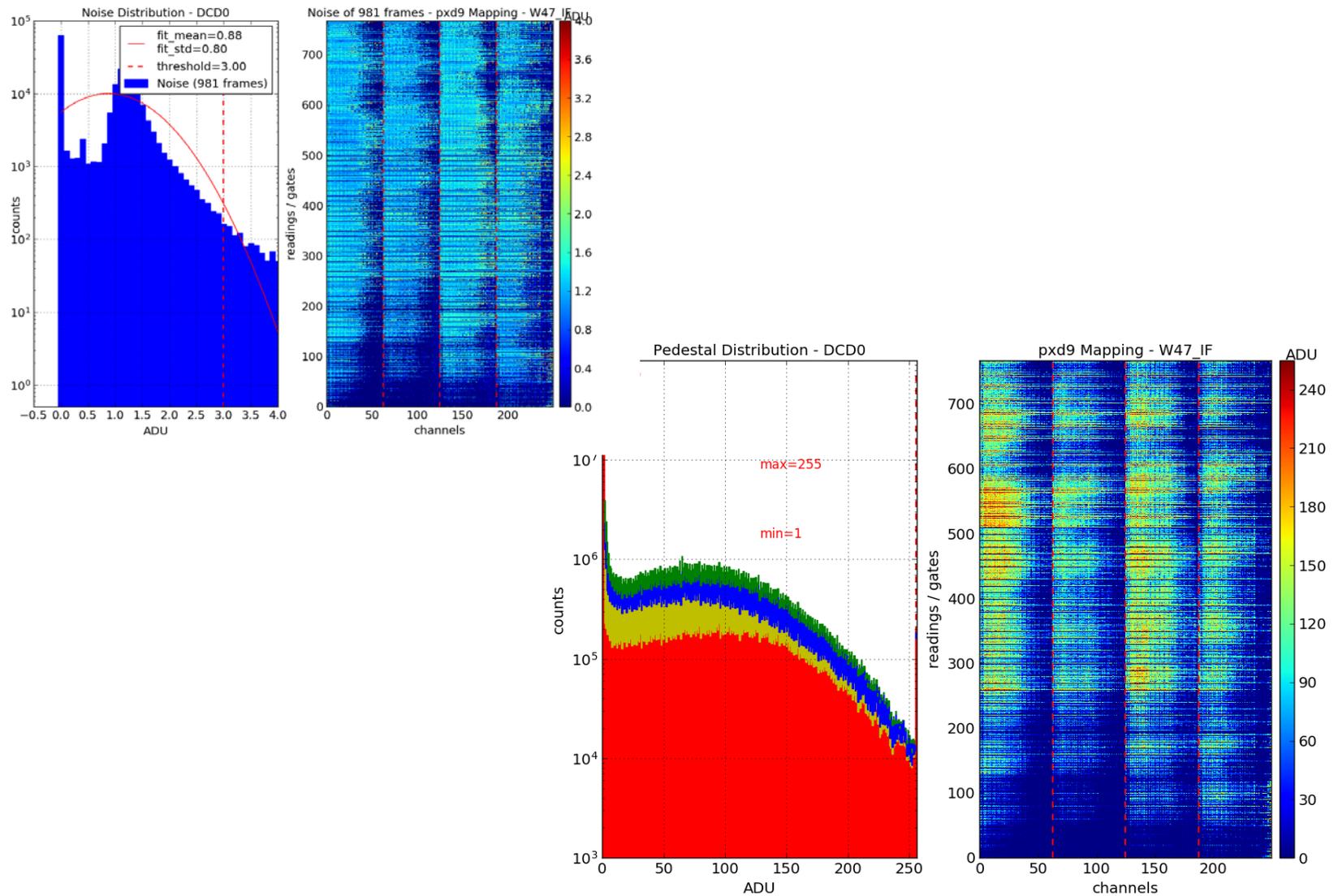
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W47_IF

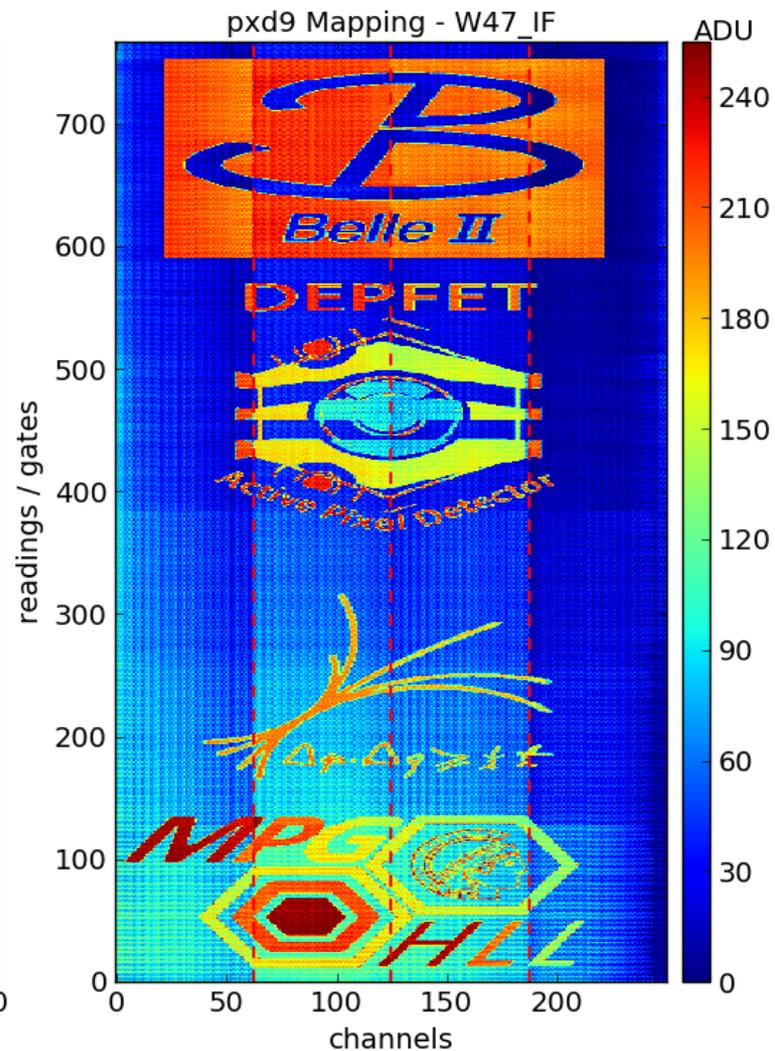
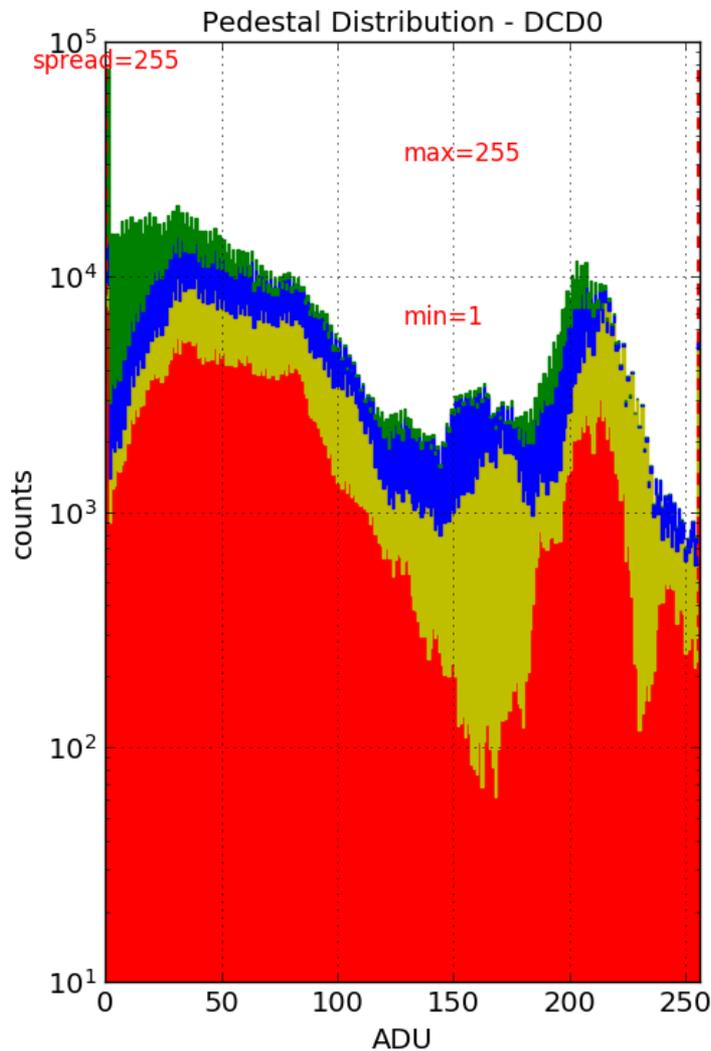


W47_IF – pedestals without offsets, without ACMC



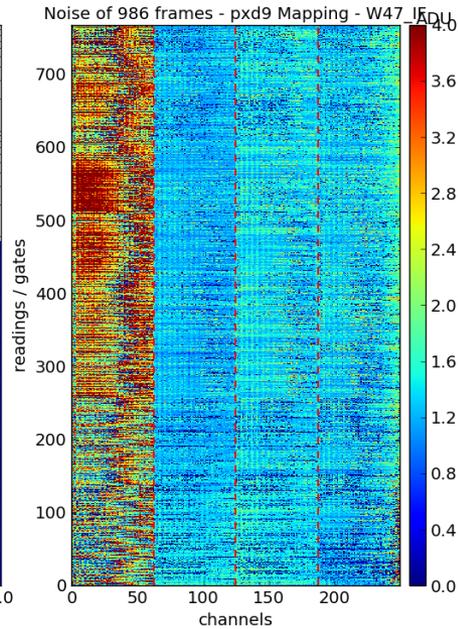
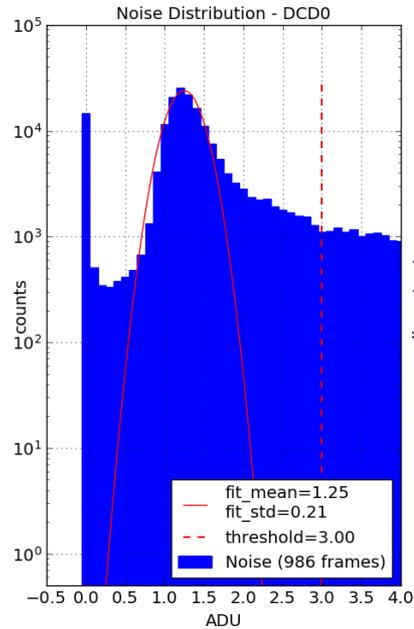


W47_IF – offset delays

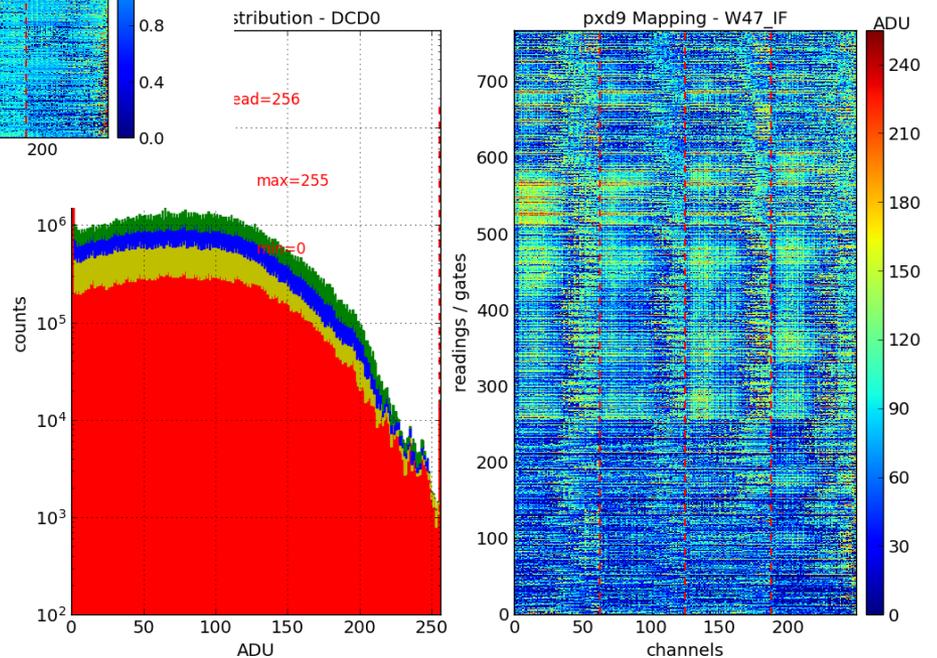




W47_IF – pedestals with offsets, without ACMC

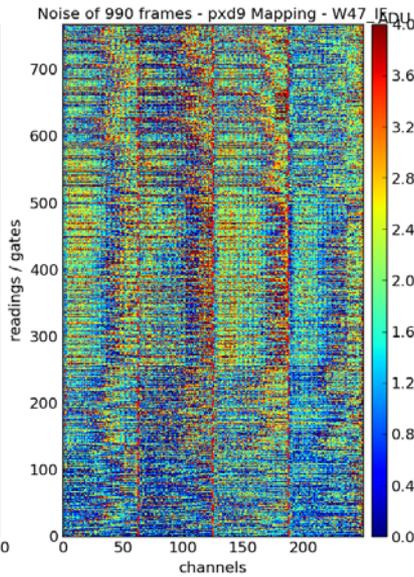
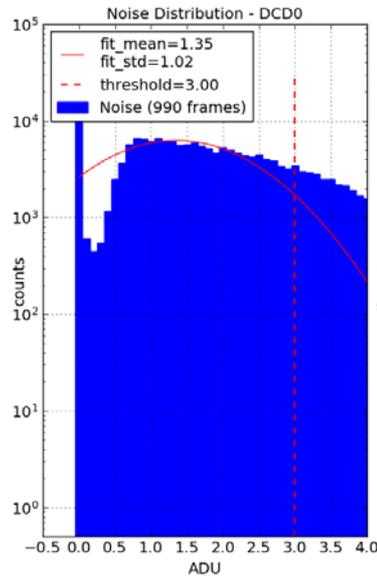


high noise on DCD1

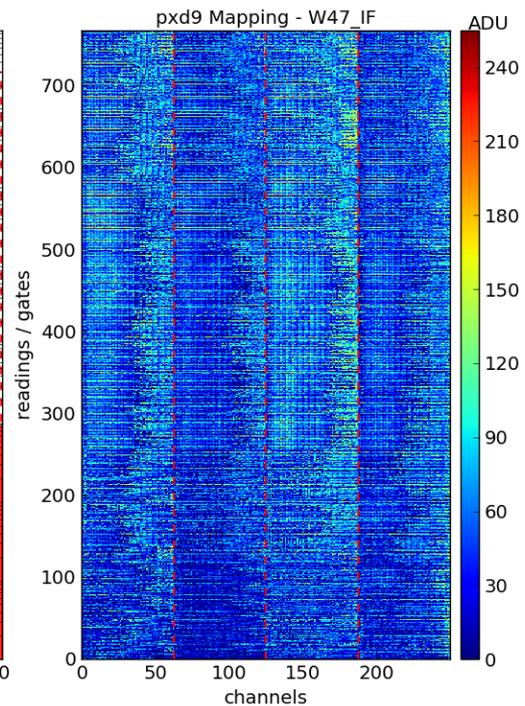
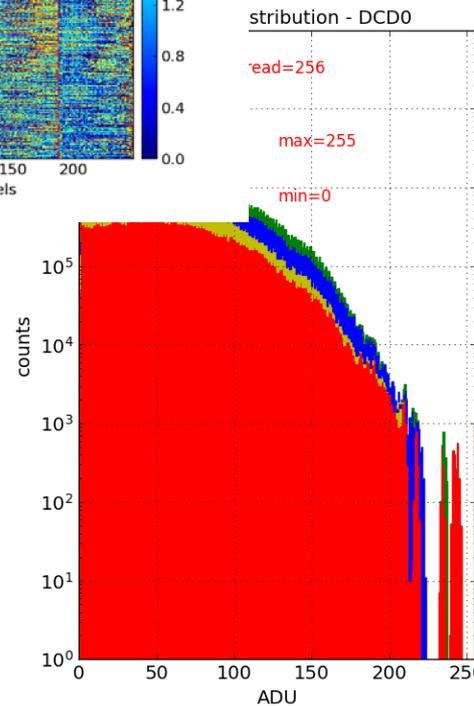




W47_IF – pedestals with offsets, with ACMC



high noise

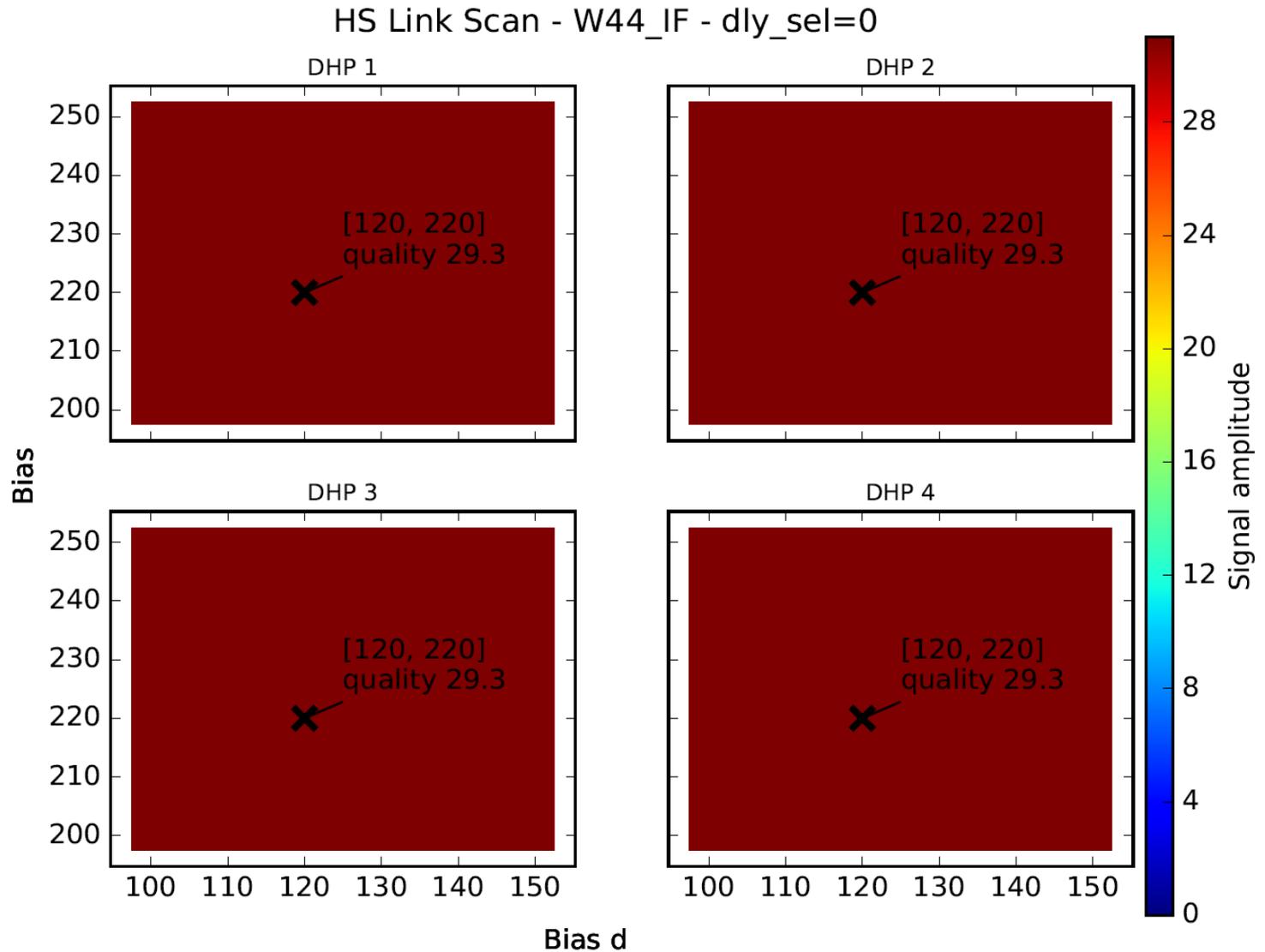




W44_IF

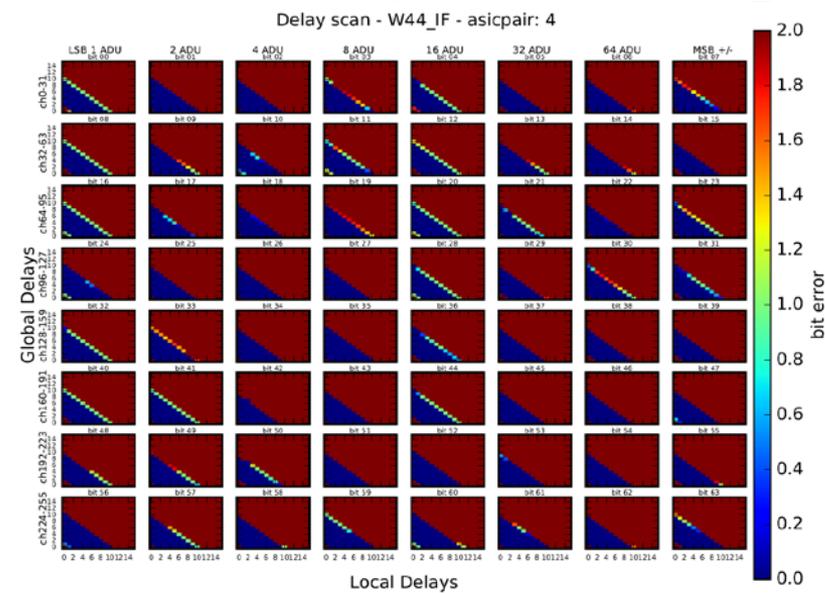
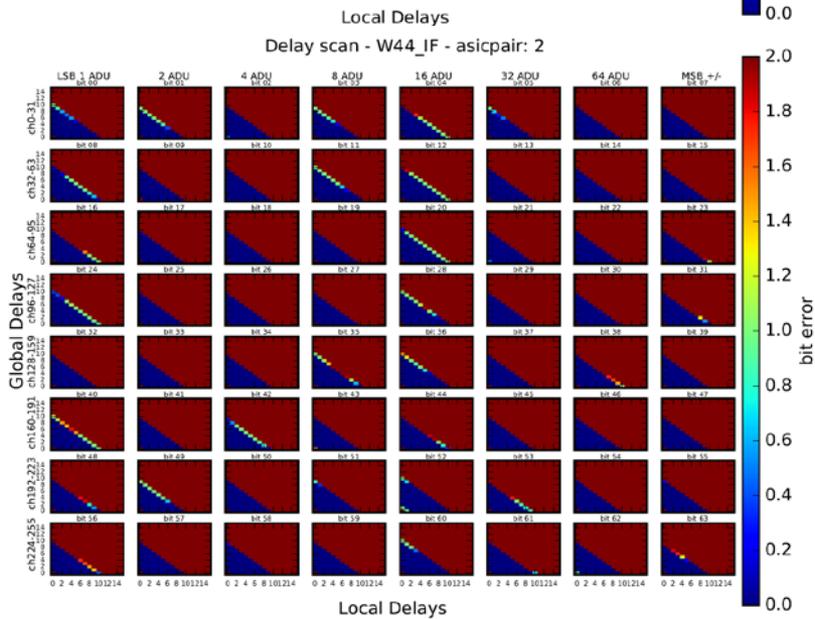
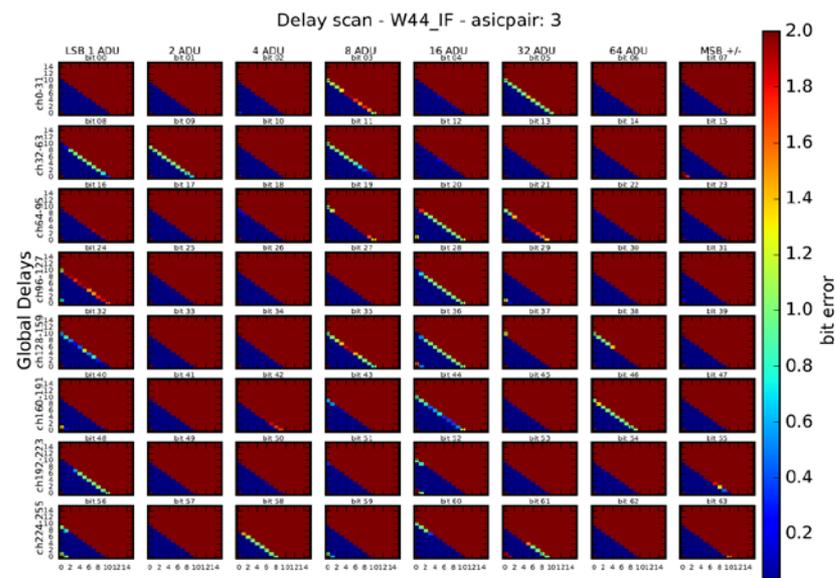
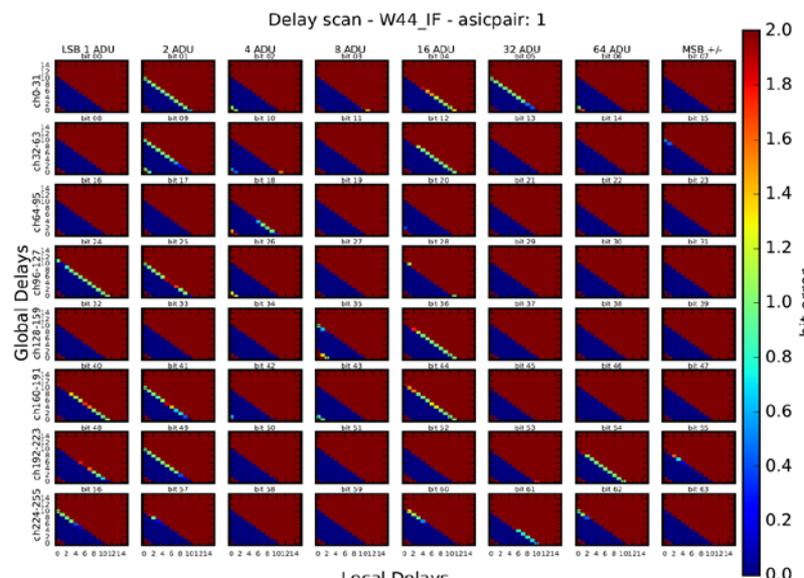


W44_IF – HS links



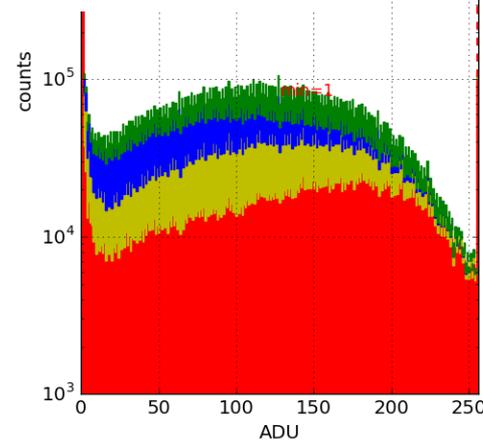
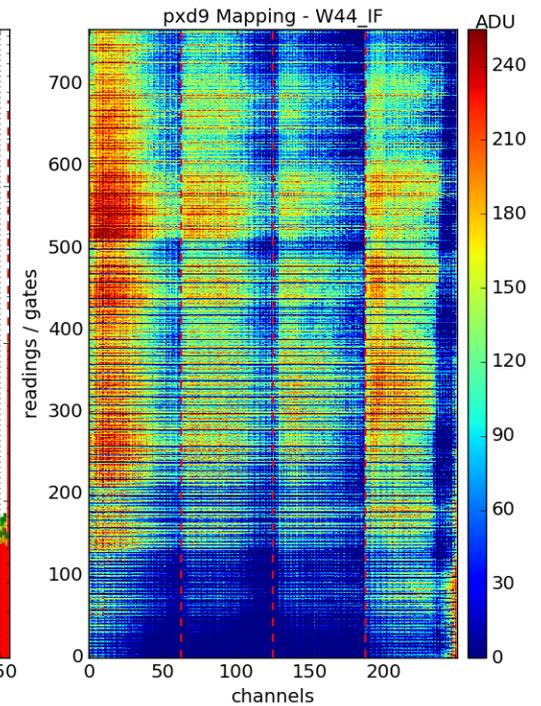
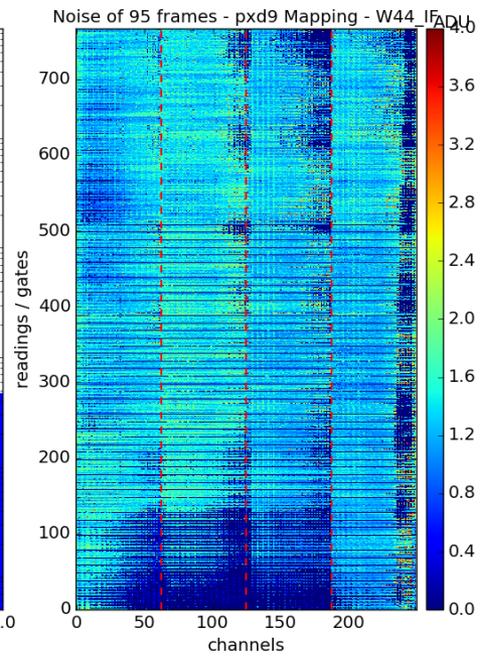
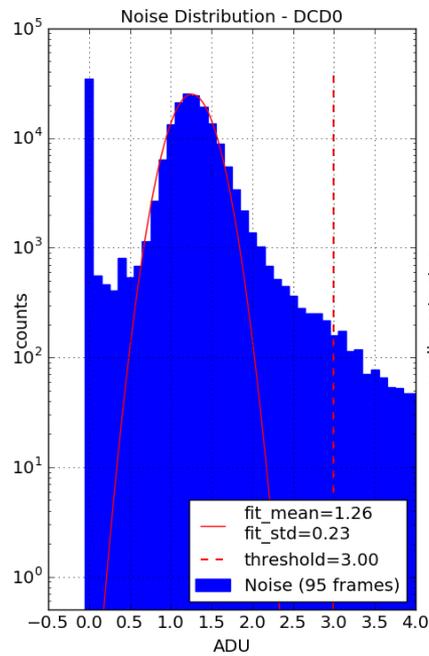


W44_IF – delays



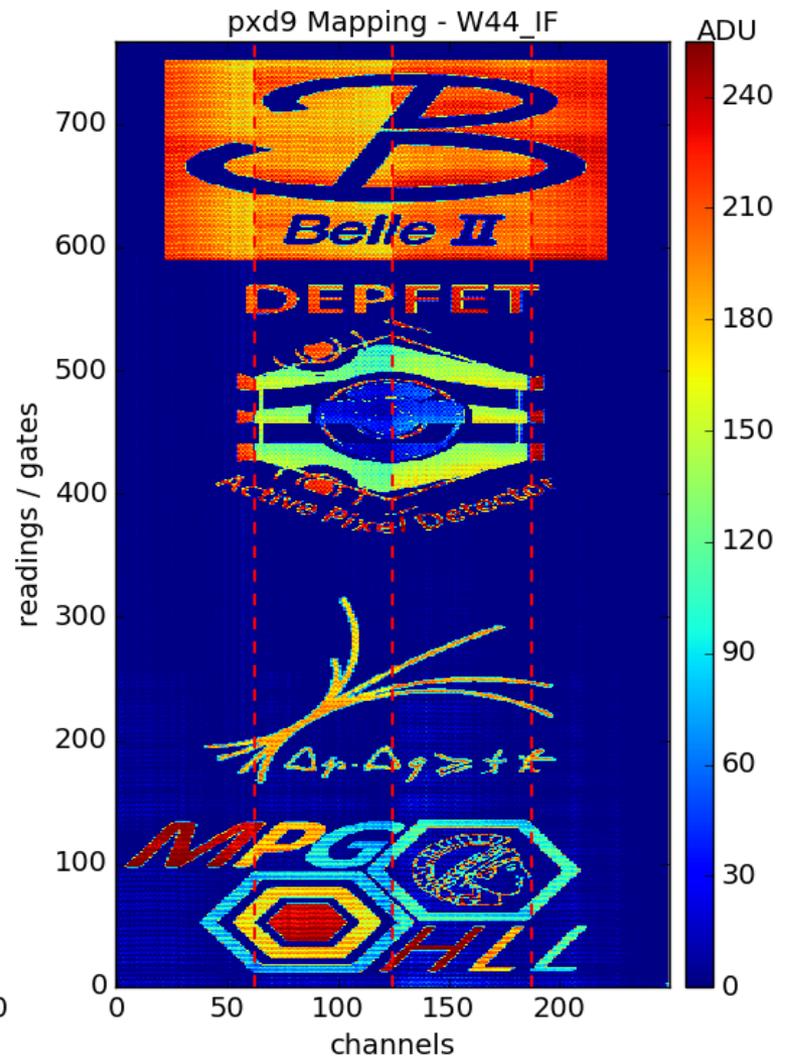
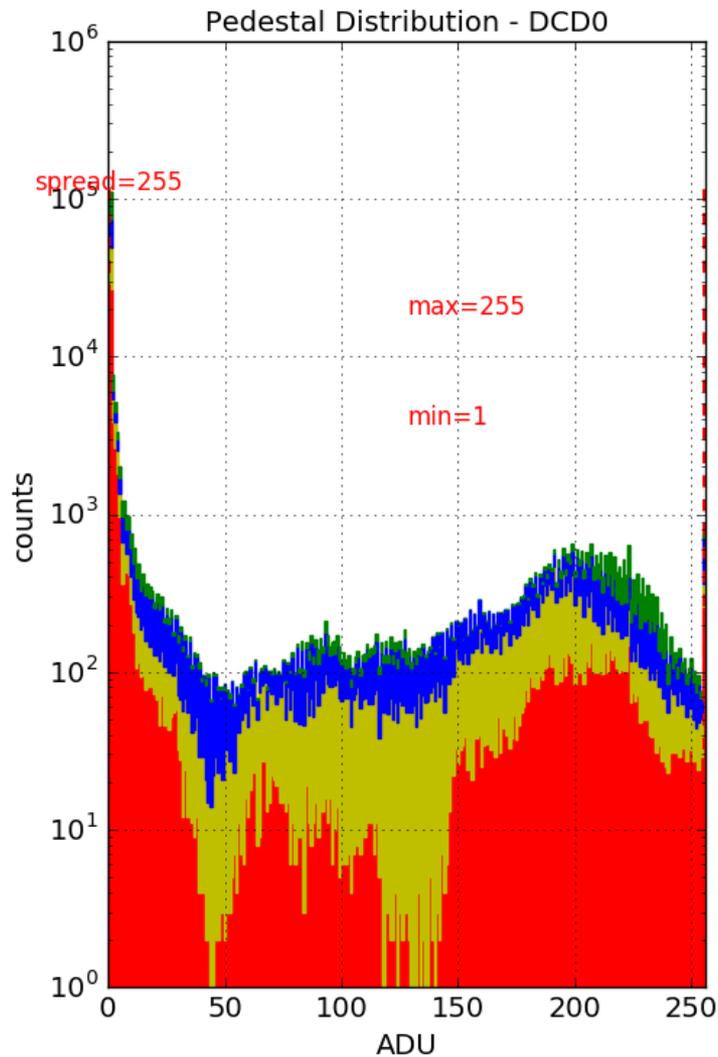


W44_IF – pedestals without offsets, without ACMC





W44_IF – offset delays





W44_IF – pedestals with offsets, without ACMC

to do



W44_IF – pedestals with offsets, with ACMC

to do



Backup



Module checks before glueing - **Issues**

- **DHPT high speed (HS) Links**

short scan (to have a reference for later) ✓

- bias 200 to 250, step 5
- bias_d 100 to 150, step 5
- delay 0

- **Delays** ✓

problem with crowded root partition during analysis. Problem still remains

- **ADCs optimization using small parameter space**

- **Pedestal/noise (1k frames)** not defined what to analyse – compare etc?

- **Sampling Point Curve** – missing: verification of the Switcher sequence in DHP memory

- **2-bit offset (delay and current source optimization)** coding guidelines missing but working

- **Pedestal/noise (1k frames)** - same as above

- **DCD analog common mode correction (ACMC)** ✓

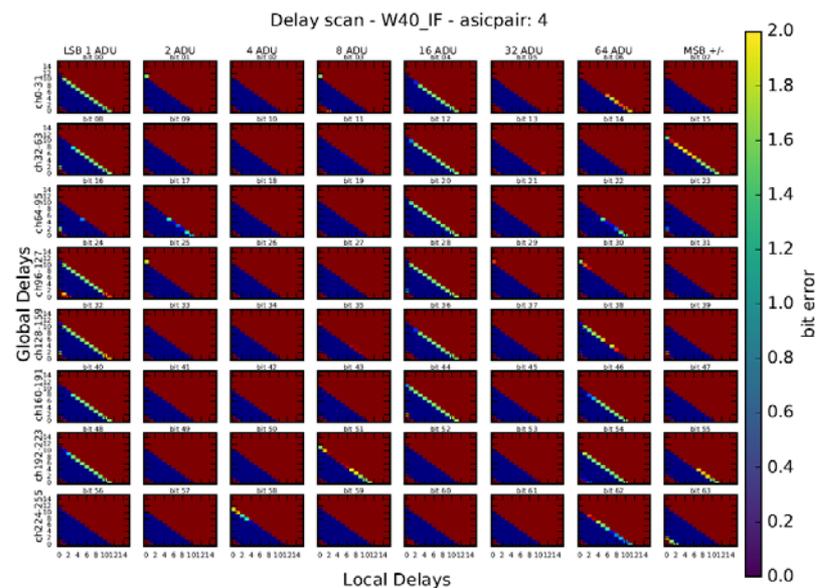
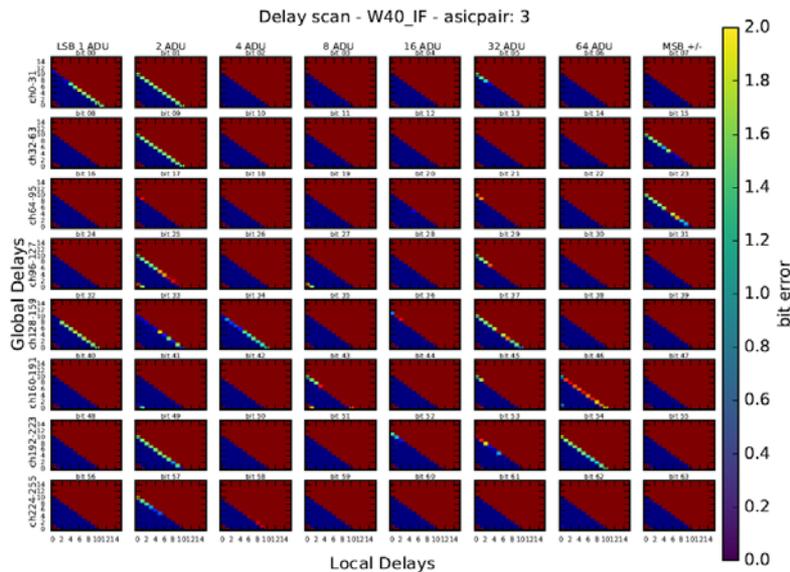
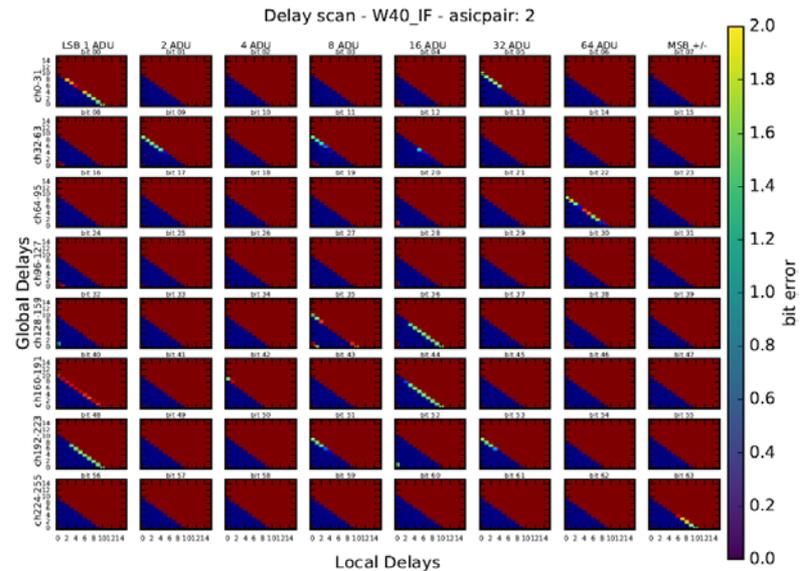
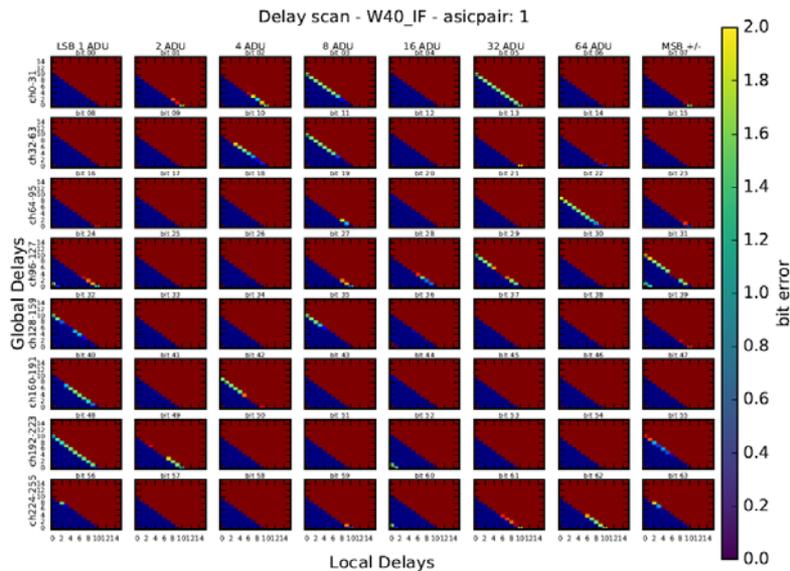
- **Pedestal/noise (1k frames)** - same as above

- **Source measurement different regions** – working but extremely slow (is the stepper implemented)

- Threshold 5
- Verify shape of the spectra
- SNR in different regions
- Adjust VNSubIn / Use ACMC



W40_IF – delays





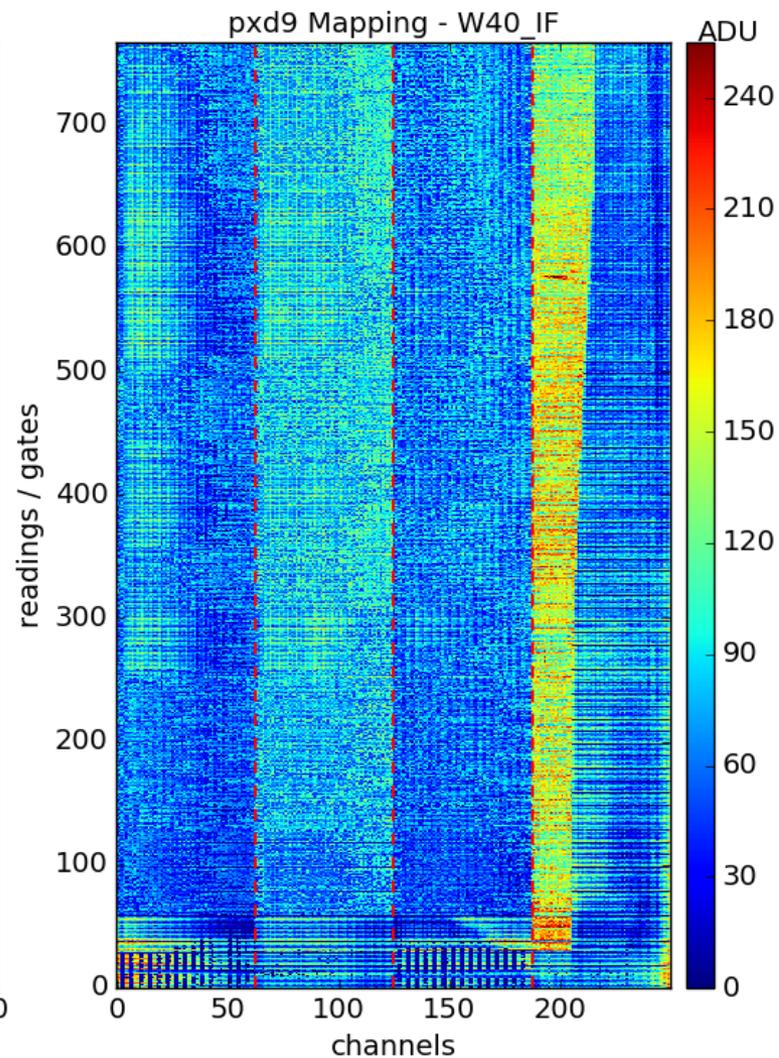
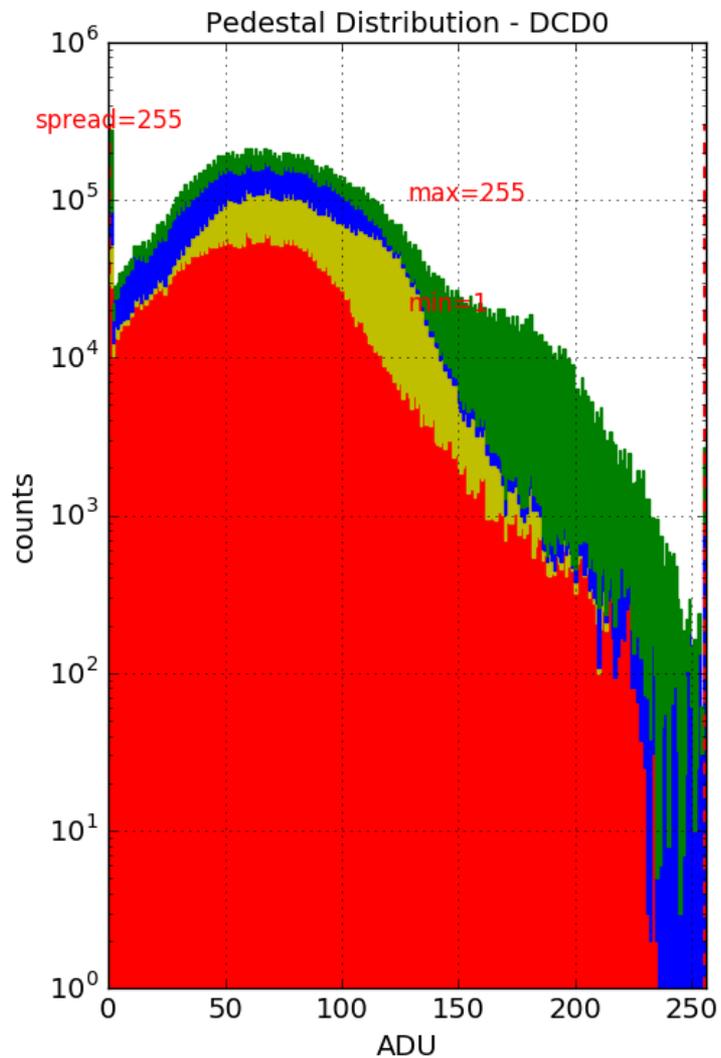
W40_IF – ADC curves

Measurements done, analysis missing

Problem with analysis

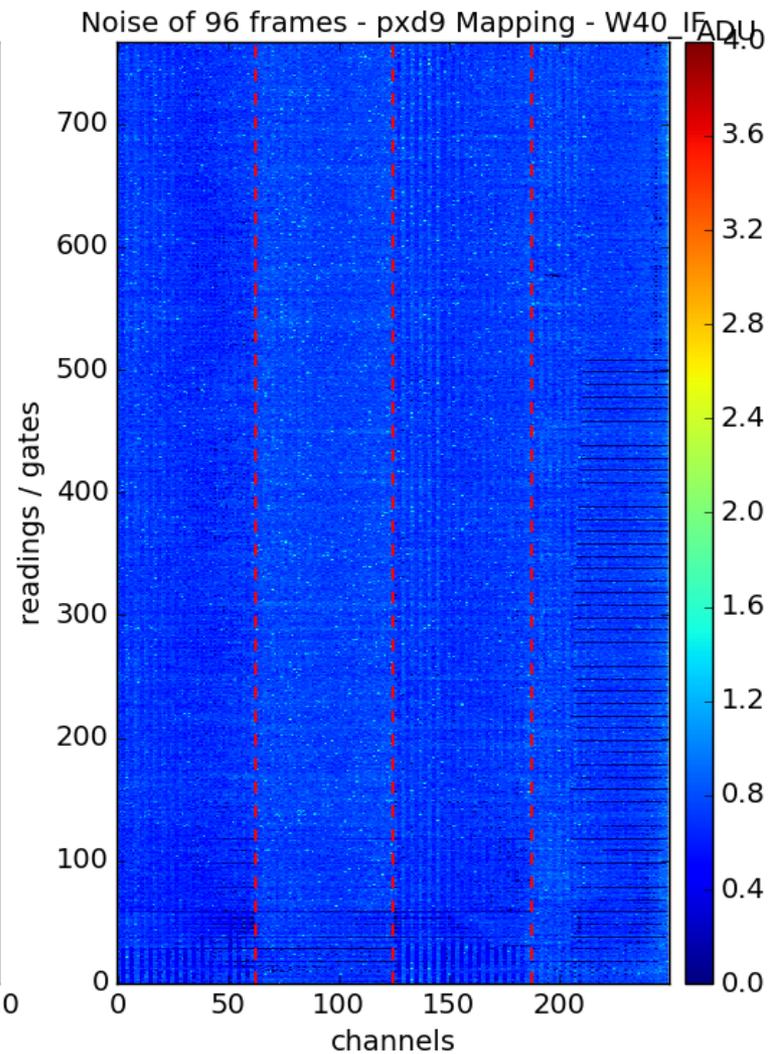
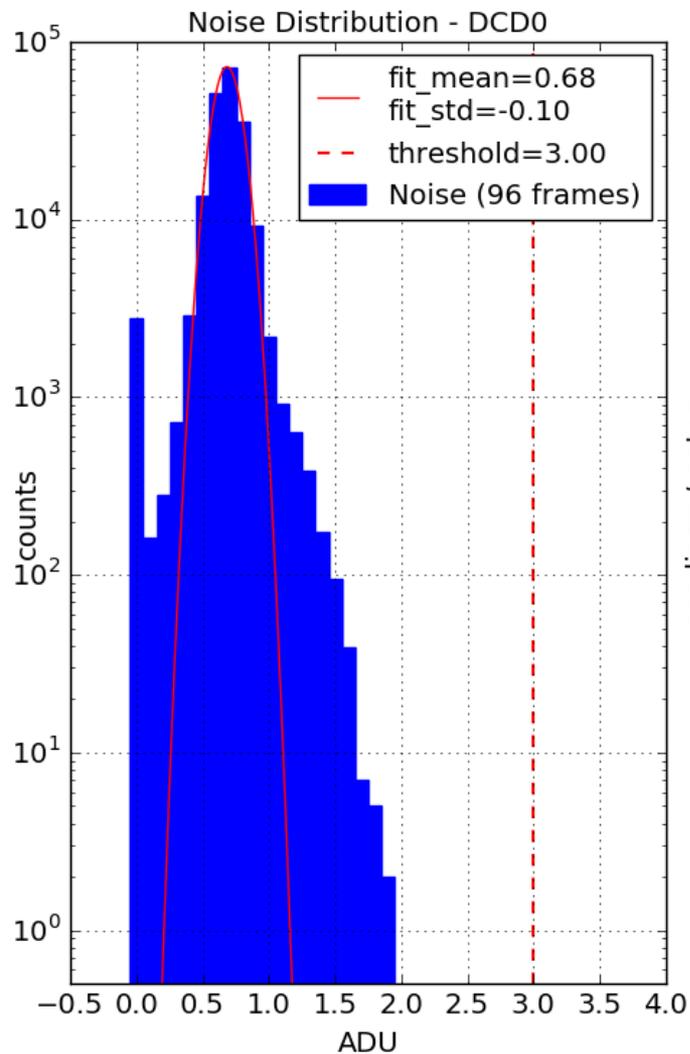


W40_IF – pedestals – with Offsets and ACMC





W40_IF – noise – with Offsets and ACMC





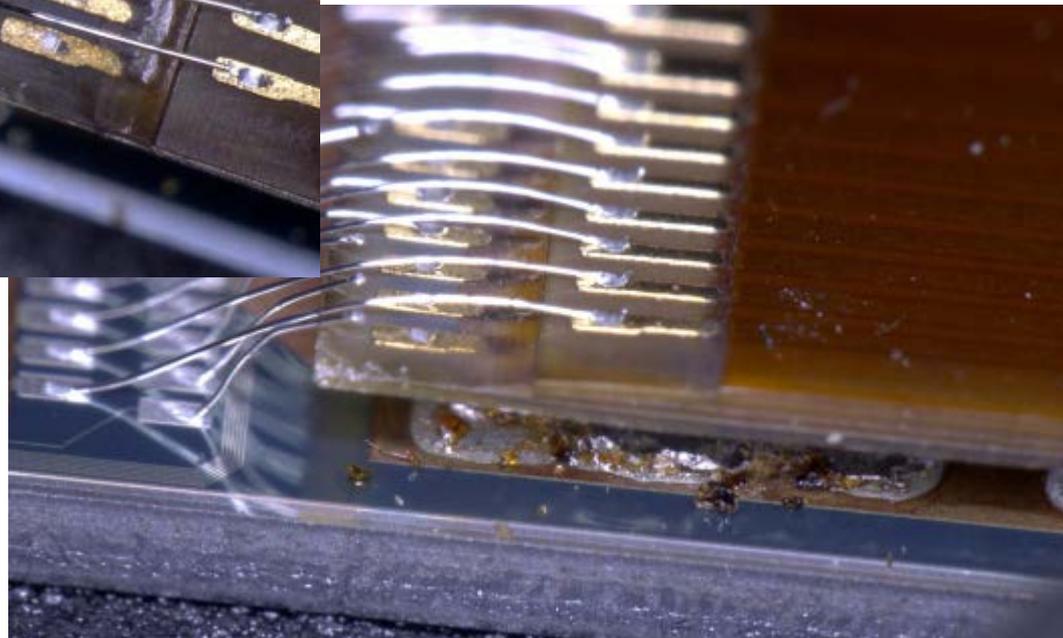
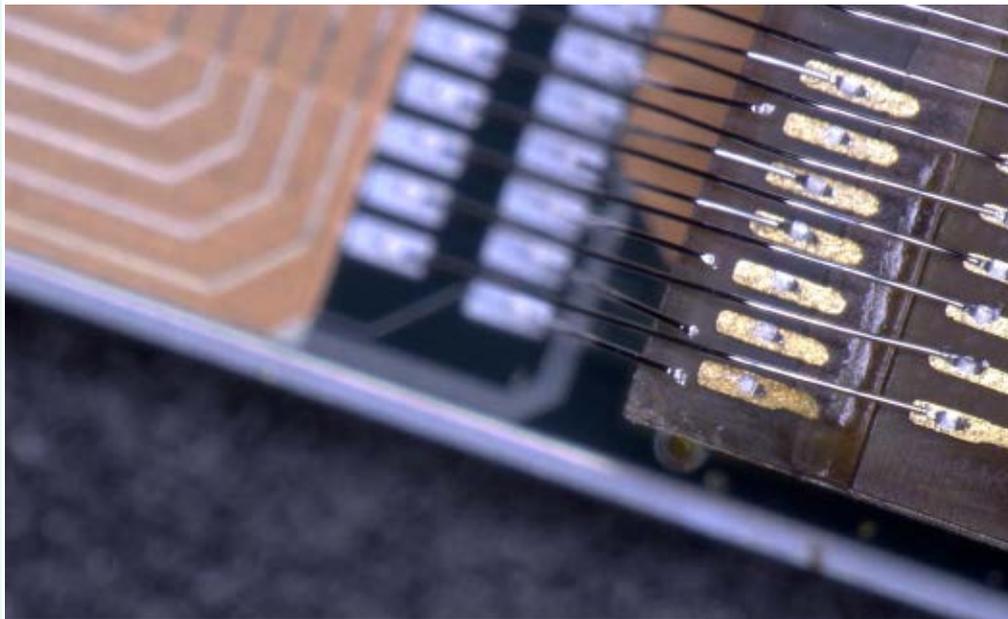
W40_OF – source measurements

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Name
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run002_nosource
run003_nosource_dcmc_threshold5_ped25_cm20
run004_nosource_no-dcmc_threshold5
run005_source_threshold5_hv60_drift4
run006_source_threshold5_hv60_drift5
run007_source_threshold5_hv60_drift6
run008_source_threshold5_hv64_drift4
run009_source_threshold5_hv64_drift5
run010_source_threshold5_hv64_drift6
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run016_source_threshold5_hv72_drift6
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run019_source_threshold5_hv56_drift6
run020_source_threshold5_hv56_drift6_pos1
run021_source_threshold5_hv56_drift6_pos0
run022_source_threshold5_hv56_drift6_pos3
run023_source_threshold5_hv56_drift6_pos4
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run025_source_threshold5_hv64_drift4_painting



W38_IB & W40_IF - ladder

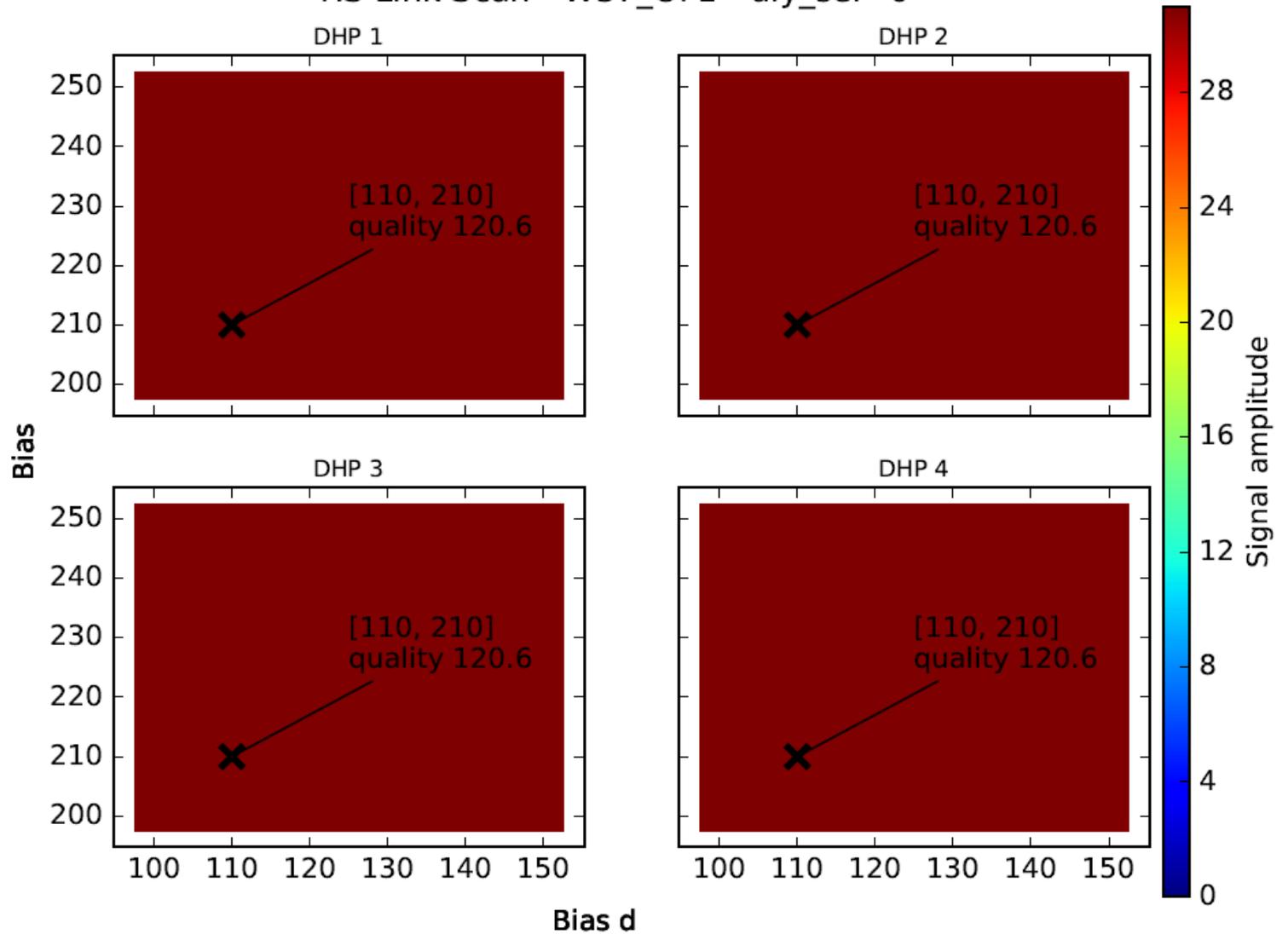


15 mA	30 mA	-4000 mV	3000 mV	3000 mV	■	3050 mV	3009 mV	5 mA	gate-on2
15 mA	30 mA	-4000 mV	3000 mV	3000 mV	■	810 mV	733 mV	16 mA	gate-on3
30 mA	30 mA	0 mV	3000 mV	6000 mV	■	3056 mV	3023 mV	10 mA	gate-off
120 mA	150 mA	0 mV	6000 mV	7000 mV	■	7238 mV	6002 mV	24 mA	source



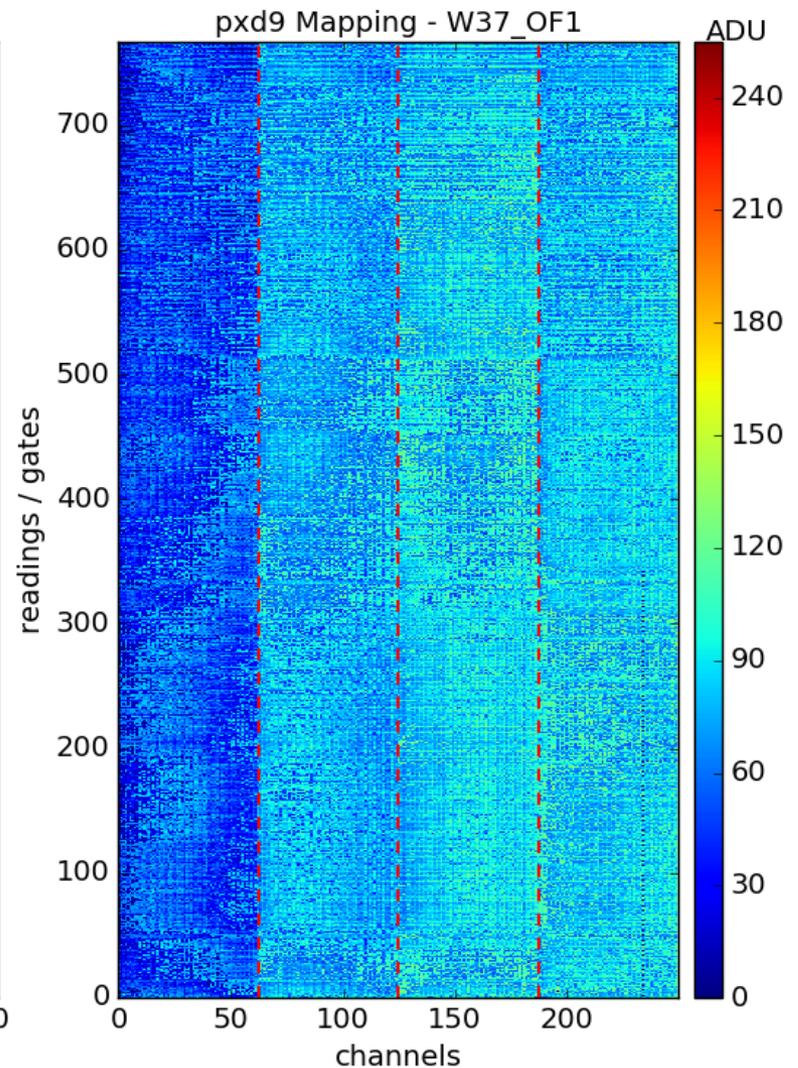
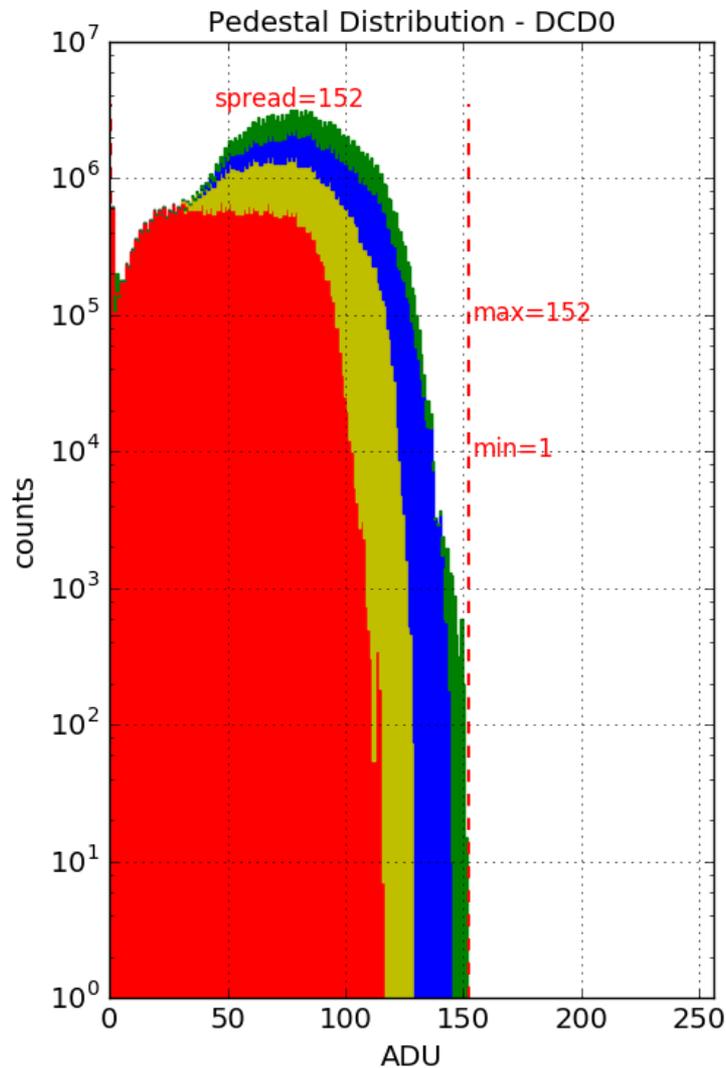
W37_OF1 – HS links

HS Link Scan - W37_OF1 - dly_sel=0



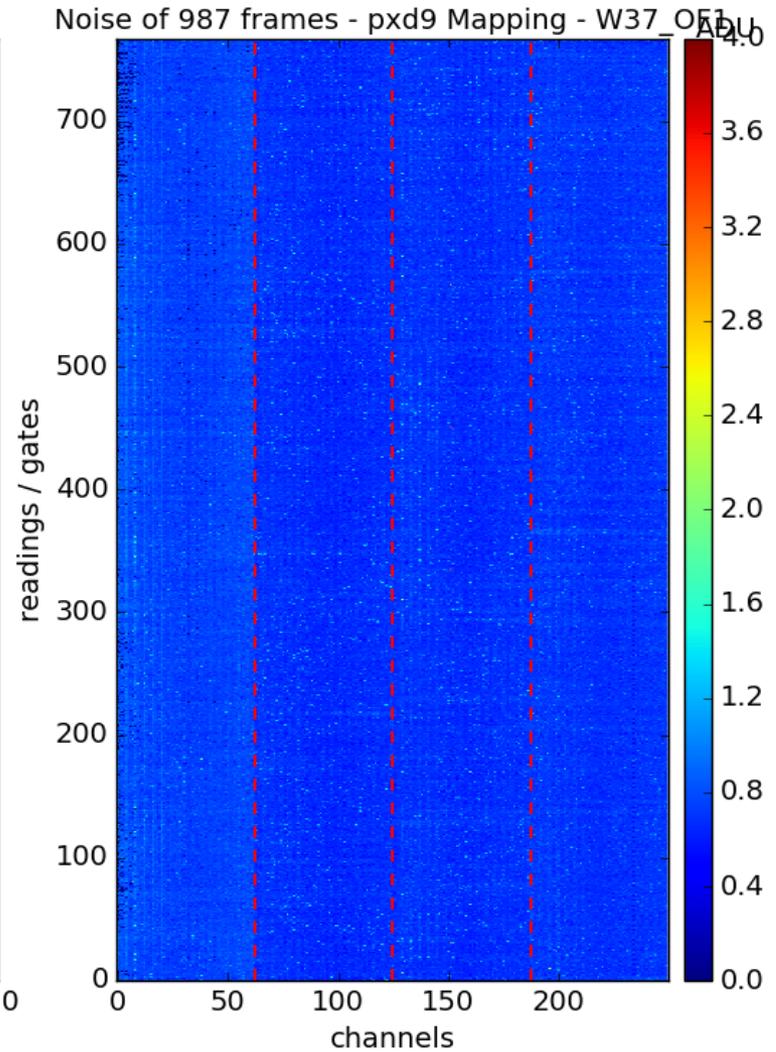
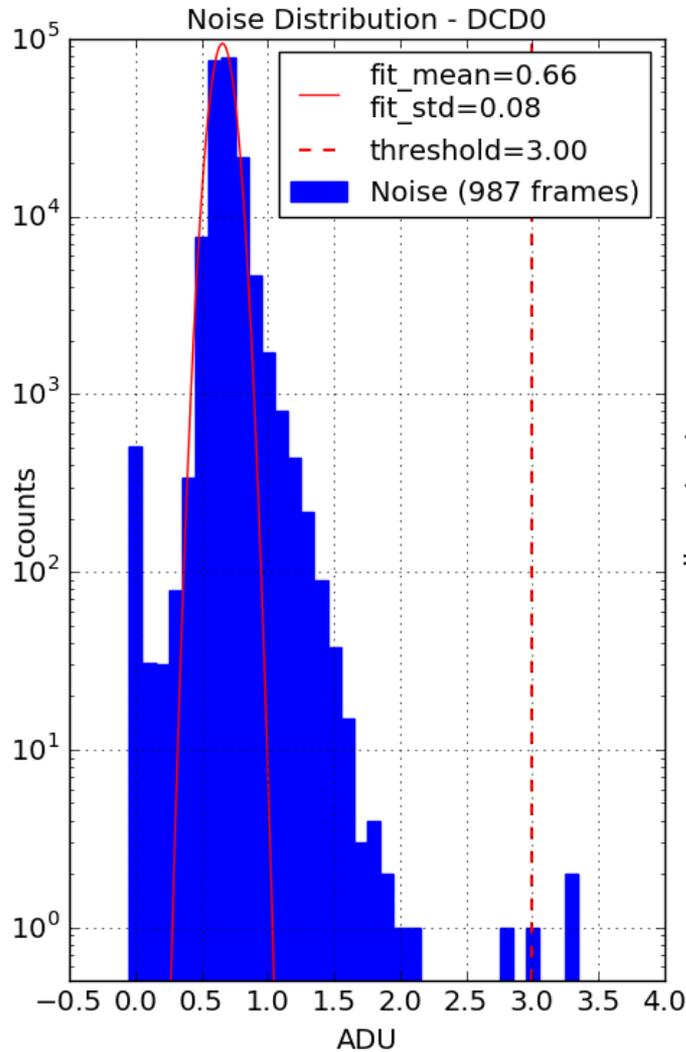


W37_OF1 – pedestals with ACMC and offsets



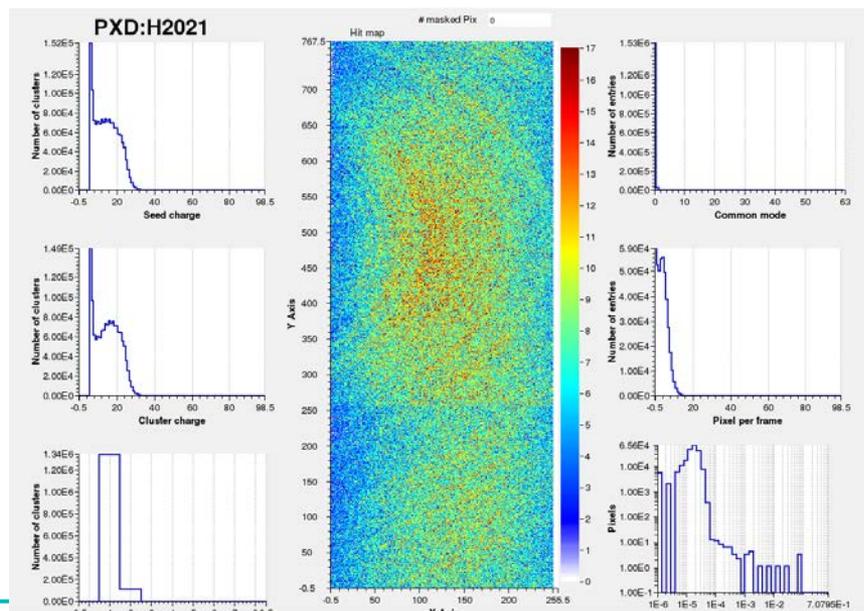
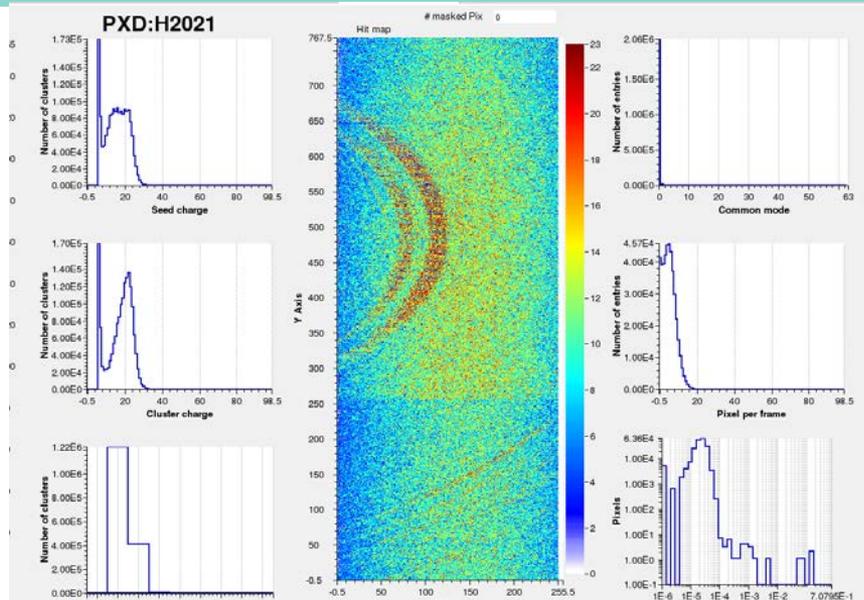


W37_OF1 – noise with ACMC and offsets





W37_OF1 – source measurements



/pdxtest8/W37_OF1/source/2017_08_10_003

Name

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- drift_-3000_hv_-62000
- drift_-3000_hv_-64000
- drift_-3000_hv_-66000
- drift_-3000_hv_-68000
- drift_-3000_hv_-70000
- drift_-3000_hv_-72000
- drift_-3000_hv_-74000
- drift_-3000_hv_-76000
- drift_-3000_hv_-78000
- drift_-3000_hv_-80000
- drift_-4000_hv_-60000
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Name

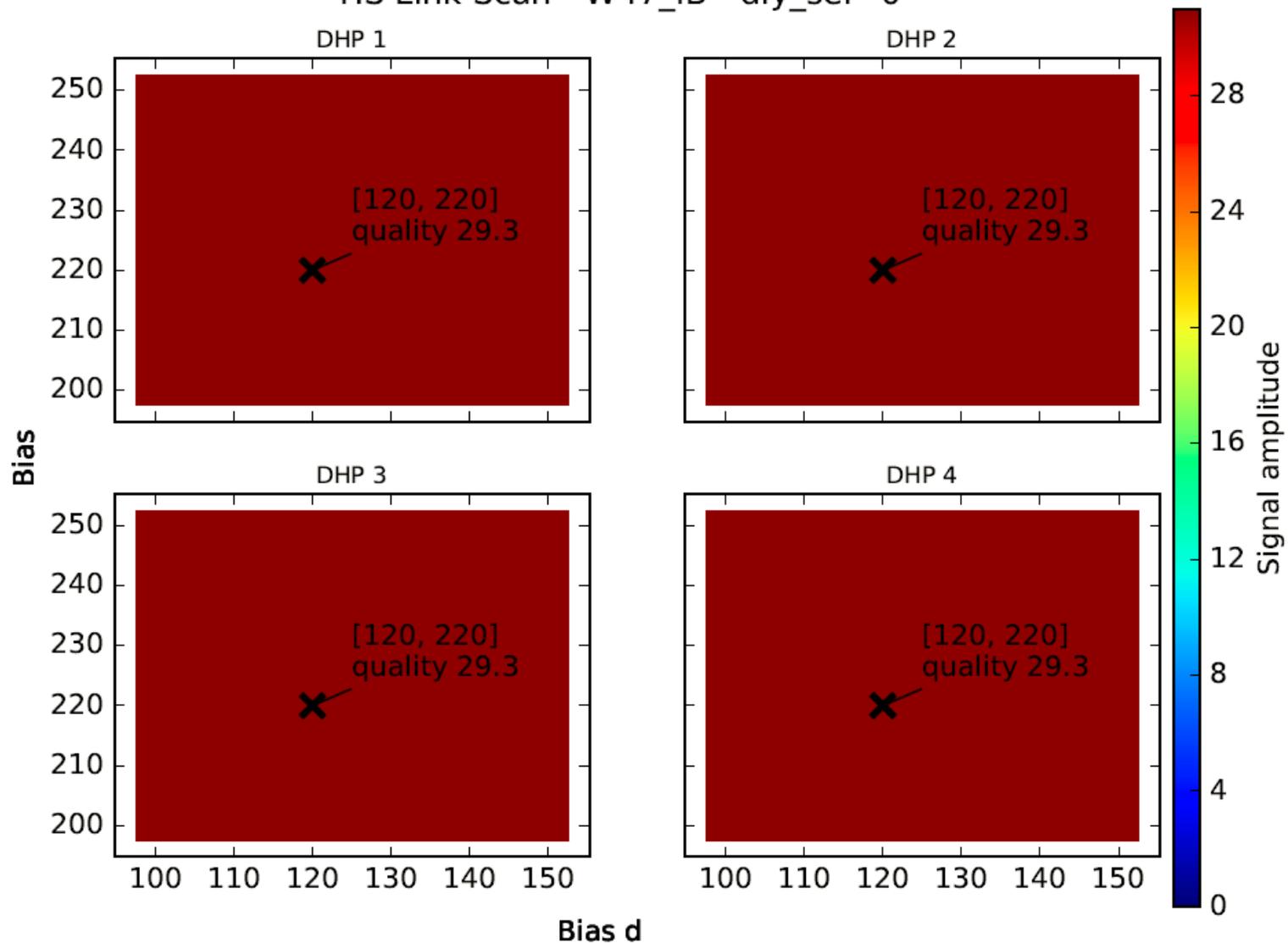
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- drift_-6000_hv_-70000
- drift_-6000_hv_-72000
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see talk by Harrison



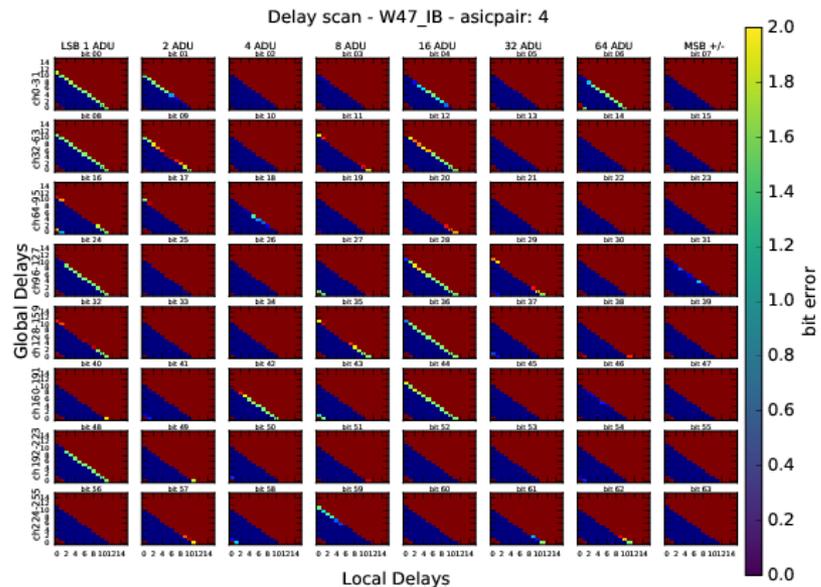
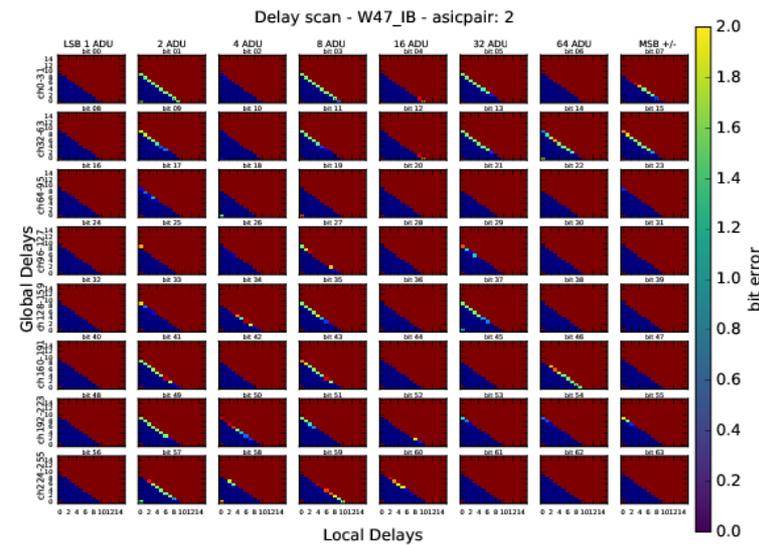
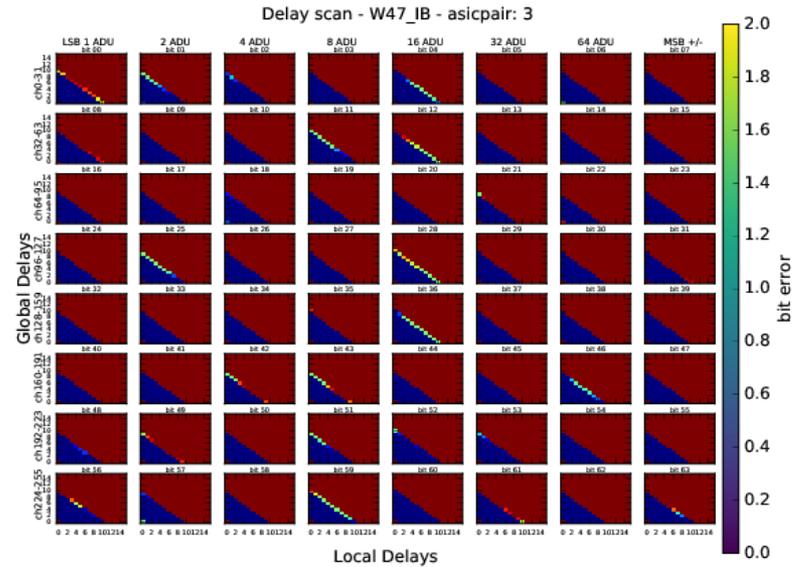
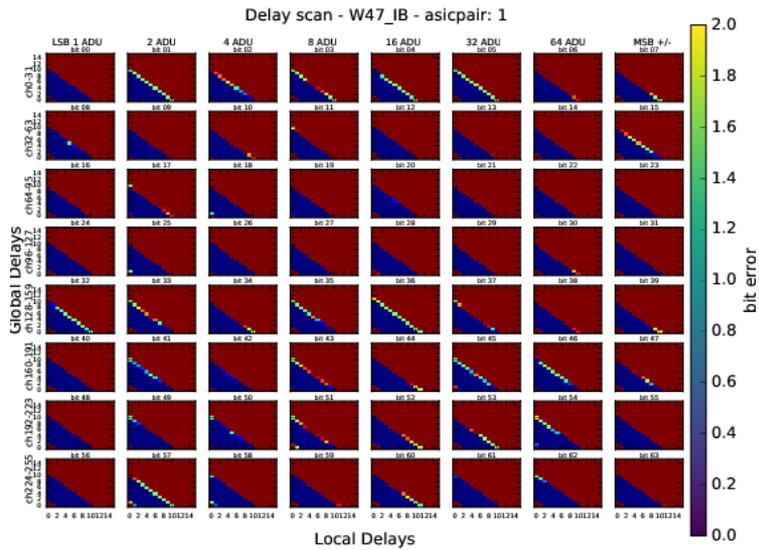
W47_IB – HS link

HS Link Scan - W47_IB - dly_sel=0



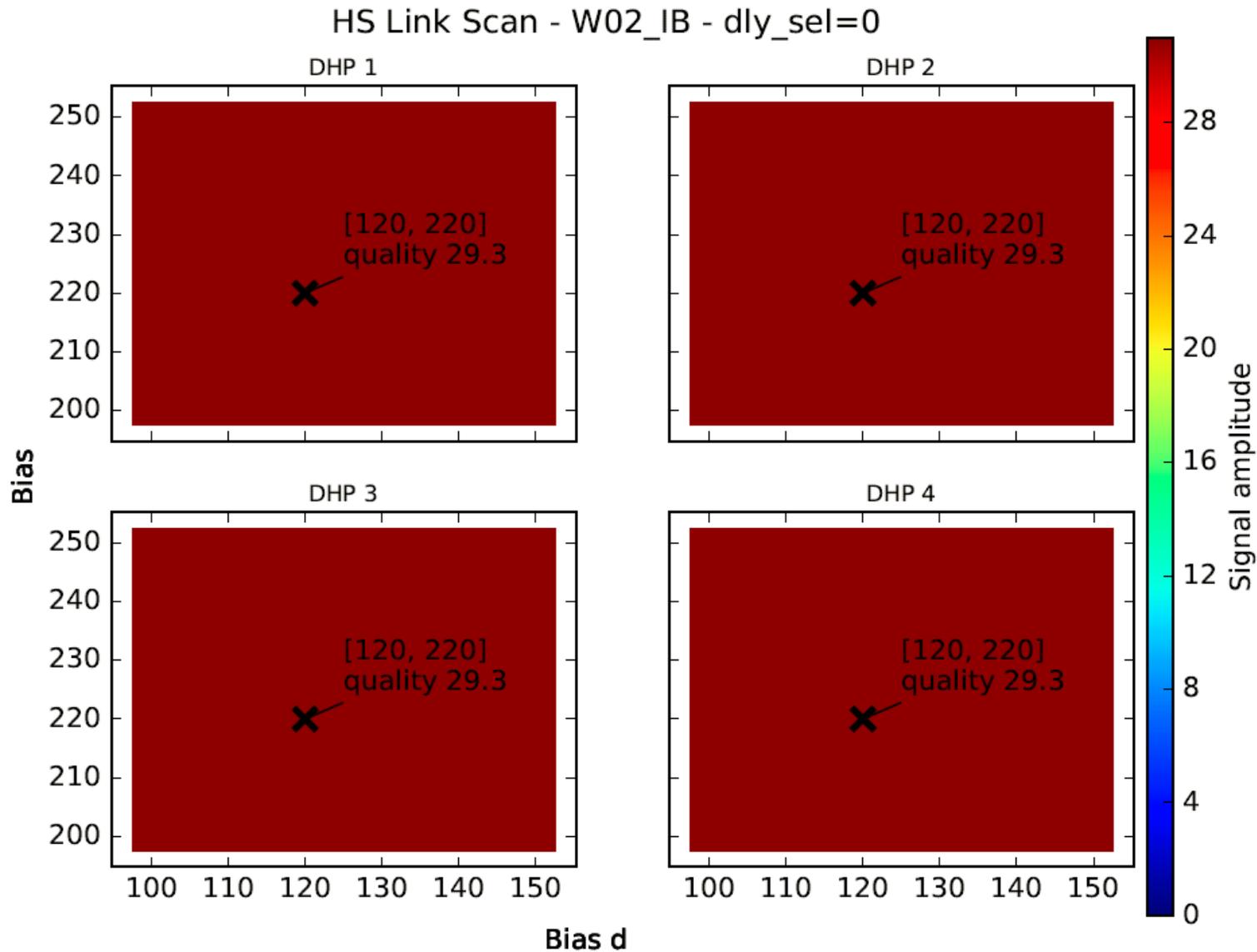


W47_IB – delays





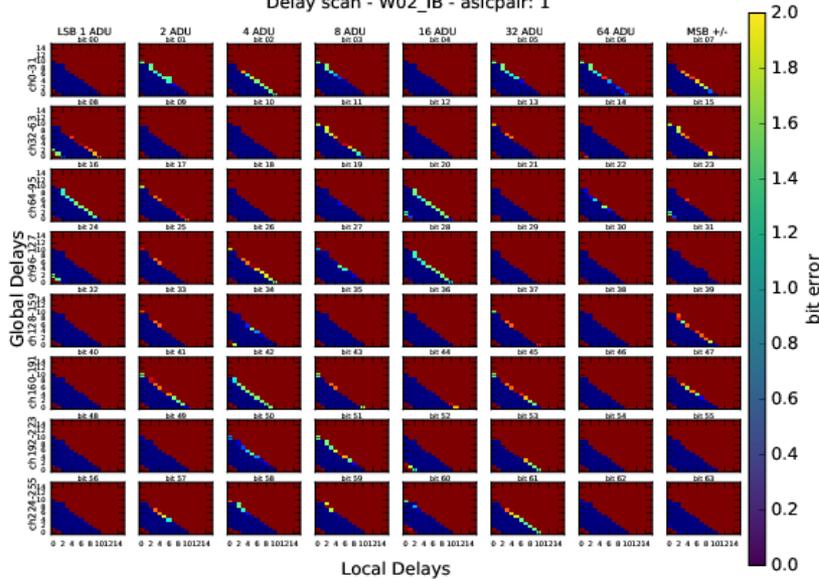
W02_IB – HS link



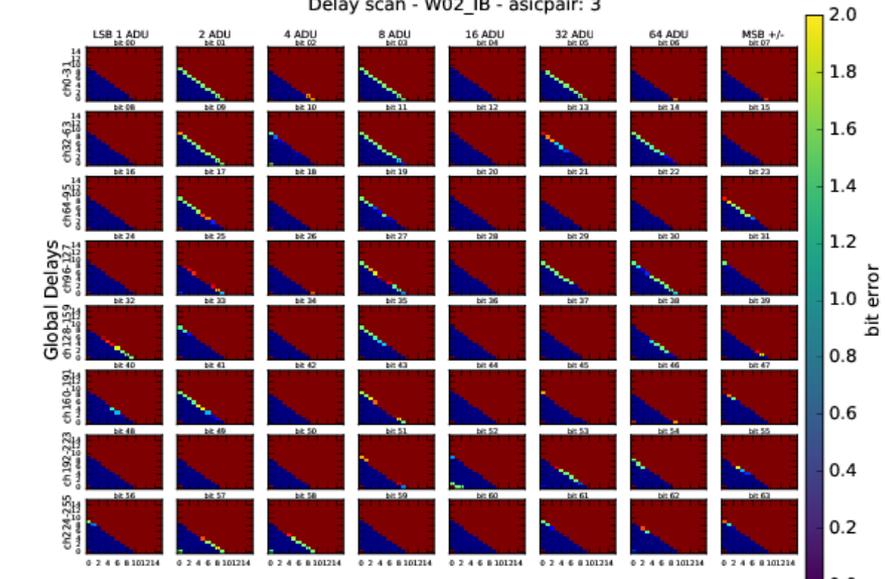


W02_IB – delays

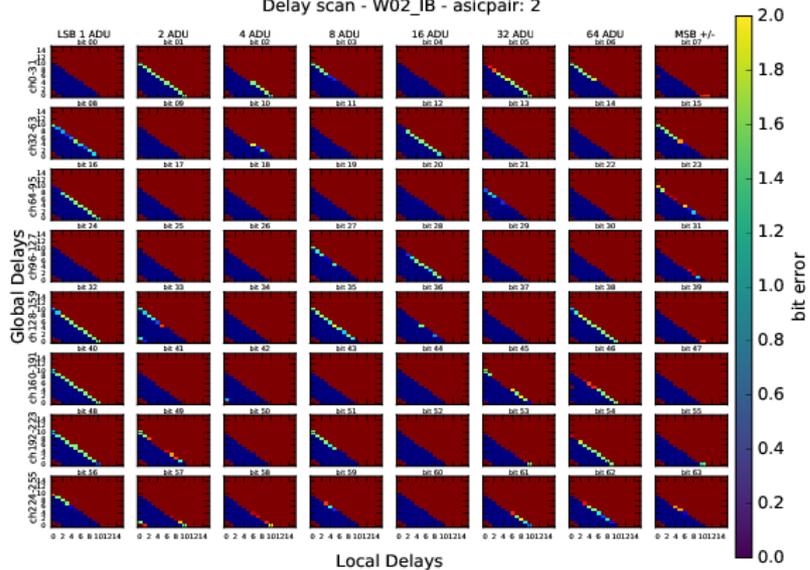
Delay scan - W02_IB - asicpair: 1



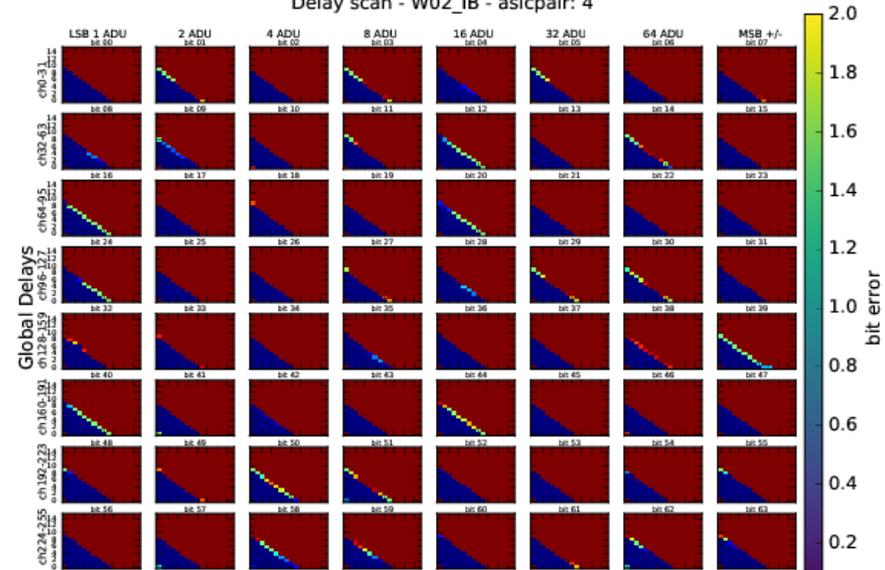
Delay scan - W02_IB - asicpair: 3



Delay scan - W02_IB - asicpair: 2



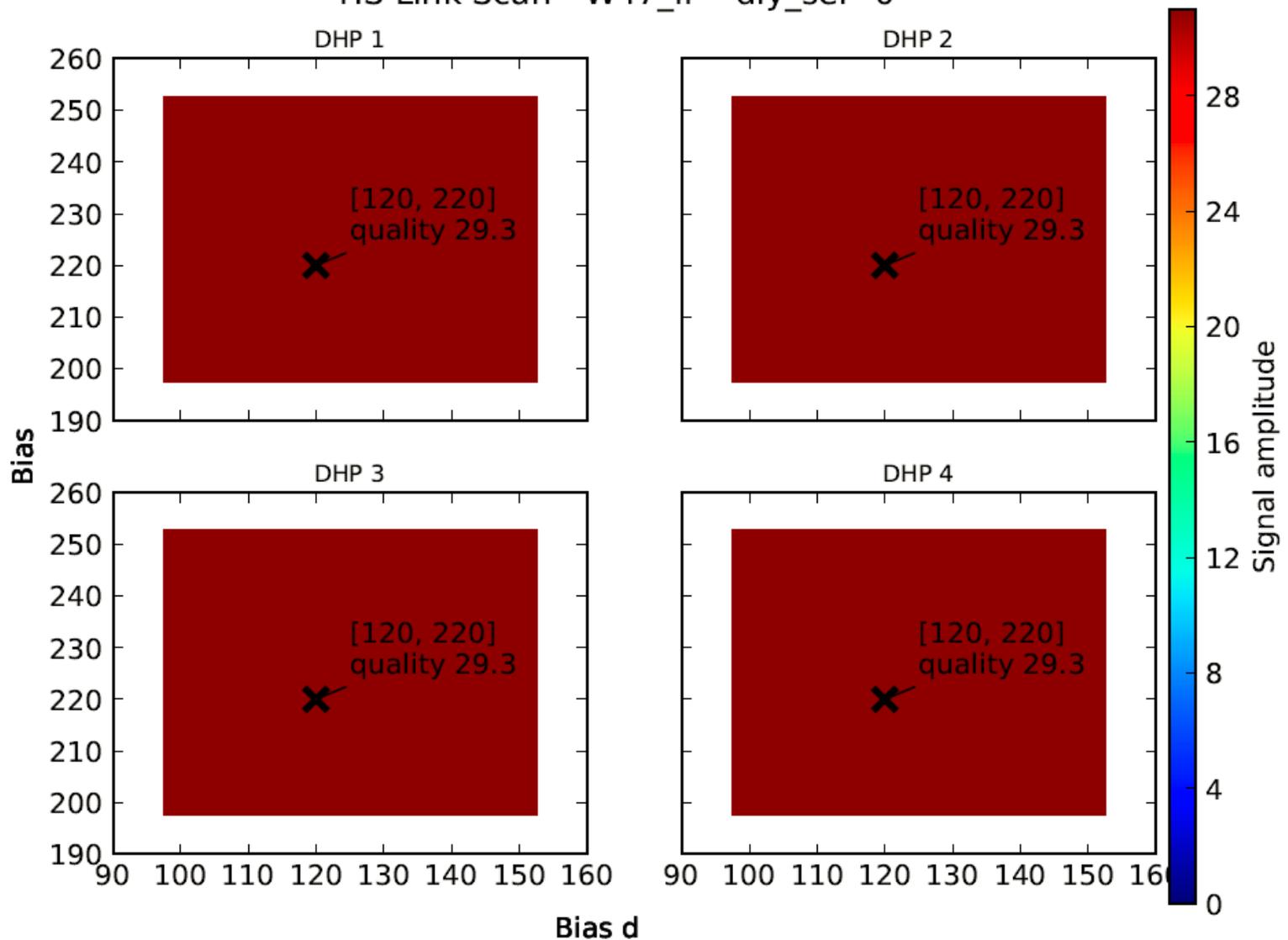
Delay scan - W02_IB - asicpair: 4





W47_IF – HS link

HS Link Scan - W47_IF - dly_sel=0





W47_IF – delays

