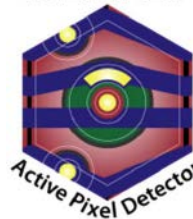




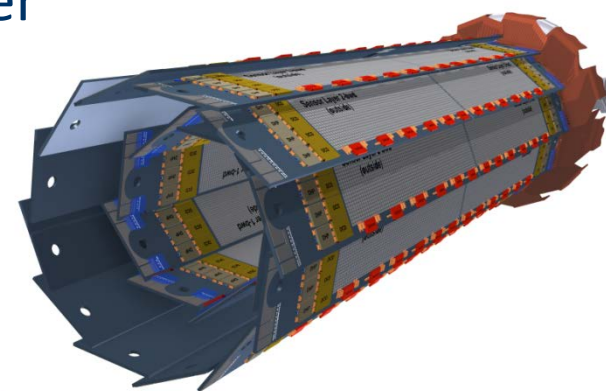
DEPFET



# Power down sequence meeting

Philipp Leitl, Felix Müller

Jan 9<sup>th</sup>, 2018

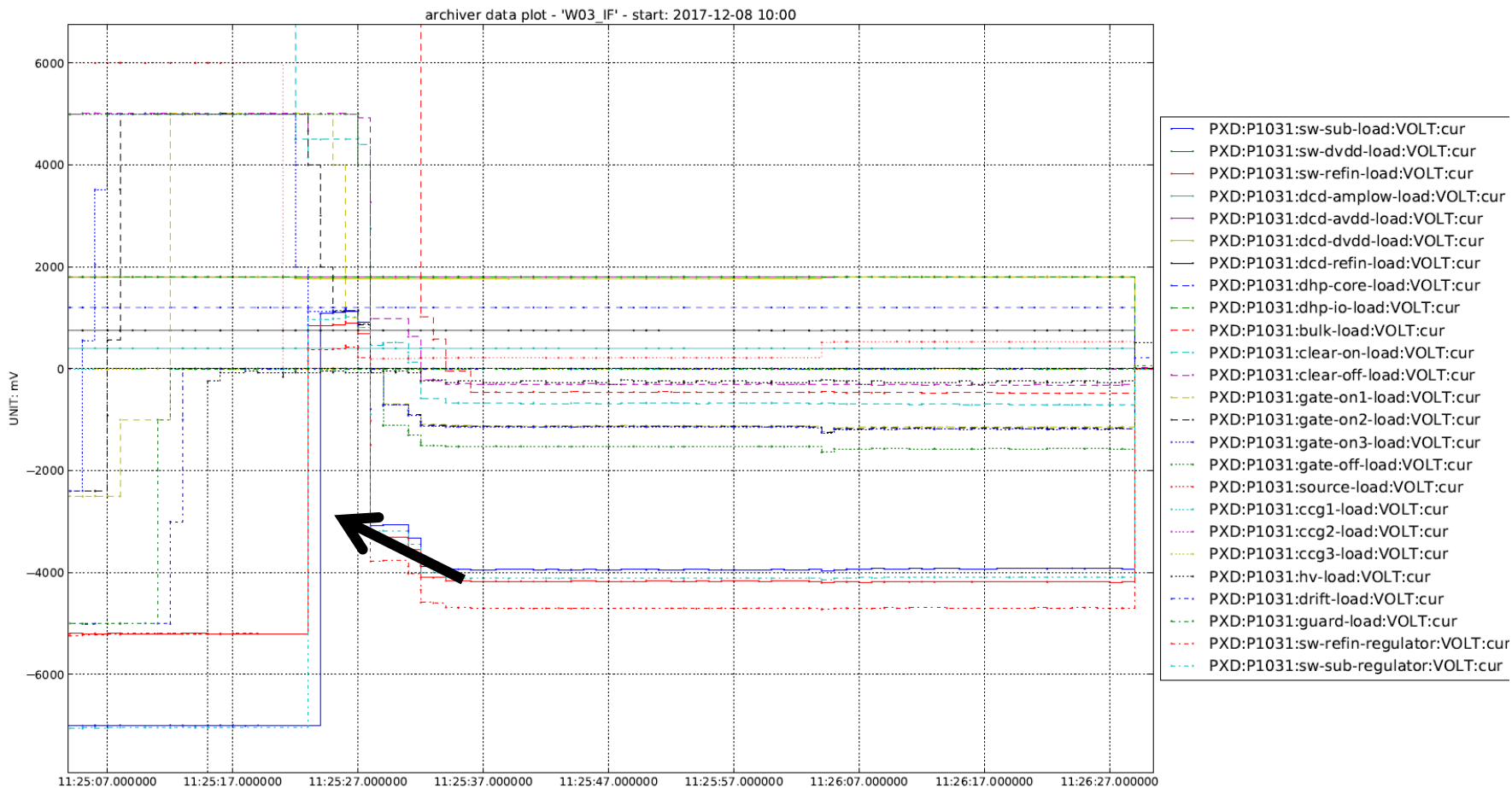




# What happened?

During the power down sequence the current limits of sw-sub and sw-refin were reached. Hence, the voltages raised from -7 V (sw-sub) and -5.2 V (sw-refin) to ~ +1 V. This partially destroyed the switchers.

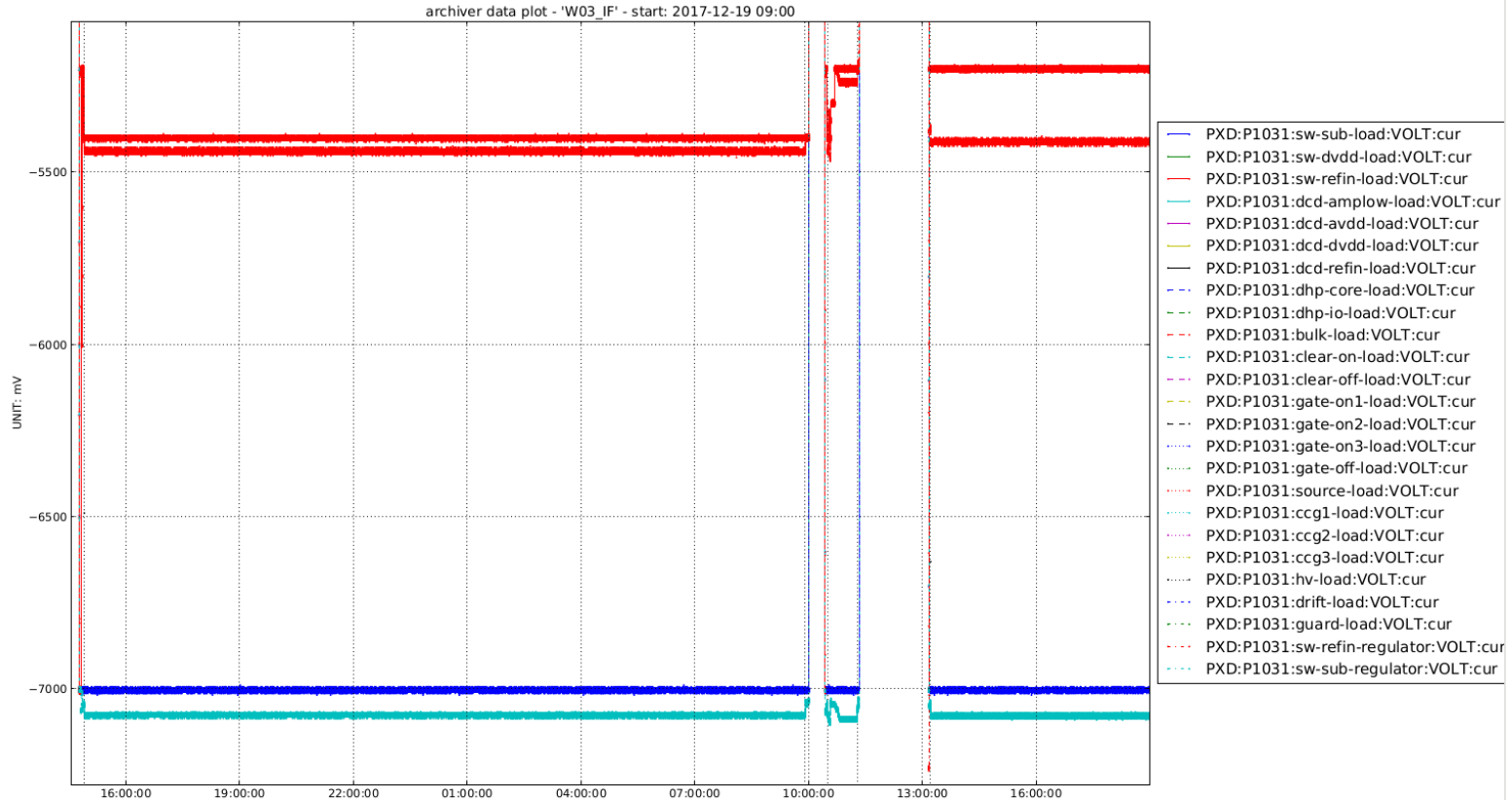
This behavior occurred at W02\_IF and W03\_IF on Dec 8





# Observations (1) W03\_IF

Difference of sw-refin @ regulator and @ load is increased from ~40 mV to ~ 200 mV



why is the voltage difference 200 mV although no current is flowing?

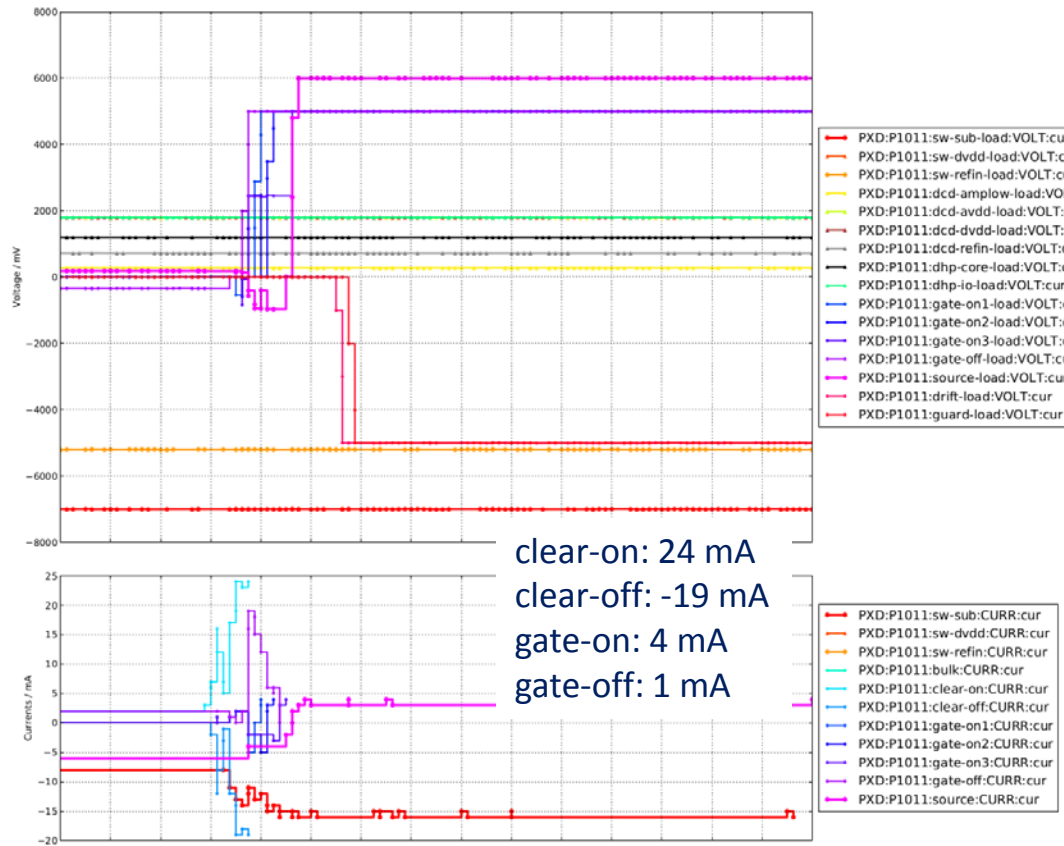
Which voltages are applied at the module?

Voltage at Regulator	Voltage at Load	Current	
-7086 mV	-7008 mV	-19 mA	sw-sub
2907 mV	1800 mV	20 mA	sw-dvdd
-5415 mV	-5203 mV	0 mA	sw-refin



## Increased clear-on, clear-off, gate-on, gate-off currents

past



now

Voltage at Load	Current	
19003 mV	77 mA	clear-on
3019 mV	-60 mA	clear-off
-2498 mV	-7 mA	gate-on1
-2503 mV	-7 mA	gate-on2
-2501 mV	-6 mA	gate-on3
5002 mV	26 mA	gate-off



# How are the voltages sensed at the different domains?

## Gate-GND:

- GateOn (GateLow)
- GateOff (GateHigh)
- CCG1, CCG2, CCG3
- Drift

## Steer-GND:

- ClearOn (ClearHigh)
- ClearOff (ClearLow)
- Bulk
- HighVoltage (Backplane)
- Guard
- SW-SUB and SW-REFIN

## DGND:

- SW-DVDD
- DHP-CORE
- DHP-IO
- DCD-DVDD

## AGND:

- DCD-AVDD
- DCD-REFIN
- DCD-AMPLOW
- SOURCE

Voltage	Sensing - Location
sw-sub	Breakout Board / Dock Box
sw-dvdd	Module (before sw close to EOS)
sw-refin	Module (before sw close to EOS)
dcd-amplow	Module (mid of DCDs)
dcd-avdd	Module (mid of DCDs)
dcd-dvdd	Module (mid of DCDs)
dcd-refin	Module (mid of DCDs)
dhp-core	Module (mid of DHPs)
dhp-io	Module (mid of DHPs)
bulk	PS
clear-on	Module (before sw close to EOS)
clear-off	Module (before sw close to EOS)
gate-on1	Module (before sw close to EOS)
gate-on2	Module at Switcher 3/4
gate-on3	Module at Switcher at gluing edge
gate-off	Module (before sw close to EOS)

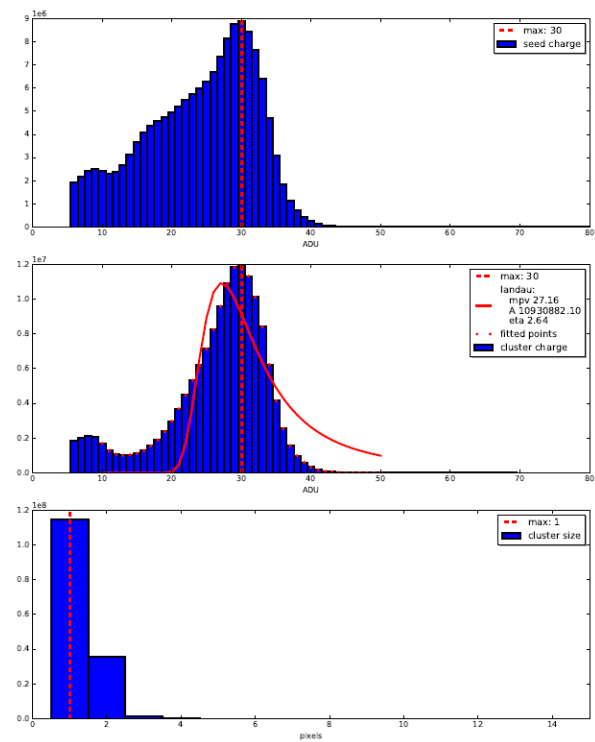
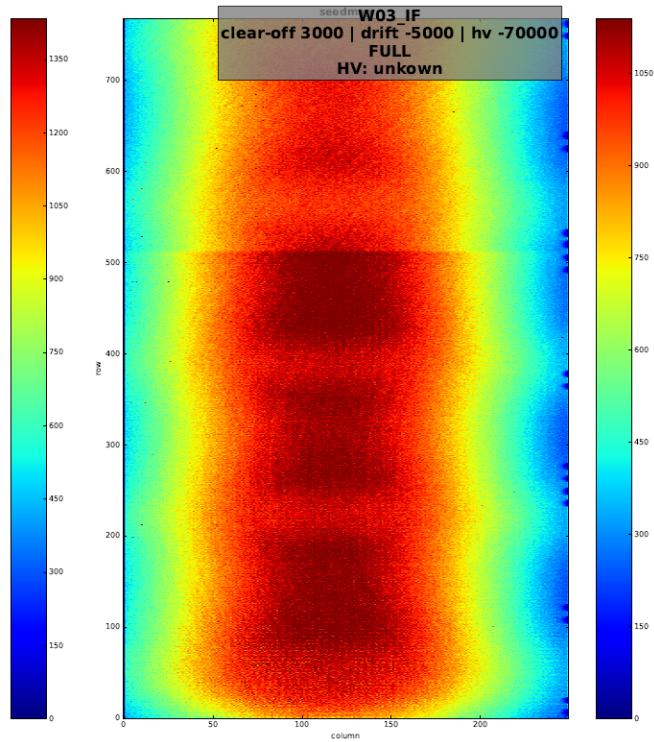
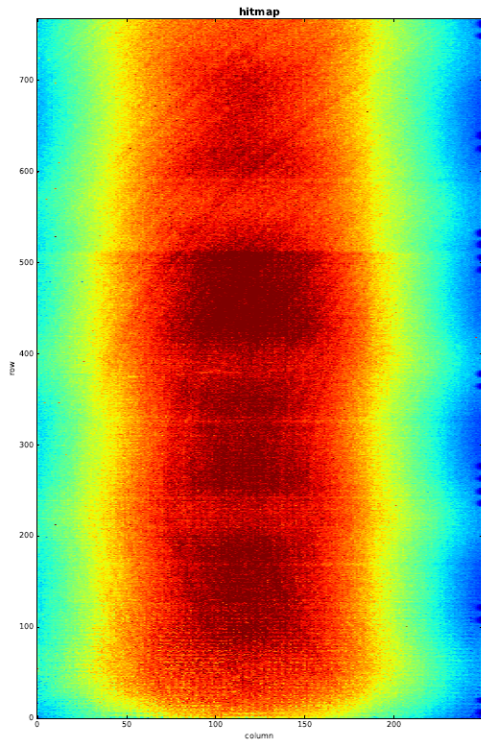
gate-on1	Module (before sw close to EOS)
gate-on2	Module at Switcher 3/4
gate-on3	Module at Switcher at gluing edge
gate-off	Module (before sw close to EOS)
source	Module between DEPFET and DCD
ccg1	PS / DockBox ?
ccg2	PS / DockBox ?
ccg3	PS / DockBox ?
hv	PS
drift	PS / DockBox ?
guard	PS
AGND	Module (mid of DCDs)
GNDD	Module (mid of DCDs)

<https://confluence.desy.de/display/BI/Voltage+Sensing>

<https://agira.desy.de/browse/BIIPXDH-161>

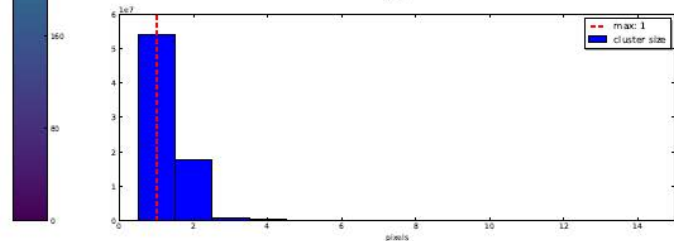
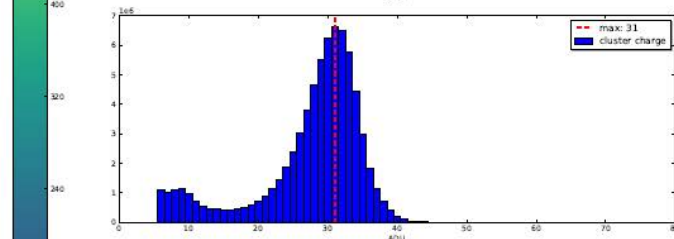
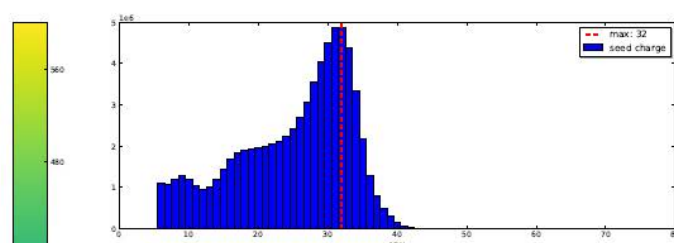
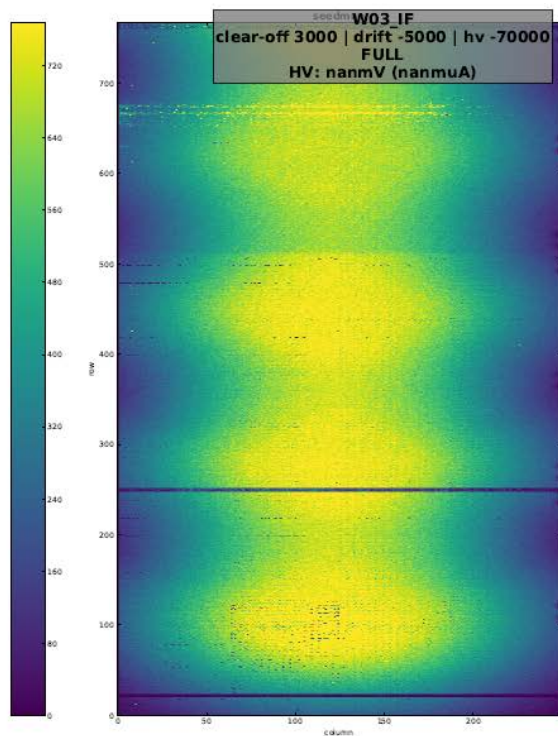
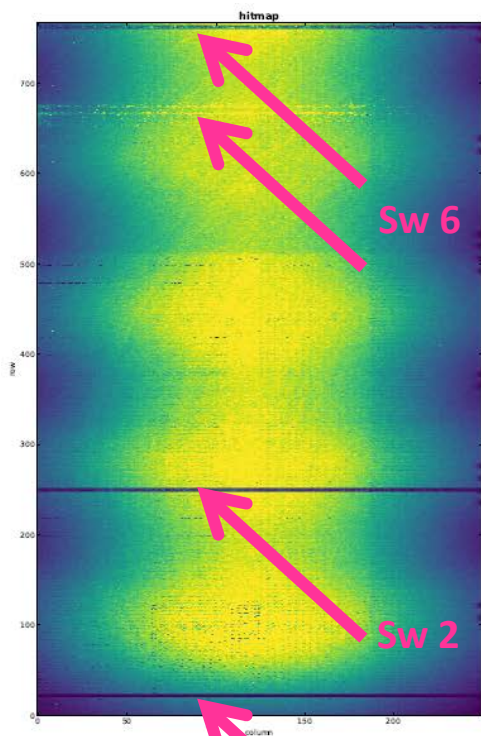


# Comparison W03\_IF (before accident)



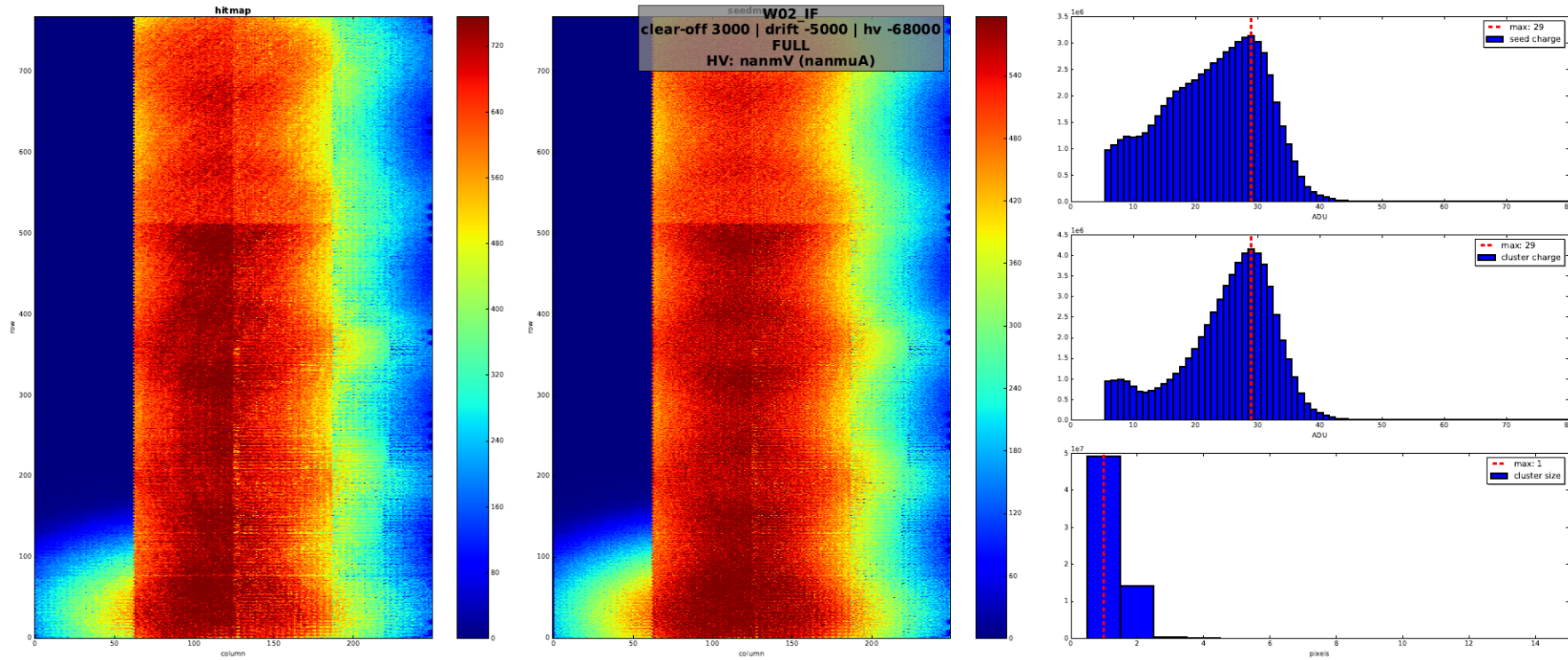


# Comparison W03\_IF (after accident)





# Comparison W02\_IF (before accident)

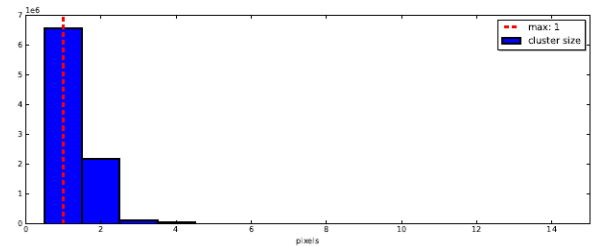
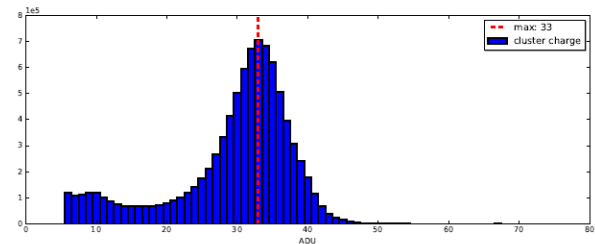
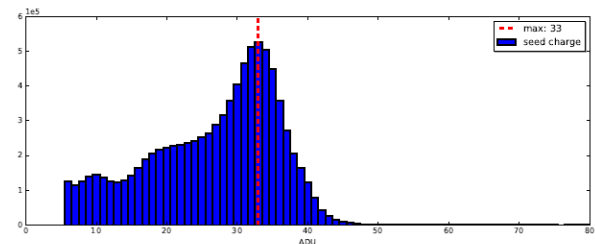
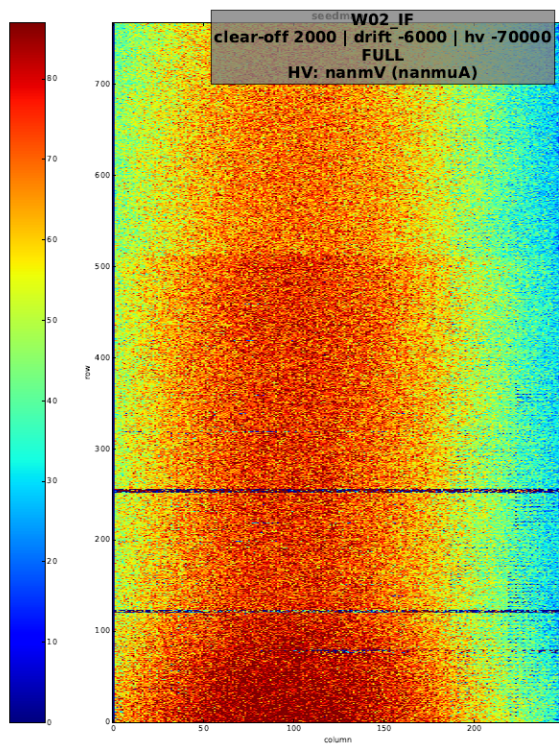
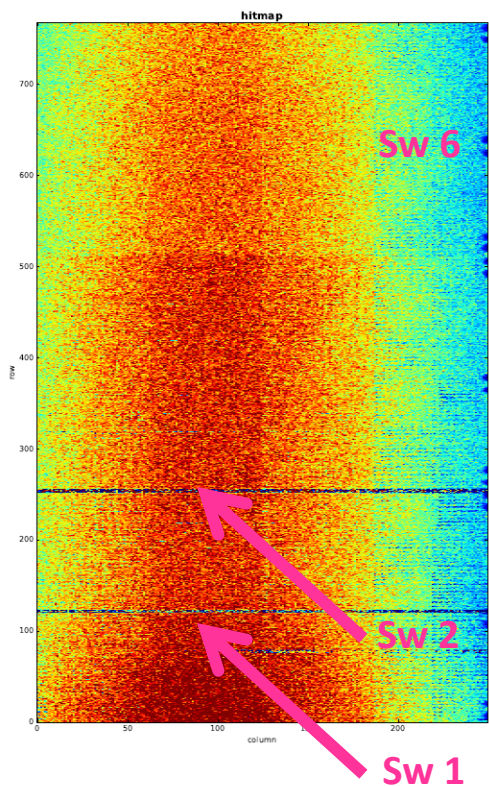


one link crashed – accident happend when repeating the scan. Therefore, power cycle should be done



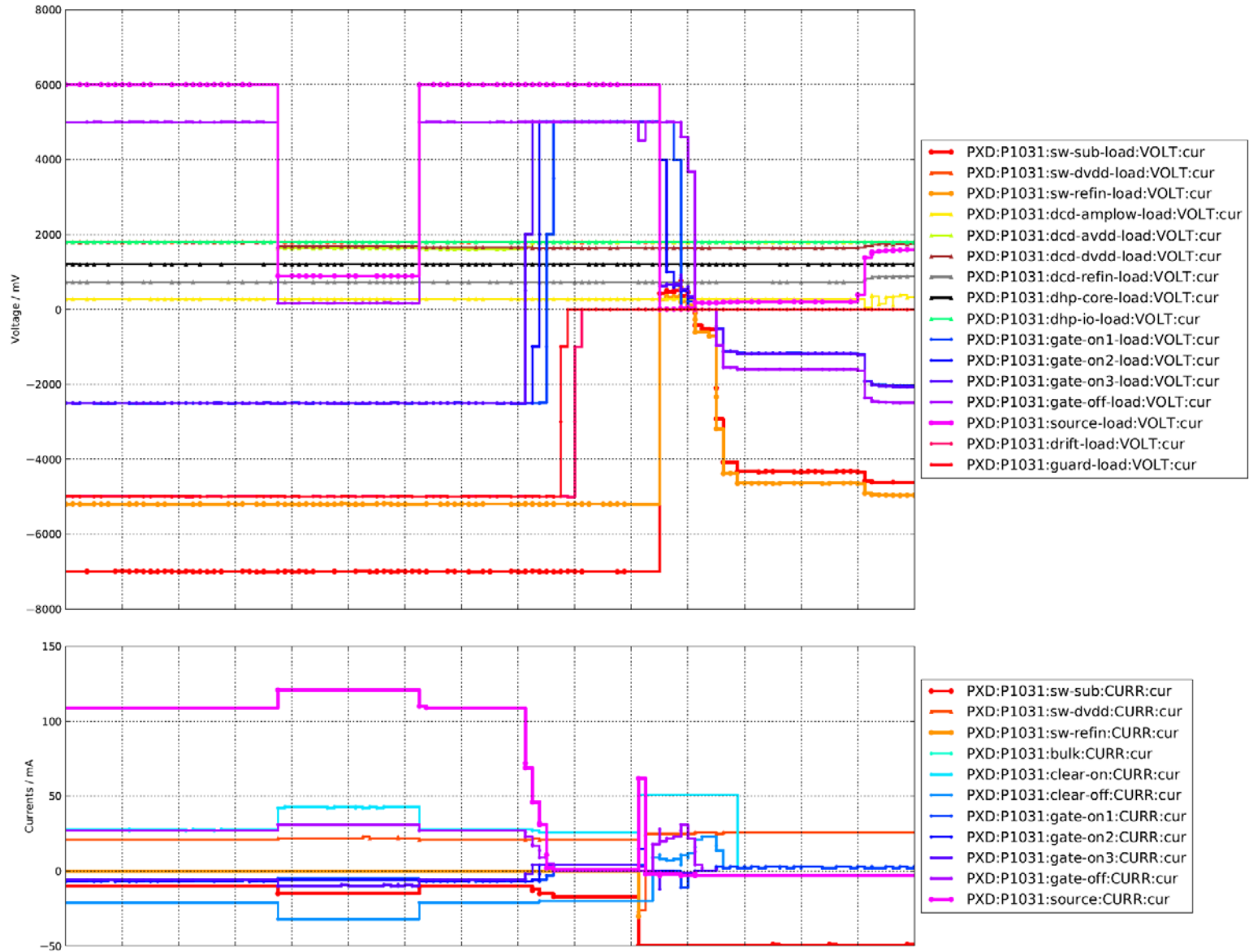


# Comparison W02\_IF (after accident)



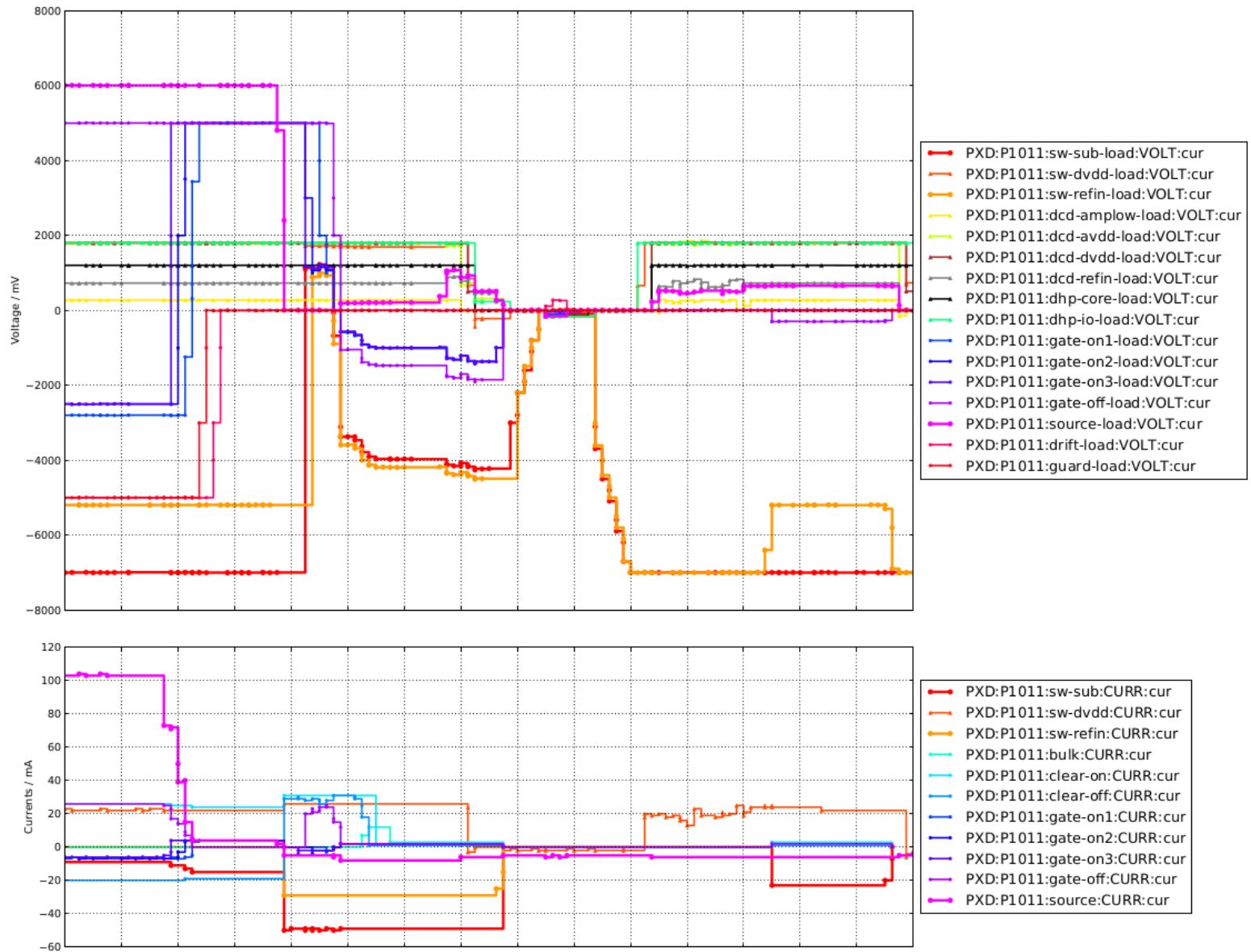


# Observations in the past, Sep 14, 17:34 – unknown module





# Observations in the past, Sep 26, 14:45 – W08\_IF





# W02\_IF – Nov 2, 2017 – W08\_IF



# Conclusion



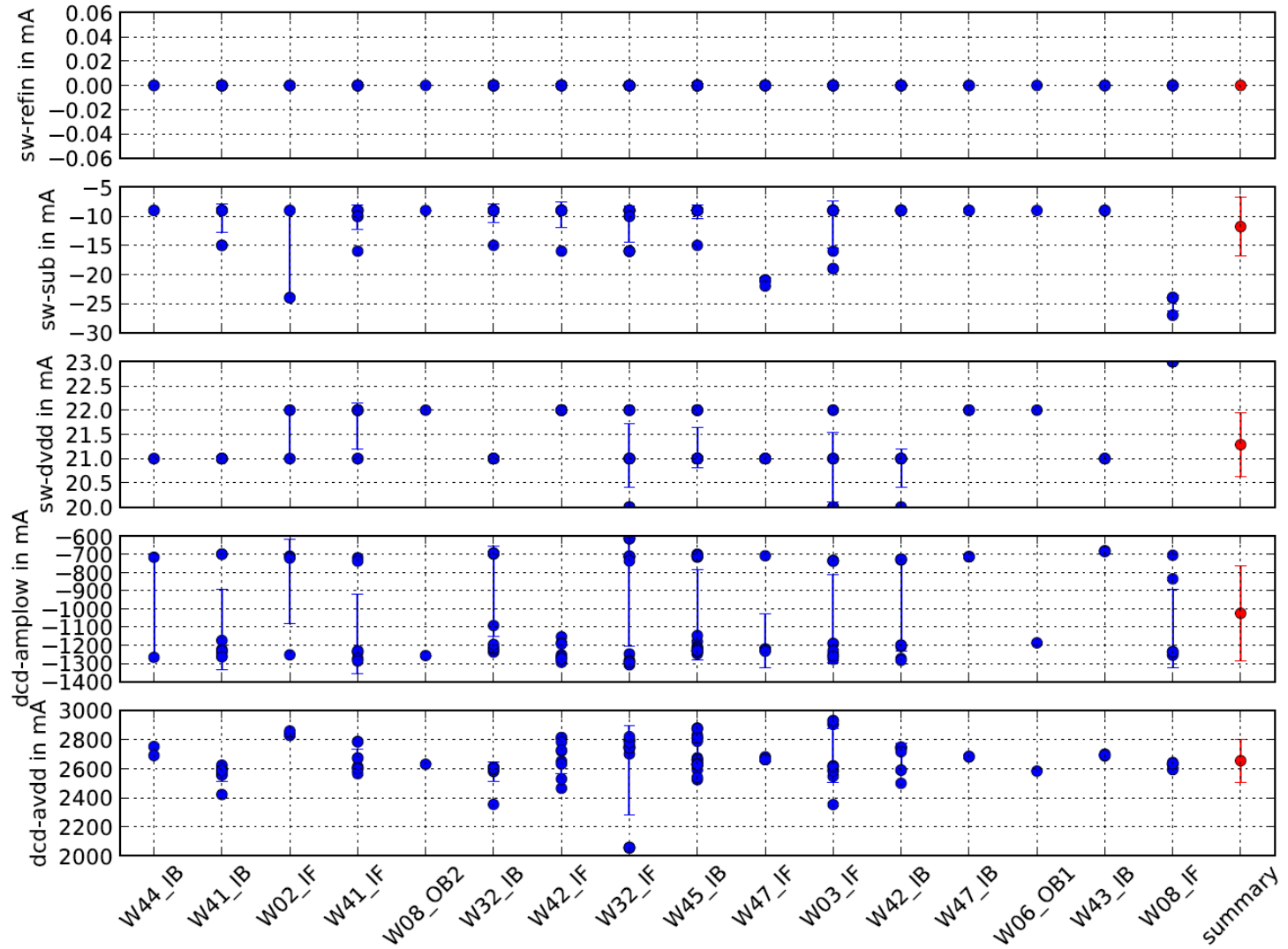
After investigations of all power down cycles since the archiver was set up. This switcher behavior occurred once (begin of November) which did not destroy the switcher

Ramp down source slower

Capcitors between sw-sub & source, sw-refin & source on Kaptons ? influences?

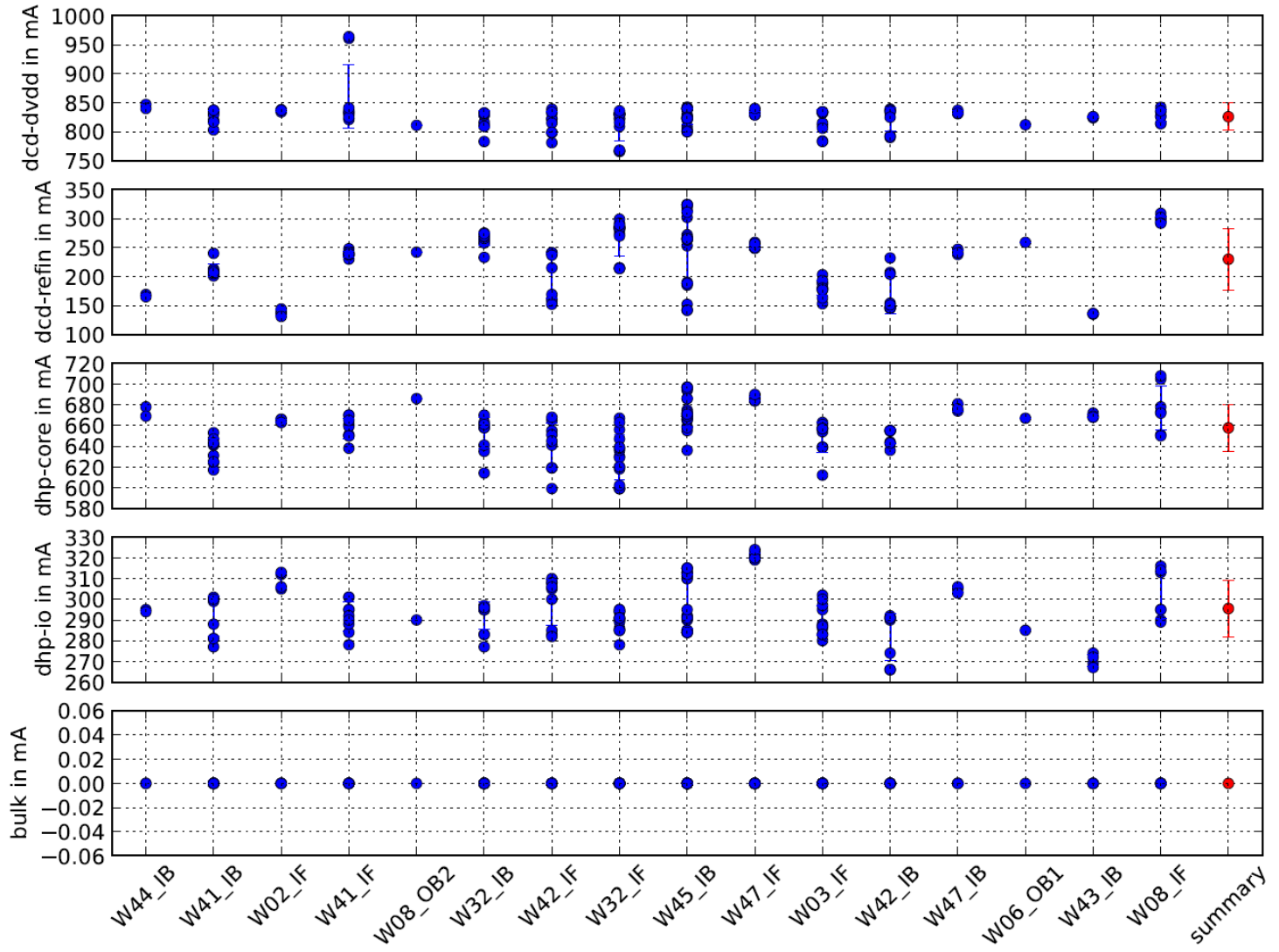


# Default current consumptions



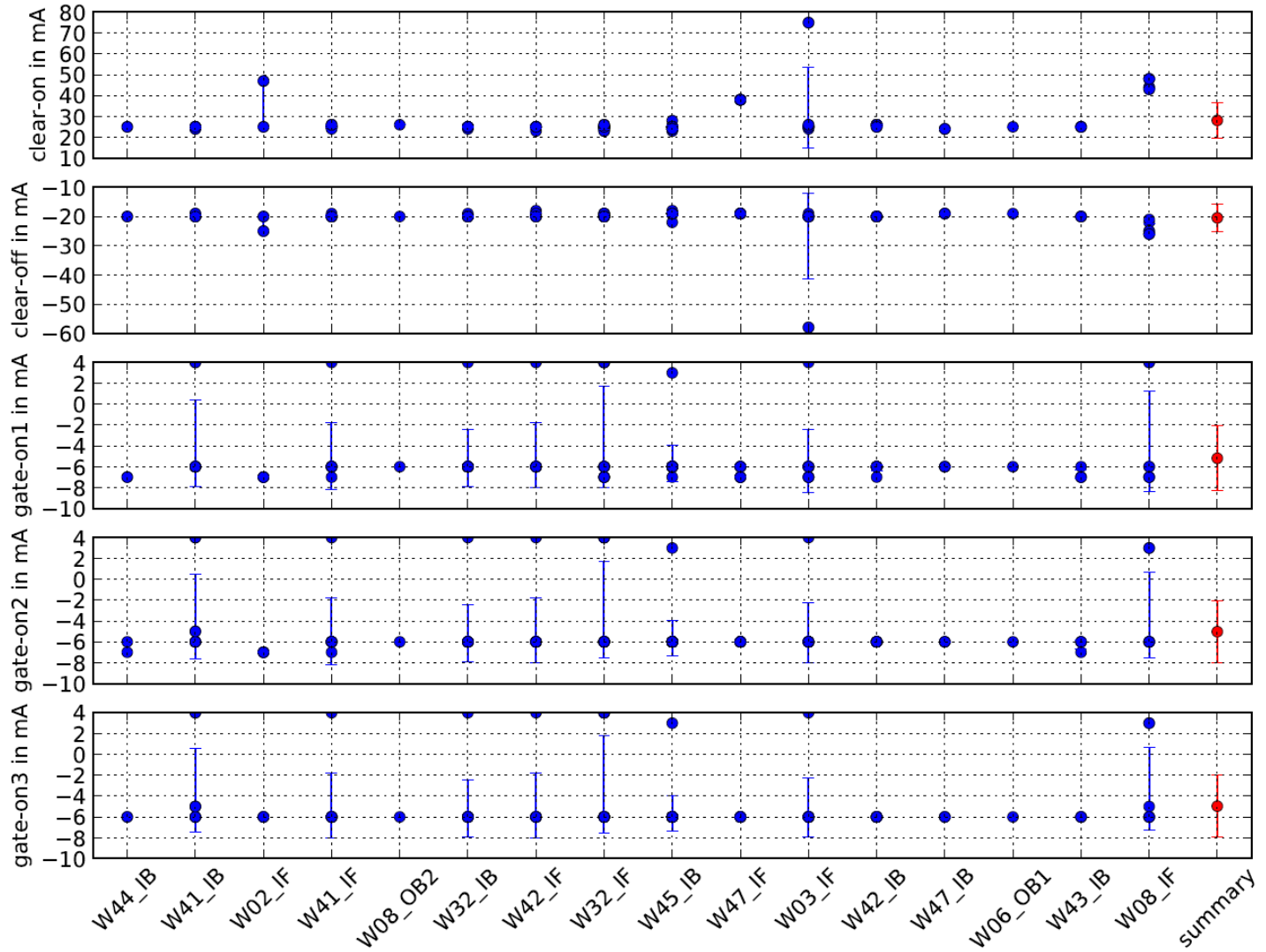


# Default current consumptions





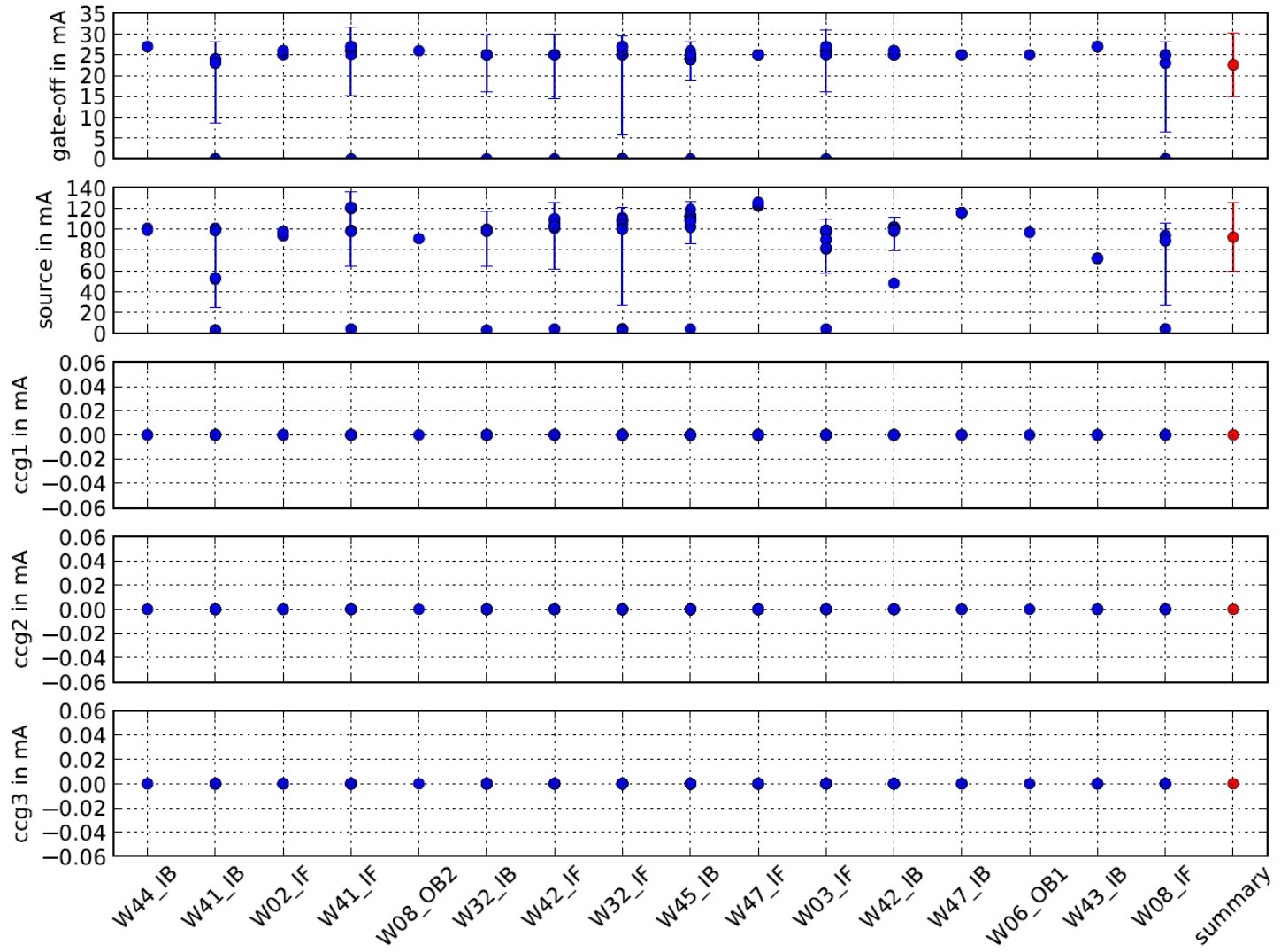
# Default current consumptions







# Default current consumptions





# Default current consumptions

