Technology at the HLL

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for the HLL Technology Group

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What technology do silicon pn-sensors require?

- **Maintain the purity** of FZ-Silicon (~$10^{12}/cm^3$)
- Process **both wafer sides** equally carefully.
- **Wafer-scale detector** designs => extensive visual inspection and repair strategies

MPI-HLL is the only lab worldwide that does process pn-detectors with integrated readout electronics.

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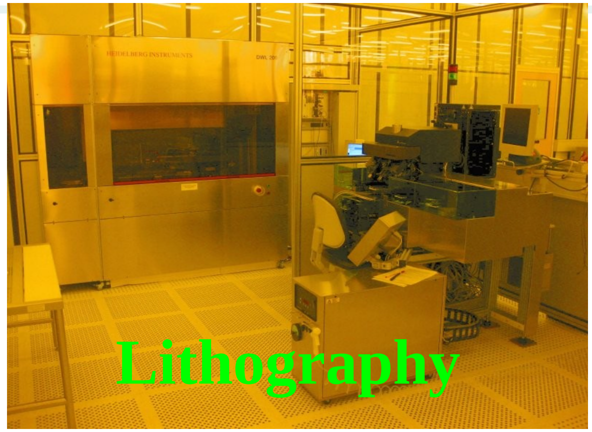
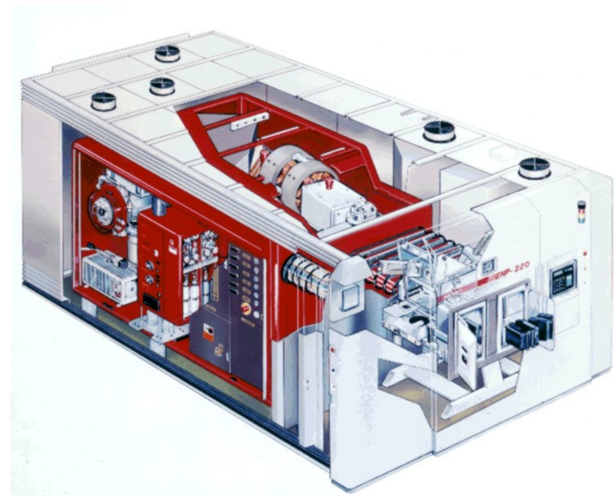
Technology overview



A wafer's life at HLL



Ion Implantation

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New processing steps introduced

- *Reduction of Leakage Current*
  - **Wafer Cleaning: automatic wet bench**
- *Waferscale Devices*
  - **Defect Inspection: automatic inspection microscope**
- *Minimum Feature Size*
  - **Polysilicon dry etch in existing PECVD chamber**
- *Ion Implantation*
  - **installed refurbished Ion Implanter**

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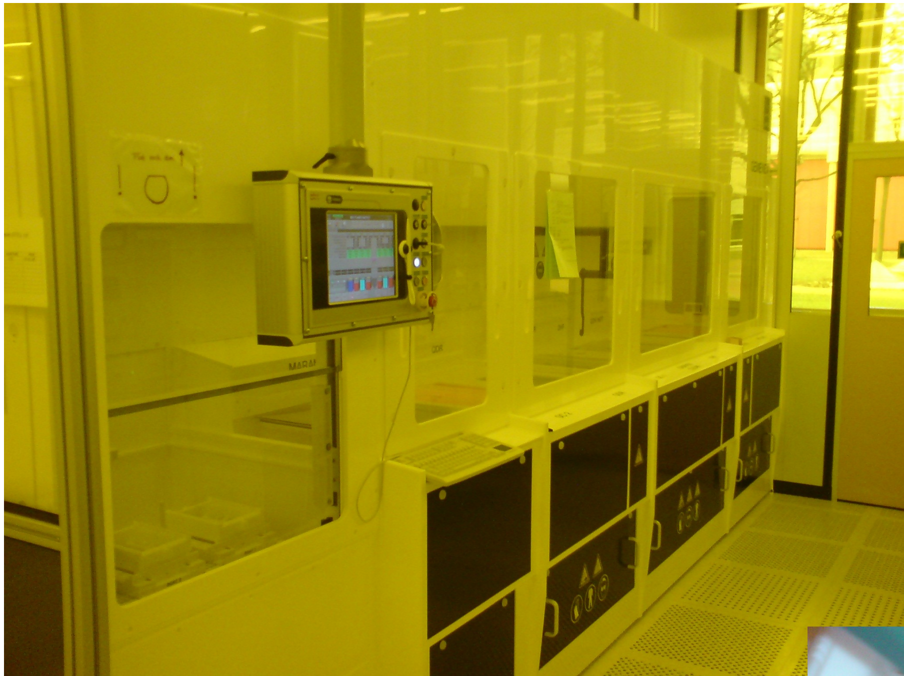
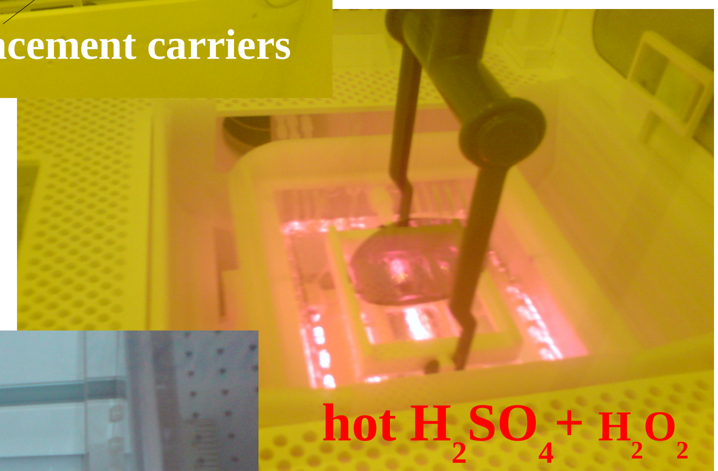
Automatic Wetbench





H_2SO_4 : organics

HF : remove oxide

NH_3 : remove particles

HCl : metals

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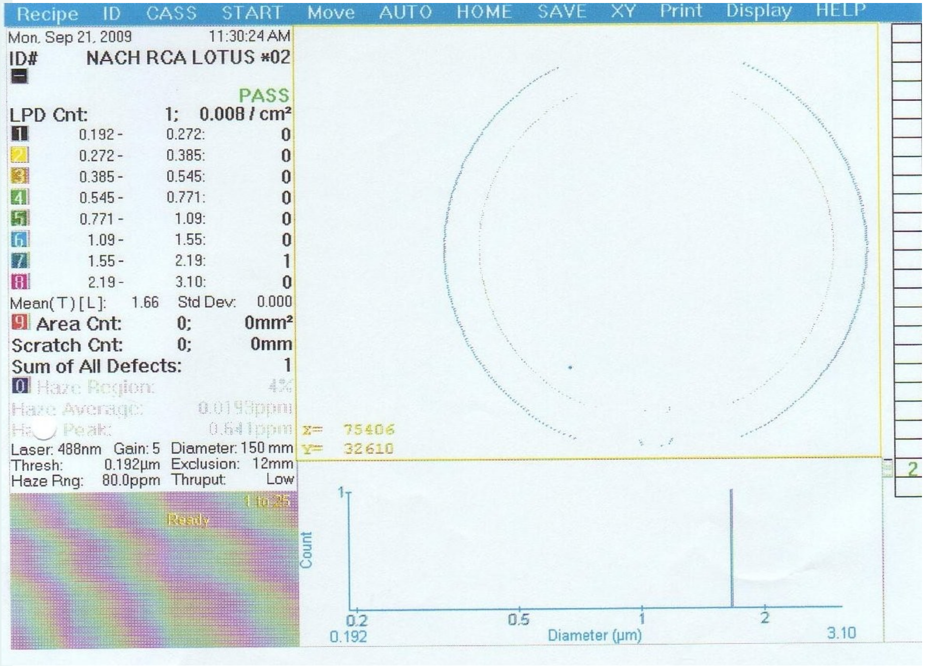
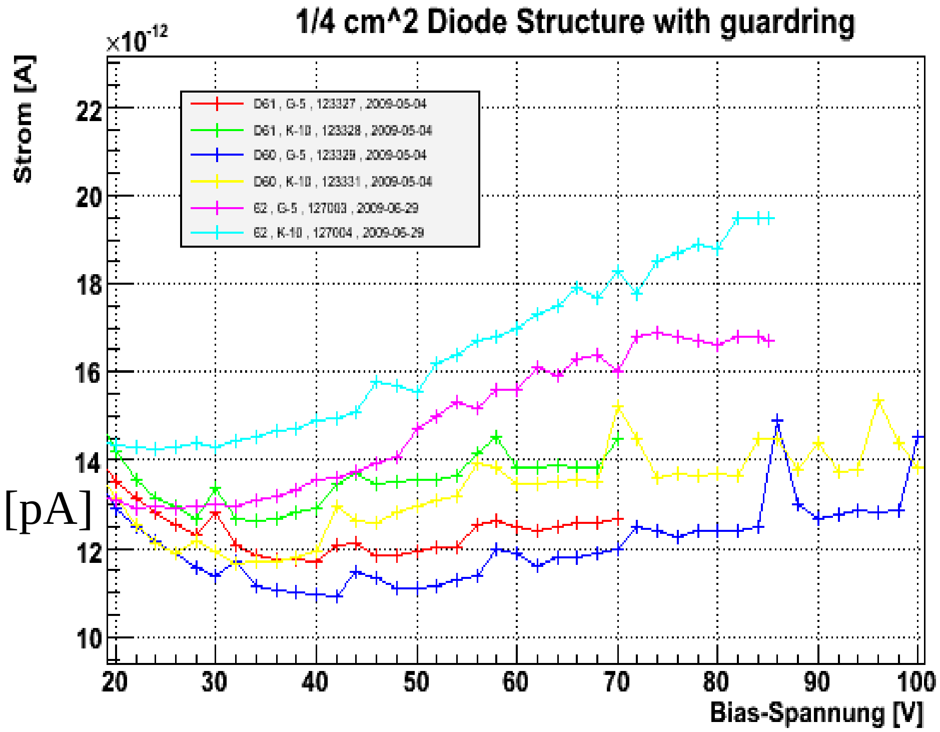
Results from Wetbench RCA clean

- excellent particle cleaning: less than 5 part > 200 nm
- stable surface metal concentration below detection limit (VPD-ICPMS)
- very good levels of leakage current in the fabrication





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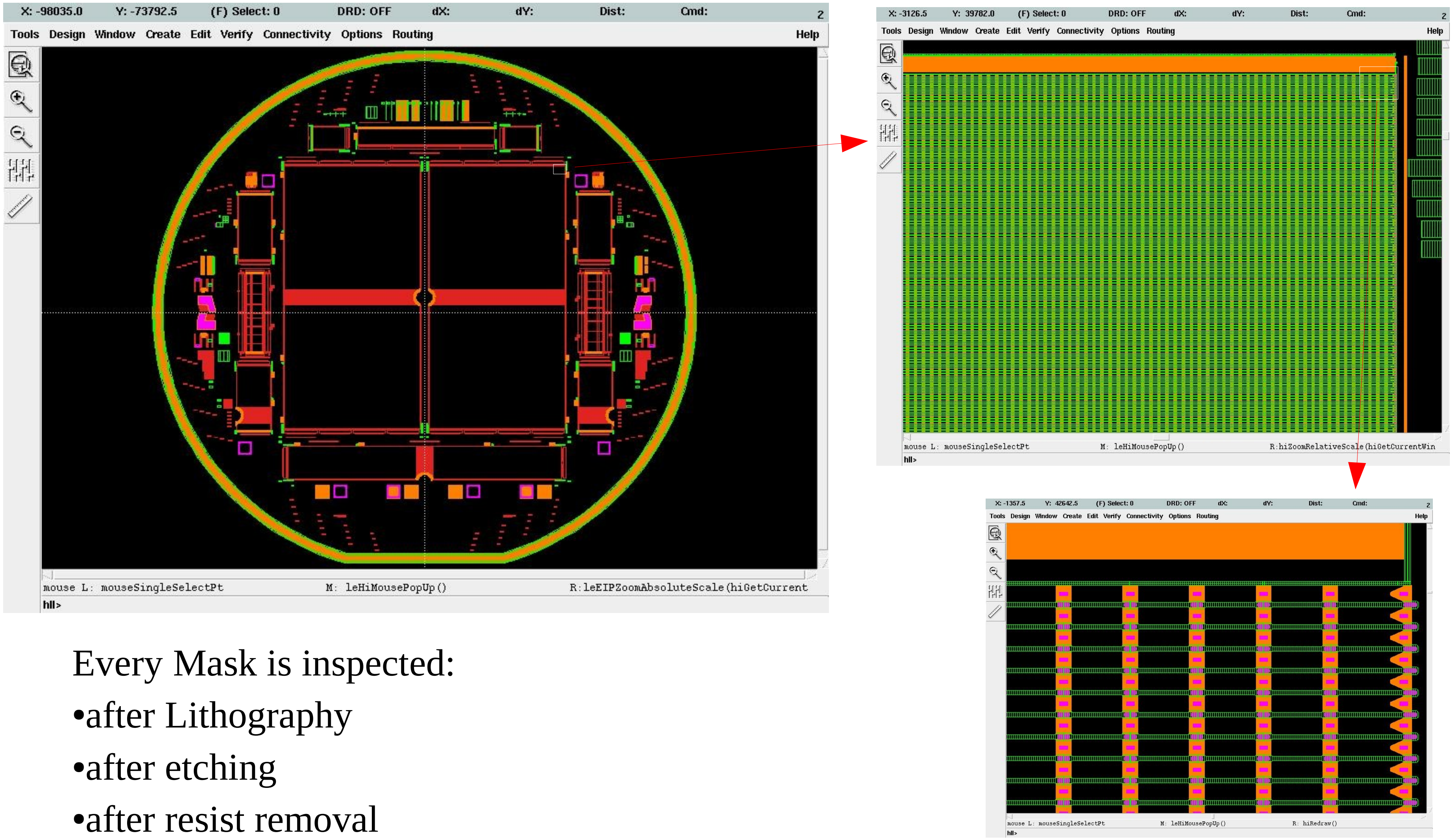
Manual Waferinspection is Timeconsuming



Every Mask is inspected:

- after Lithography
- after etching
- after resist removal

6 x 512 x 1024 = 3,1 Mio contact holes per ccd

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Brightfield-Inspection compares
one chip to the average of some others.

But: sometimes there are no others.

- large non-repetitive structures,
- any shapes allowed
- continuous design changes

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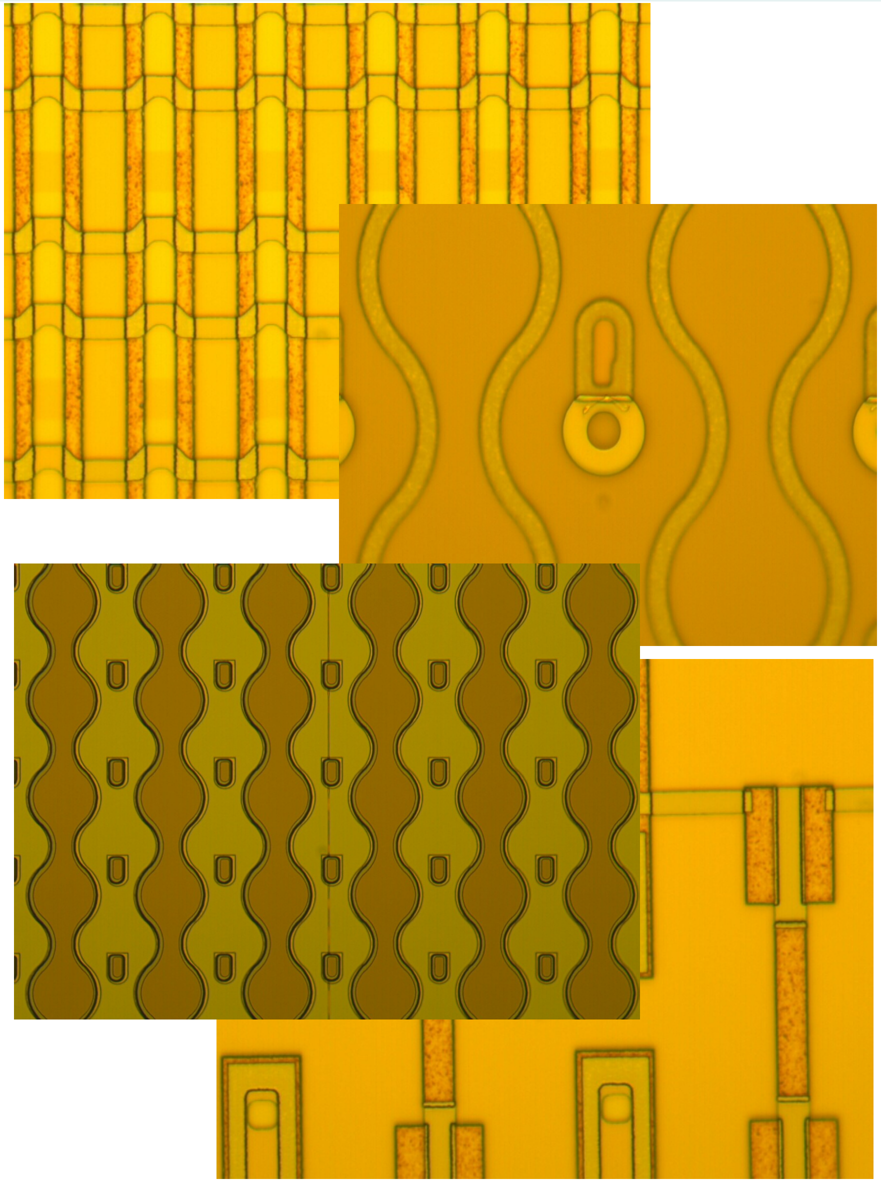
the plan: compare a whole wafer to
the average of some others



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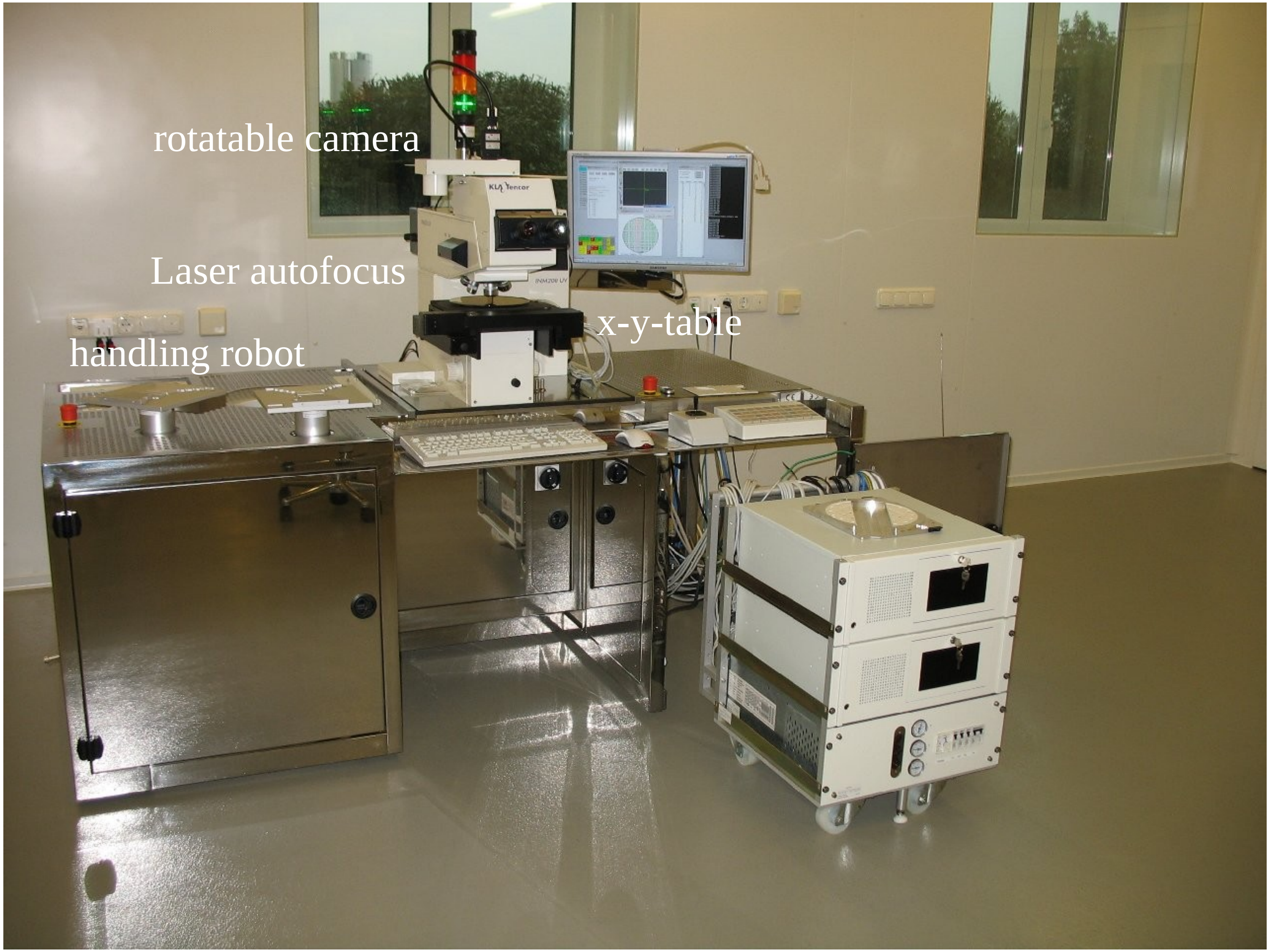
µ-tec Defectcheck 3000



Continuously
scanning
with electronic
shutter.

+computing
rack

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Requirements and Methods

Once per wafer

- Camera rotation alignement
- Wafer coordinate system alignement
  (Table accuracy ~2µm)

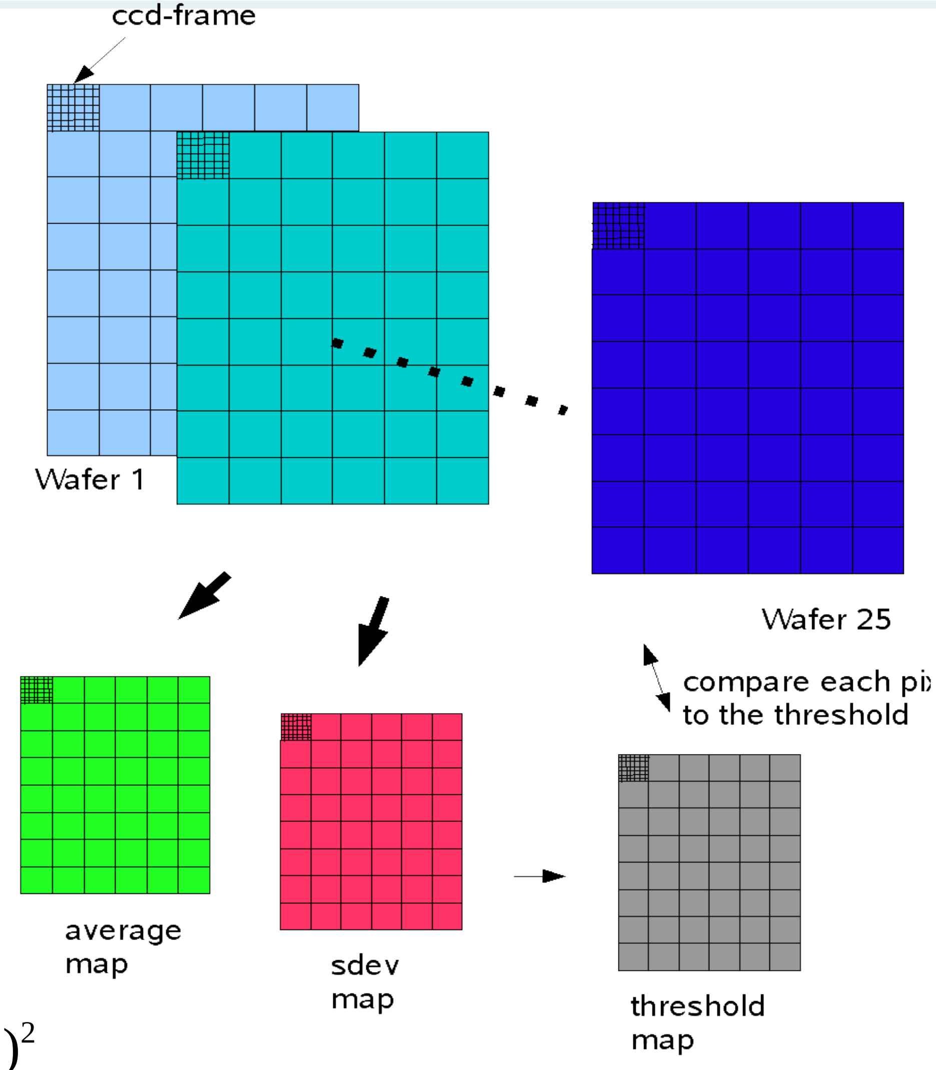
each frame

•frame alignment with subpixel resolution

each pixel

•calculate average, sdev, threshold
•compare

Pixelsize 0,5 µm (or less)
=> 90 GB of 8-Bit values per wafer $(3 \times 10^5)^2$
parallel computing => 20 min per wafer



-> defect classification

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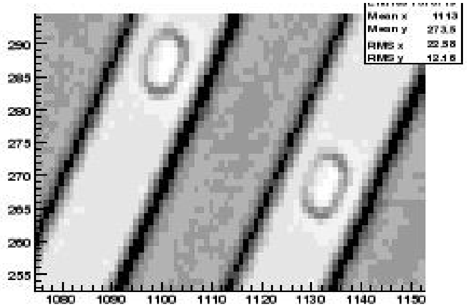
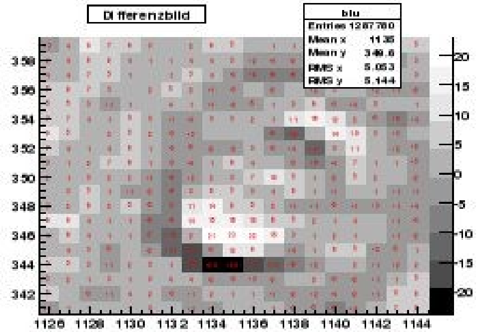
problematic alignment at unconventional shapes

ccd frame





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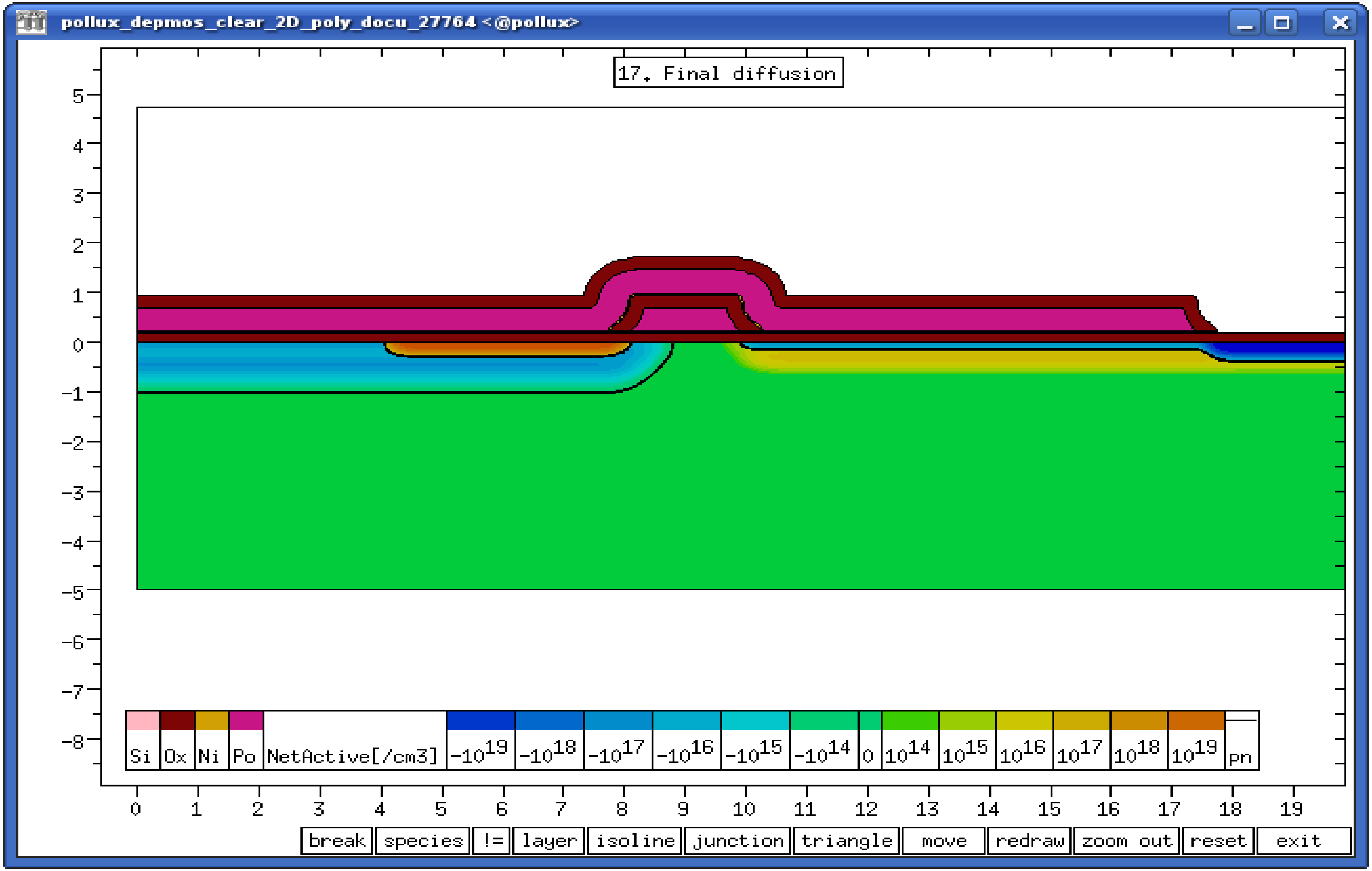
Polysilicon Technology



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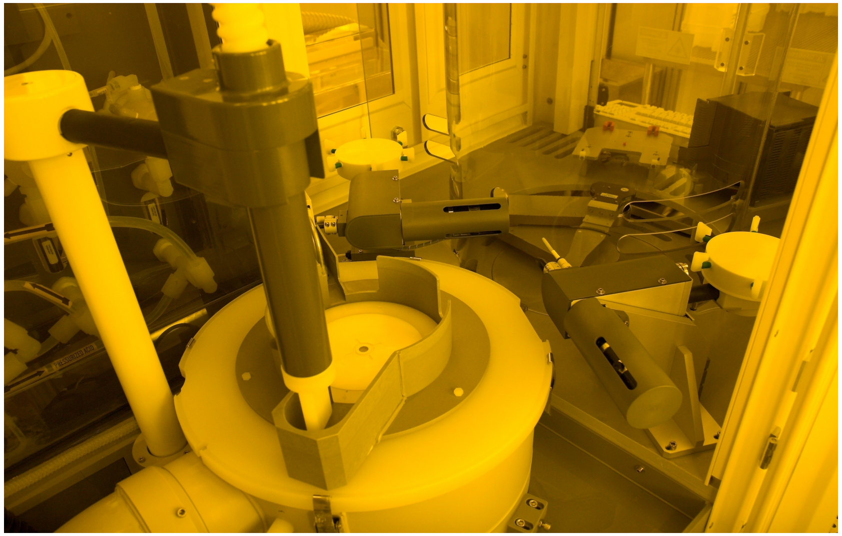
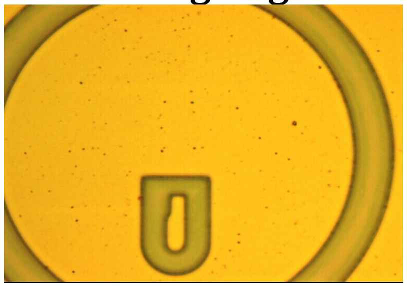
Feature sizes: wet etching of Polysilicon

Polysilicon is etched in a mixture of HNO_3 / HF.
No radiation damage, but severe disadvantages:

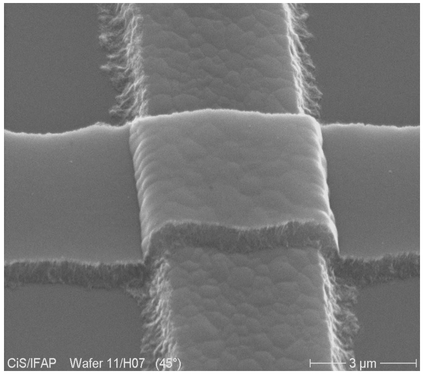
Single Wafer Spinetcher



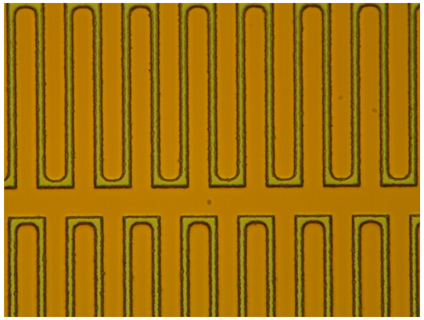
remaining Si grains

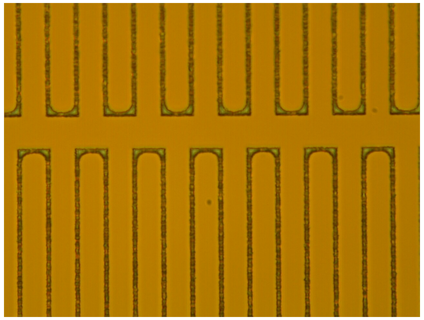


mousebites



Homogeneity
Dependence of etch-speed on surrounding structures (3 ym meander structures at different positions on chip)





=> poor linewidth control

(even worse for low-doped Poly)

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Feature sizes: plasma etching of Polysilicon

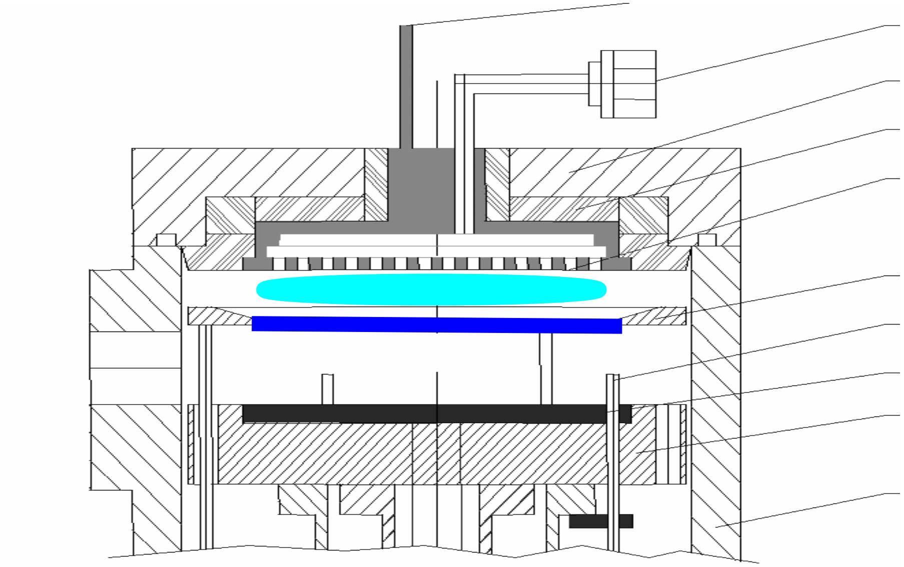
Plasma etching with SF6 at minimum Bias.

-> small physical (sputter) component.

-> less radiation damage

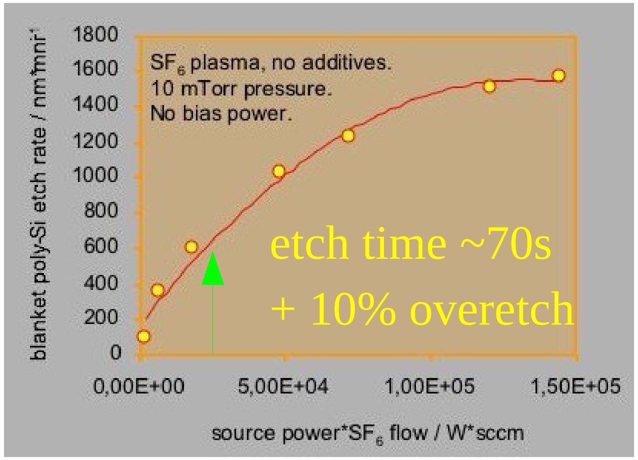
-> weak anisotropy

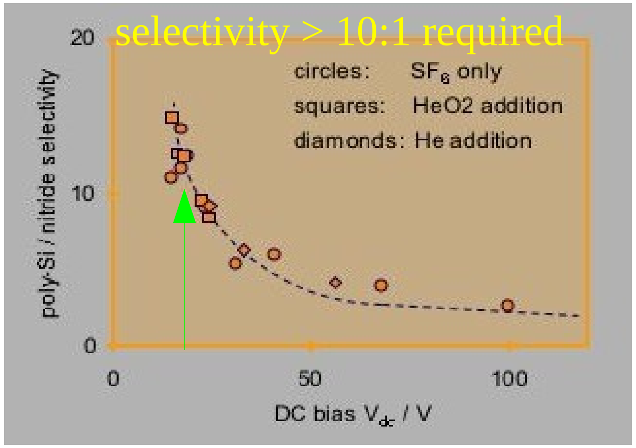
-> reasonable selectivity to Si3N4.



Existing High-Frequency (40MHz) PECVD

Deposition chamber can be used with SF6 and O2.





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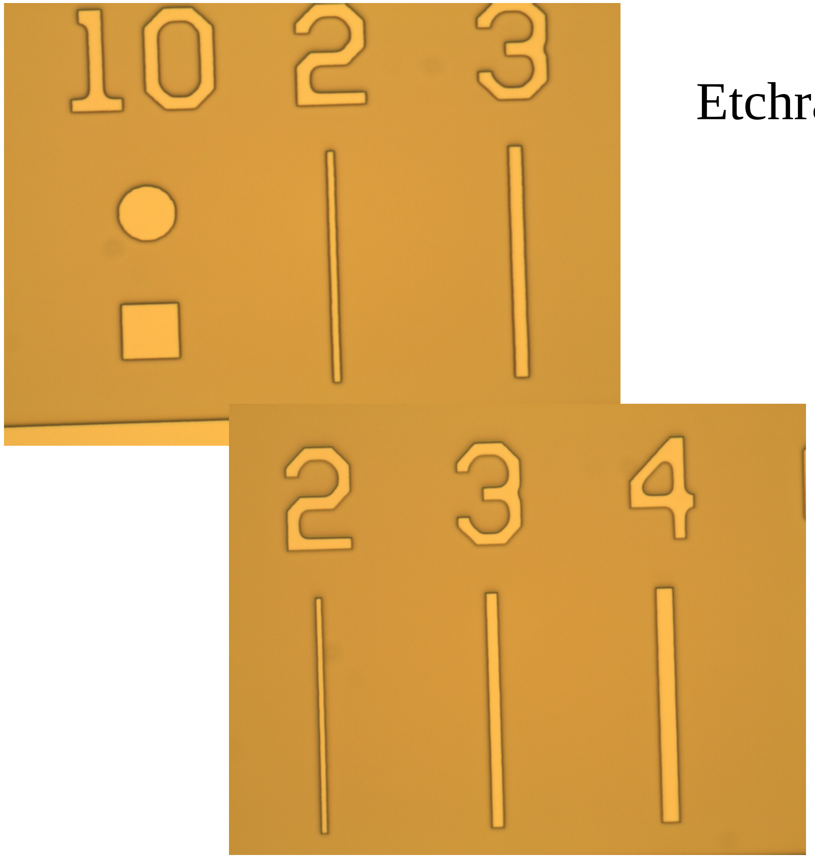
Results from SF6-Etching

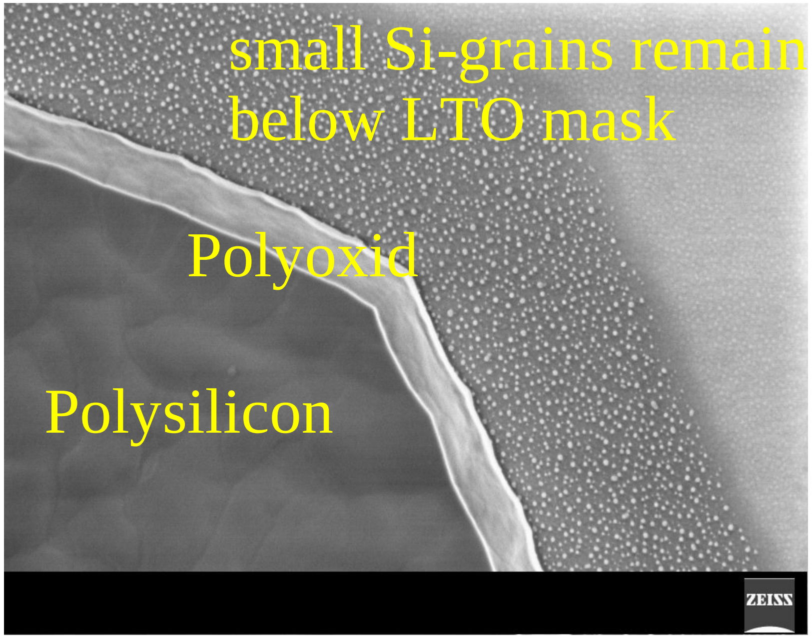
w15: center



w15: edge - 15mm

Homogeneity is improved by addition of small amount of O2 -> we use LTO hardmask

Etchrate of Si3N4 -> we loose 1/3 to 1/2 of the layer



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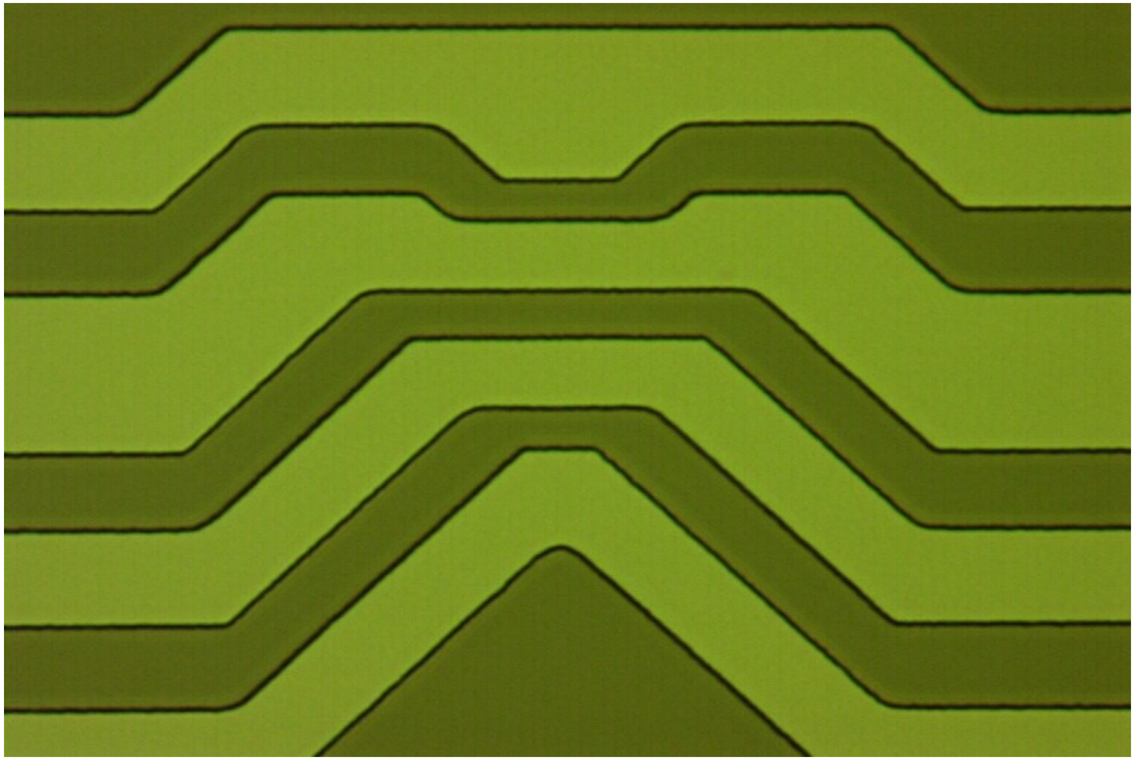
Results from SF6 etching

- structuring looks reasonably well,
- radiation damage needs to be quantified
- will be used for two wafers in pxd-6-1 (BELLE-2)



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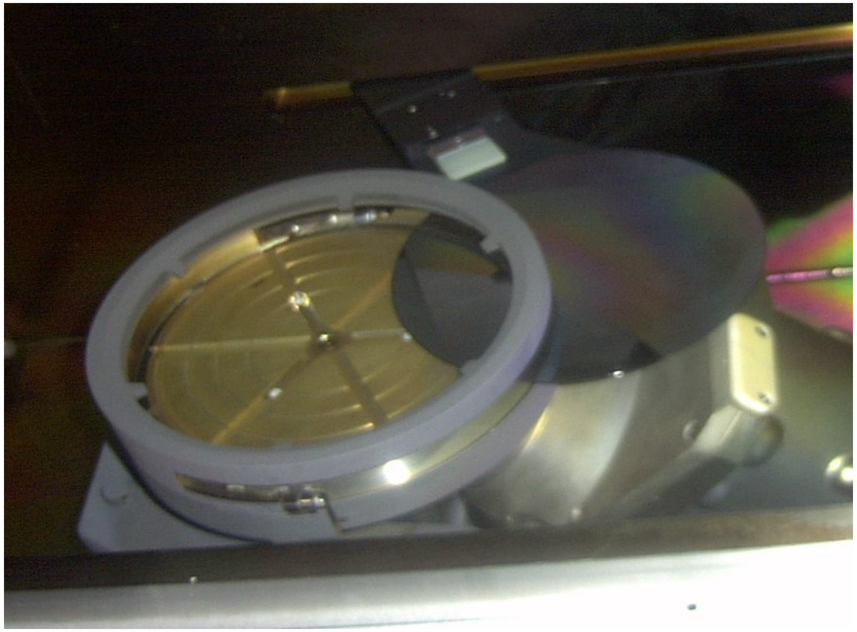
Why run our own implanter ?

1) Average time per Implant is 10 days
2) Handling is not optimized for backside protection
3) Uncertainty of supply



Medium current Implanters cover 2-750 keV, B, Ph, As

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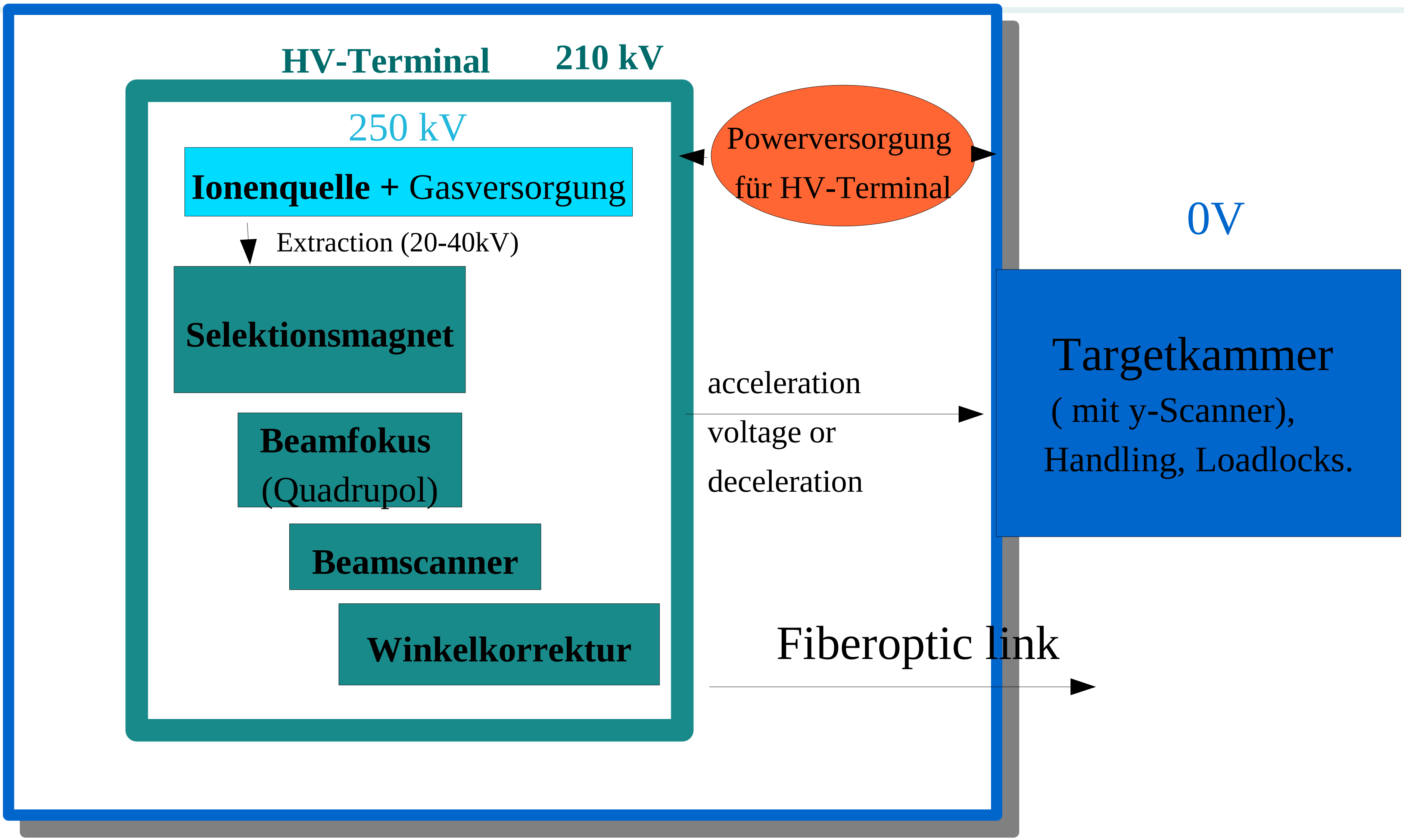
Overview of a medium current implanter



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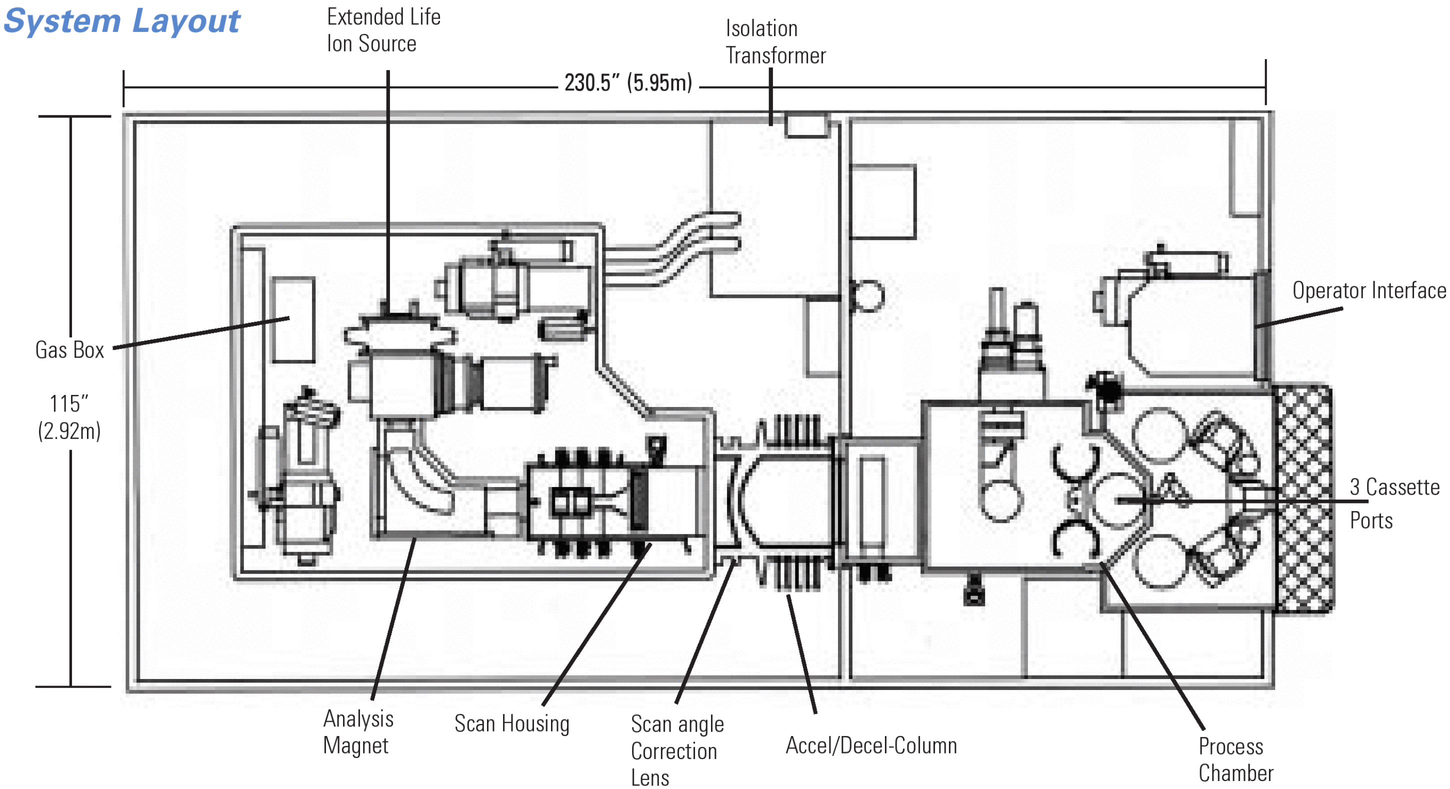
Axcelis 8250



- Plasma Ion Source with Gas supply (evaporator possible)
- Electrostatic Quadrupol focussing
- Electrostatic scanner in x
- Electrostatic lens for angular correction
- Acceleration und Deceleration-mode.
- Angular Energy Filter

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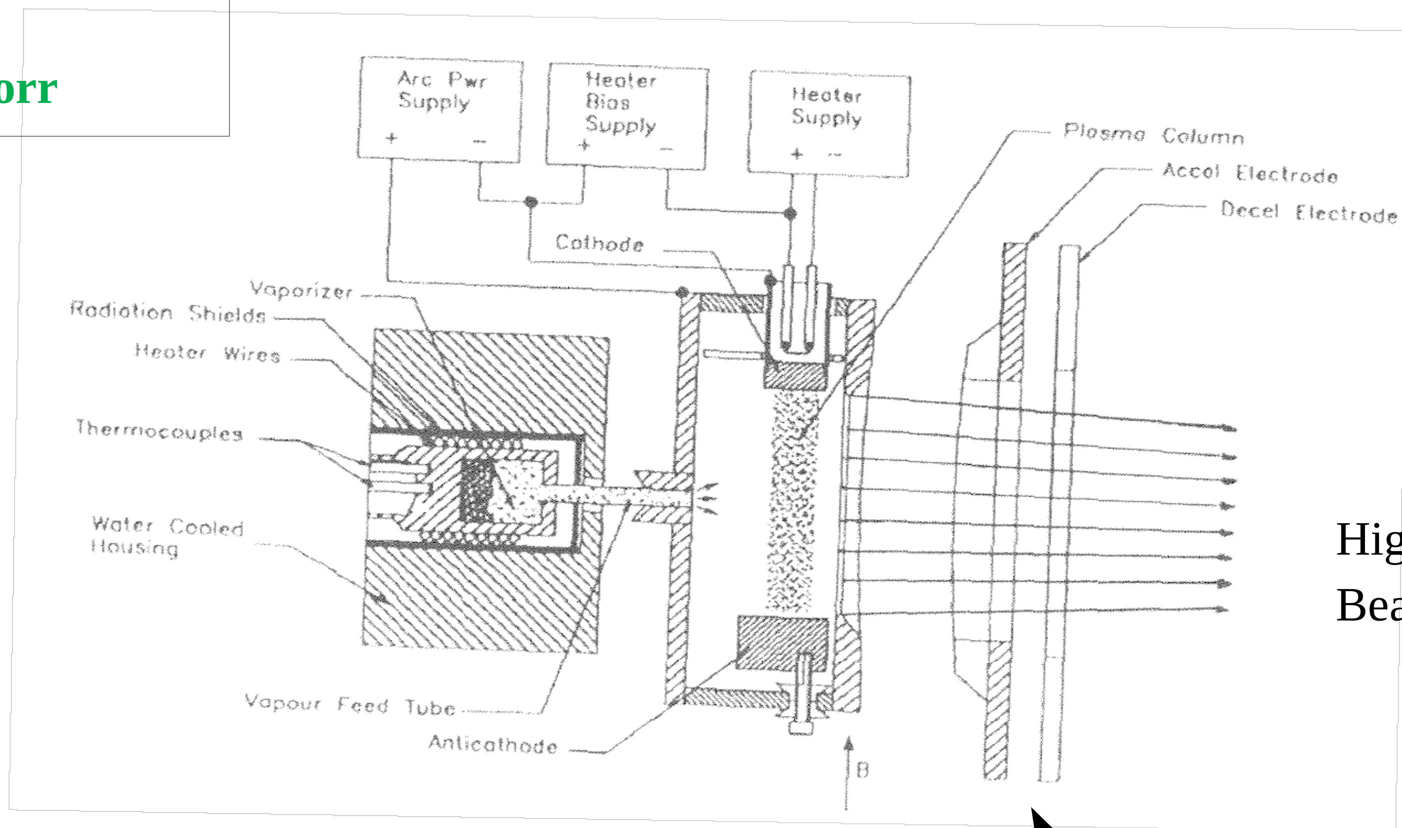
Ion Source overview

~2500°C

p~ E-3 torr



High vacuum

Beamline E-6 mBar

Source magnet

confines plasma

3-axis Electrode manipulator adjusts beam focusing

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Implanter Beamline

Terminal

Analysis magnet quadrupol lens scanner Parallelizing lens + Accelerator

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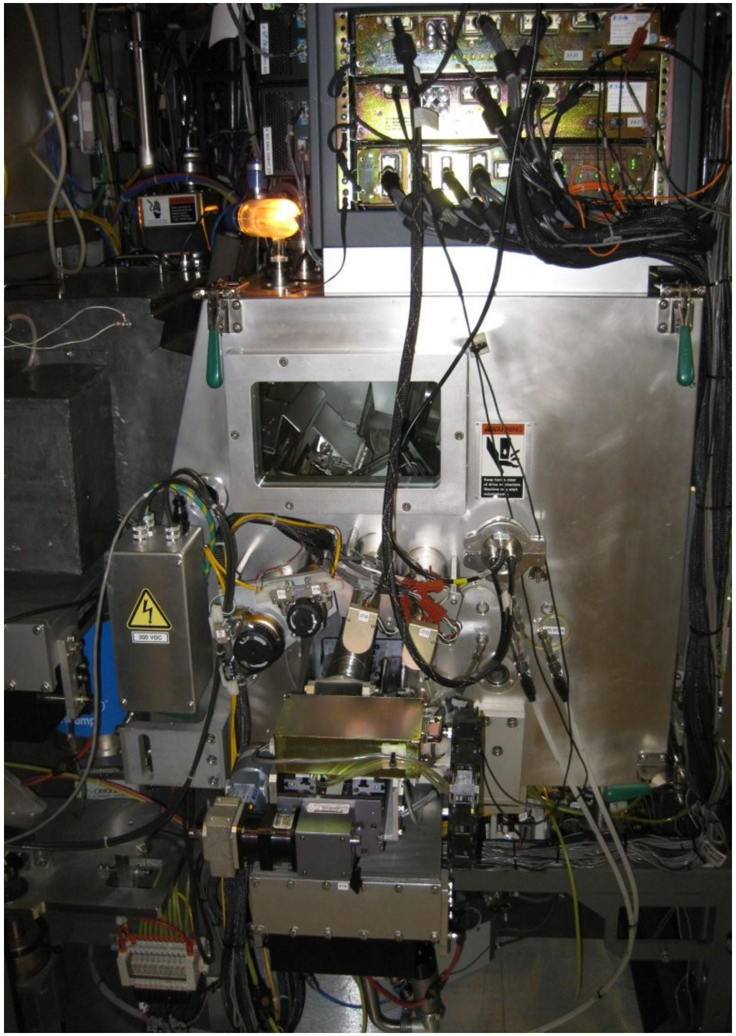
Endstation

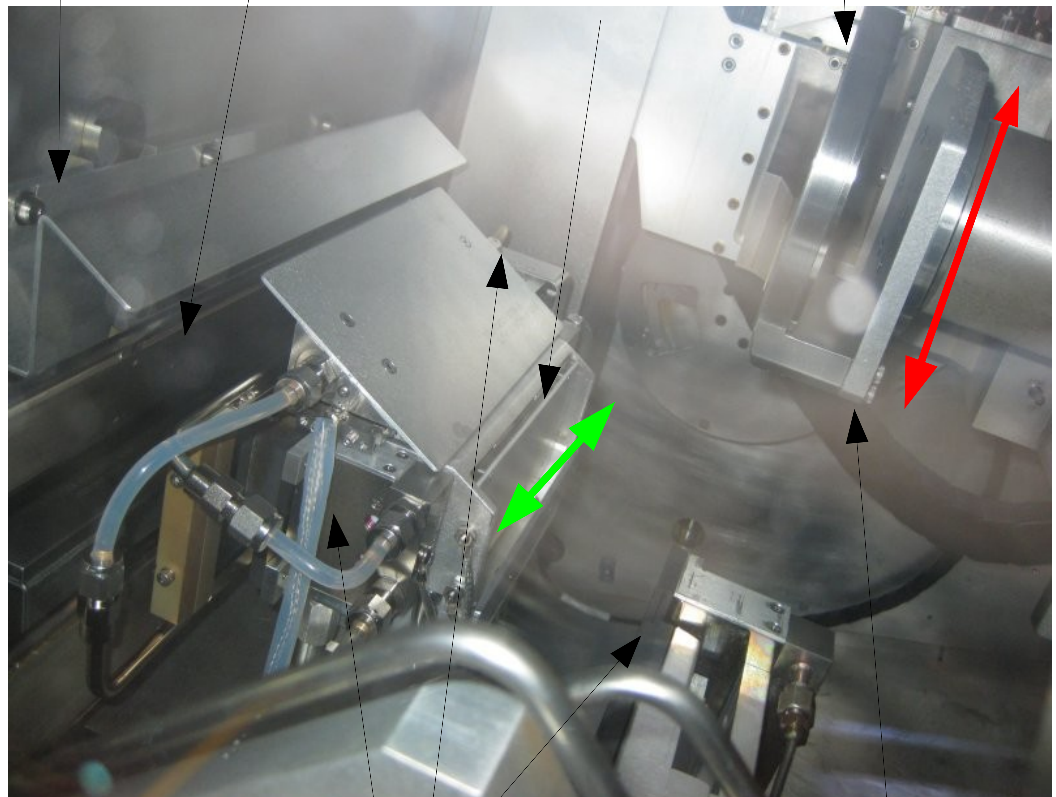


Angular energy filter 15°

variable aperture

flag (Dosimetry)

Wafer



Twist 360°

Faraday cups for profiling

Tilt 0-60°

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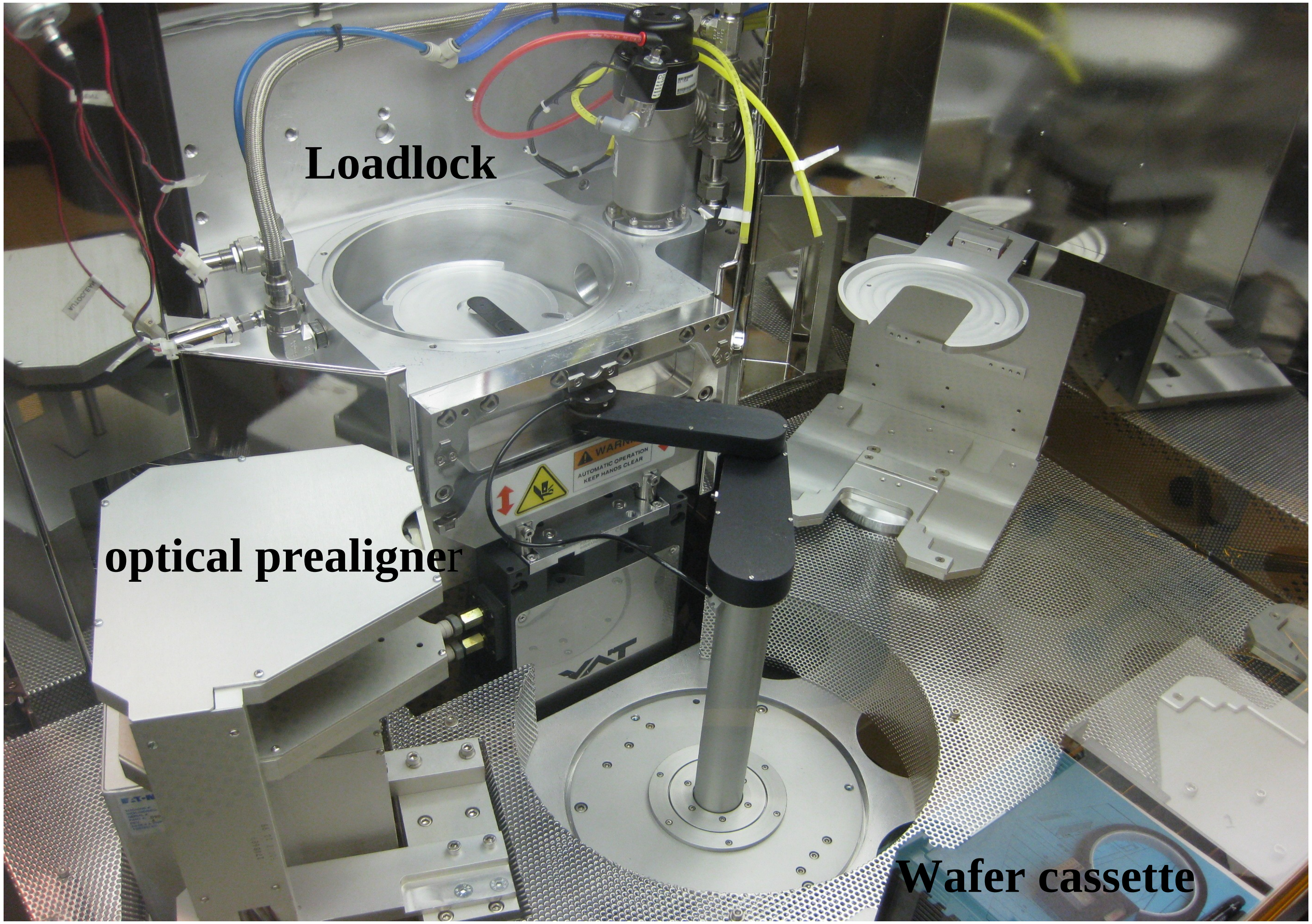
Wafer Handling



Handling will finally be 100% damage free

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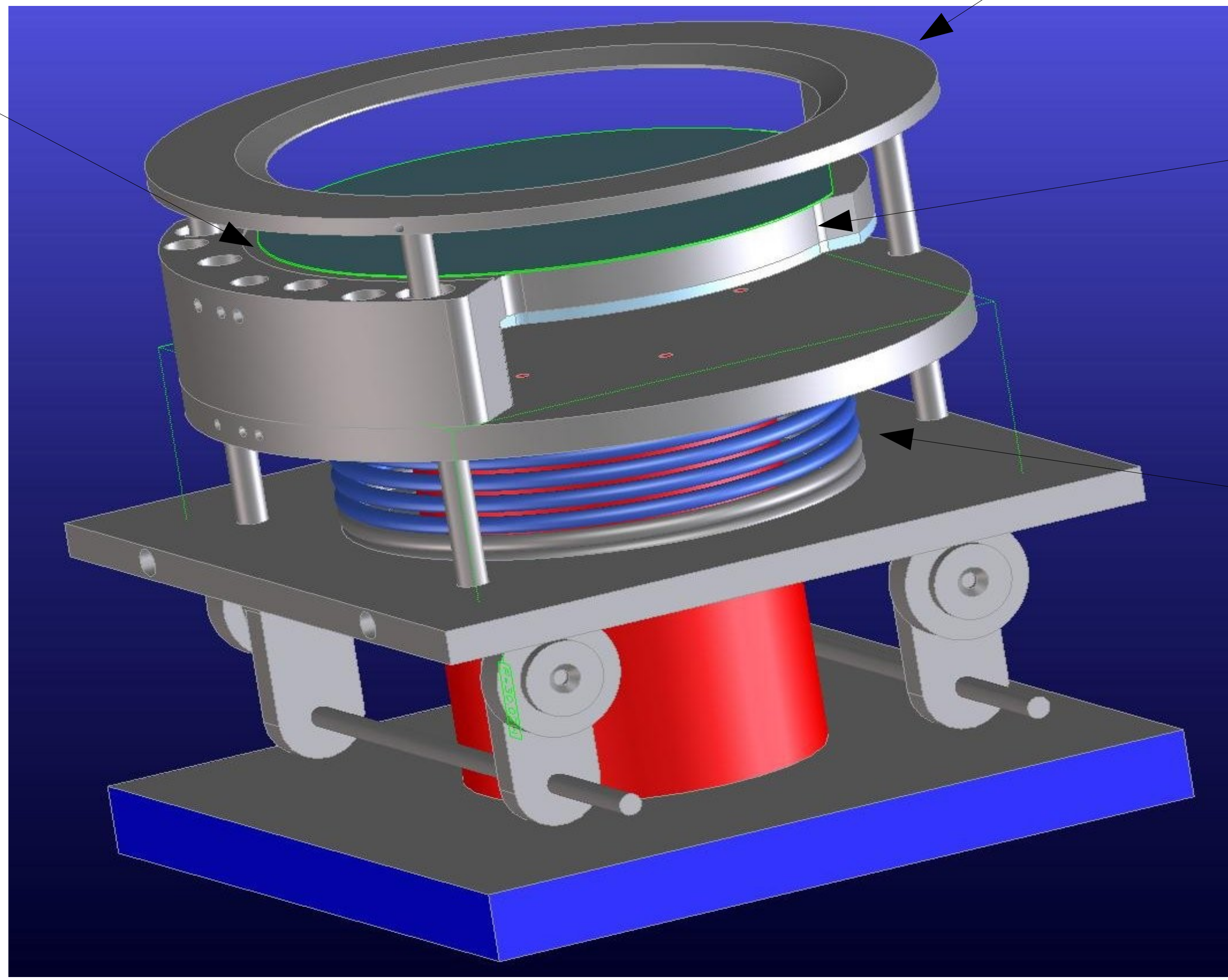
Mechanical clamp chuck new design



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Thank you

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Wärmekoppler

Unsere Leistungen liegen bei max 500 W/cm^2, aber tatsächlich werden wir zumindest 50W/cm^2 benötigen.
Also bräuchten wir etwa **0,5W/cm^2C°** um die Wafer unter 100 Grad zu halten.

Ohne Kopplung:	0,4 mW/cm^2C° bei 100 Grad Wafertemp.
Mit e-chuck ohne Gas:	100 mW/cm^2C° bei < 100 Grad Wafertemp
Mit Klemmchuck, domed platen und Gas:	1W/cm^2C° bei < 100 Grad Wafertemp
Mit Klemmchuck, open platen und Gas:	? W/cm^2C° bei < 100 Grad Wafertemp

Allerdings gibt Axcelis für den e-chuck bei -10°C Chucktemperatur eine Maximaldosis von 2E14 für < 80°C und 750W Beamleistung an. In der oberen Abschätzung ist ja keine Wärmekapazität des Wafers berücksichtigt.

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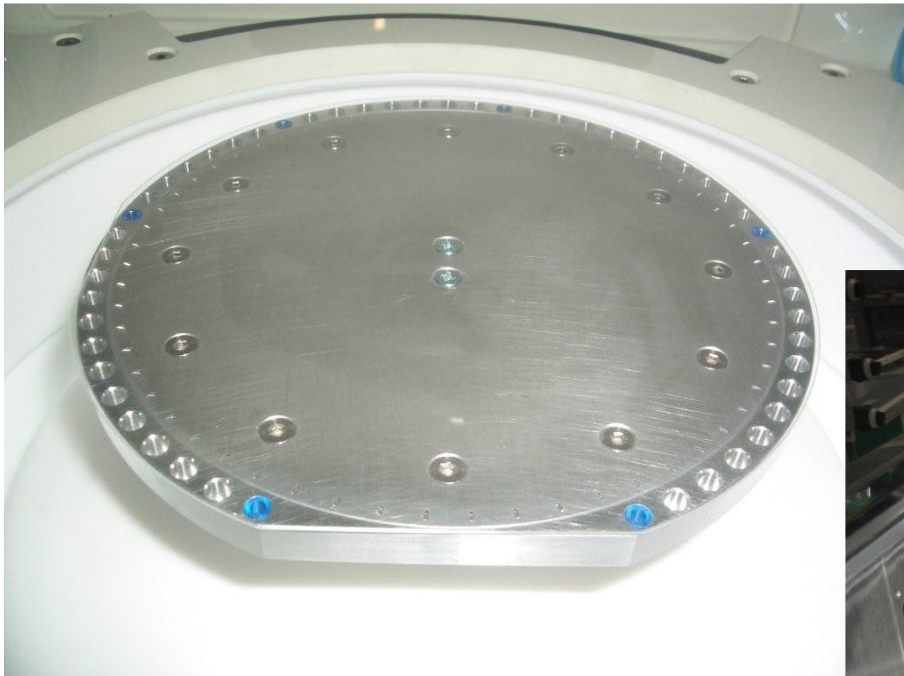
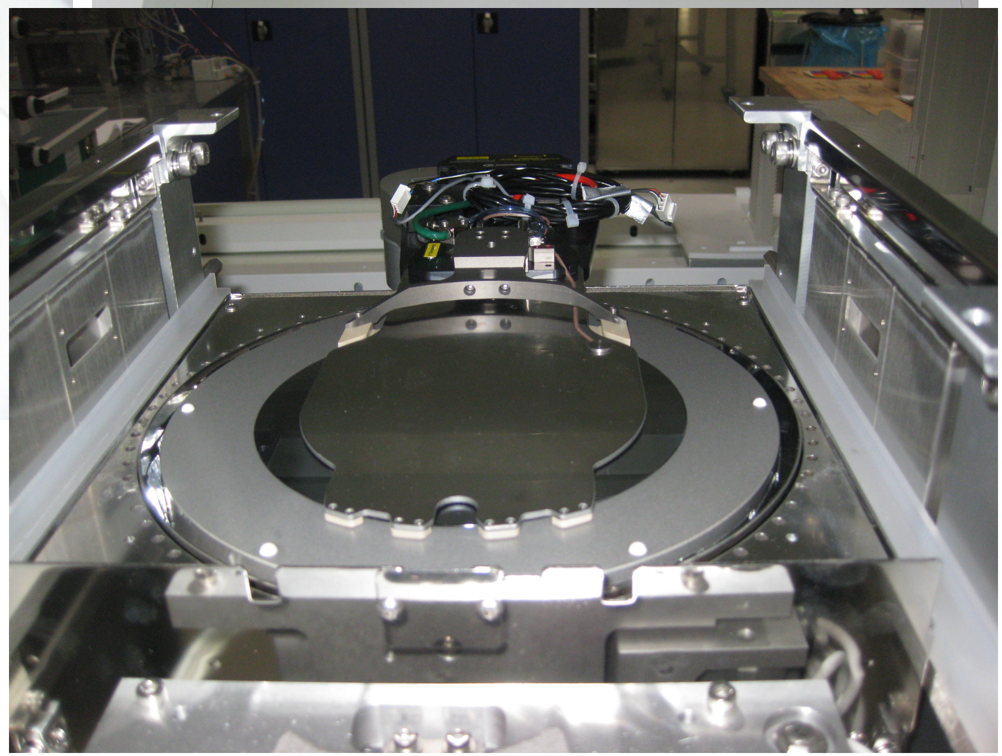
Ideas for a contactless photoresist coater/developer





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