

# Weekly PXD Meeting

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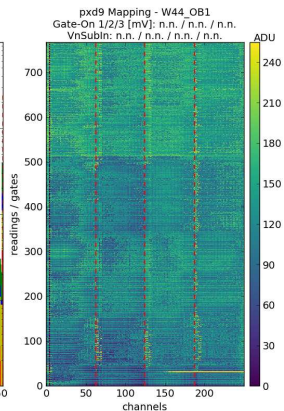
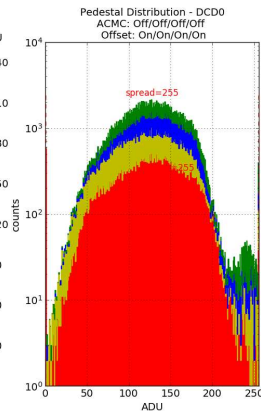
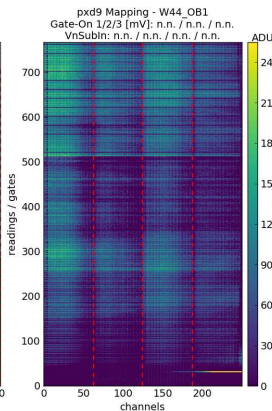
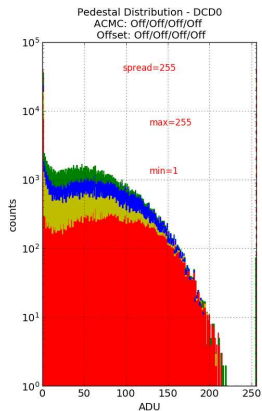


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Max-Planck-Institut für Physik  
(Werner-Heisenberg-Institut)

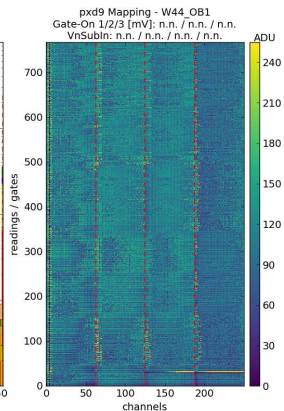
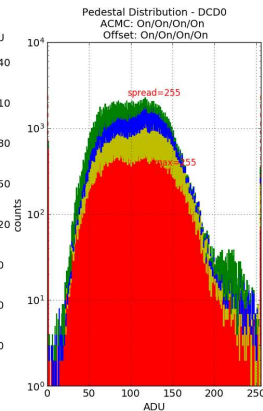
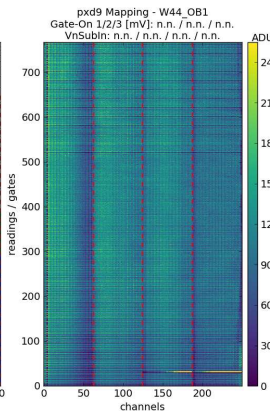
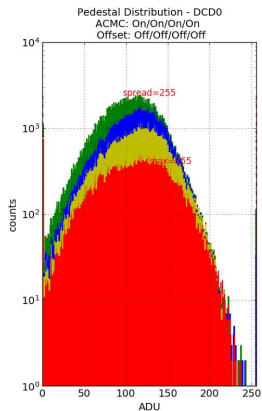
Offsets: off, ACMC: off

Offsets: on, ACMC: off



Offsets: off, ACMC: on

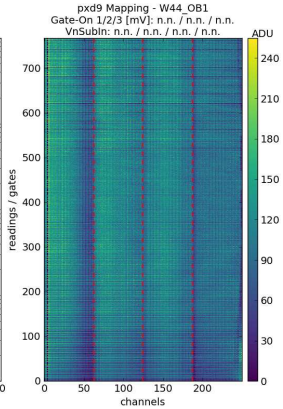
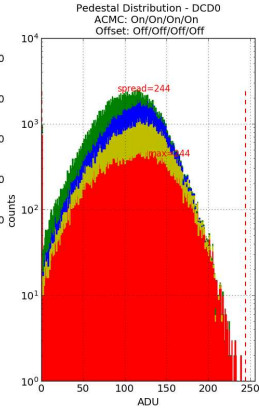
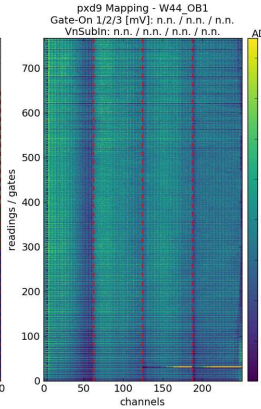
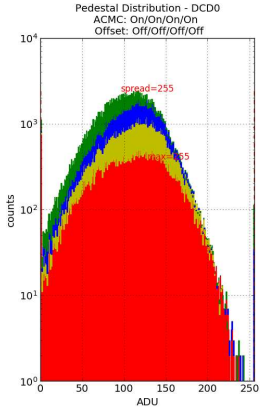
Offsets: on, ACMC: on





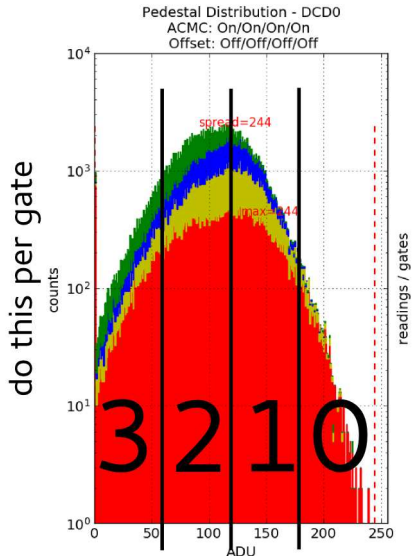
Offsets: off, APMC: on, clear-off: 3V

Offsets: off, APMC: on, clear-off: 5V



About 100 pixels are in saturation in row 30 and 31.  
Why does this effect appear as geometrical row instead of electrical gate?

Optimize the offsets gate-wise as the ACMC copes for the distribution between gates.



- turn on ACMC and move the pedestals as good as possible into the dynamic range
- take pedestals
- per gate: divide the distribution into 4 parts and assign offset values 3, 2, 1 and 0 to the parts
- make a sweep over IPDAC range to find the best value
- make a check that there are no pixel outside of the dynamic range with non logical offsets



## at MPP

- W32\_OB2 almost finished
- W45\_OB2 just started

## Modules packed for shipment to Göttingen

- W46\_OB1
- W09\_OB2
- W41\_OF1
- W32\_OF1

Still have to discuss details: when? where?