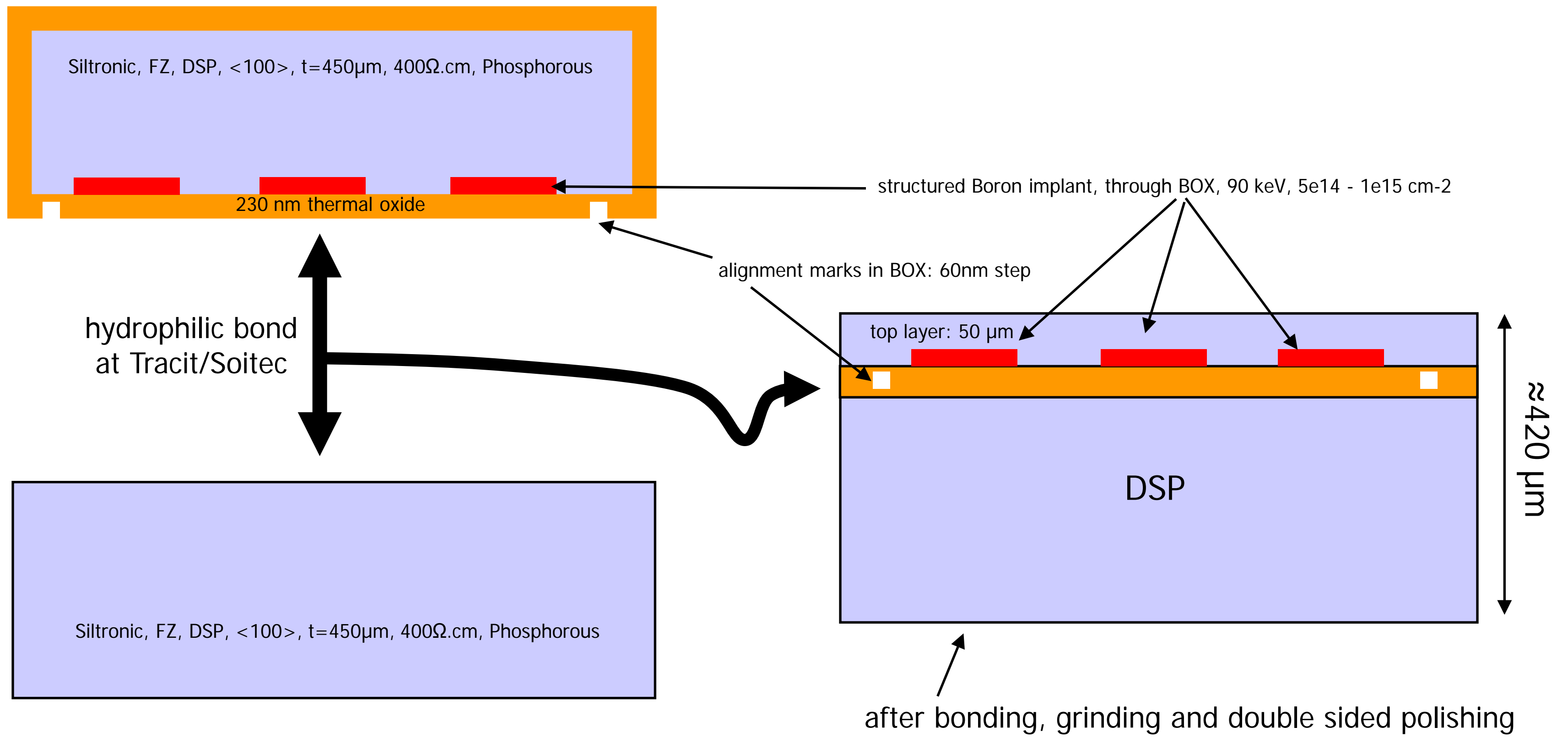
SOI Wafers ordered at Tracit/Soitec

-: top and handle wafer delivered by MPI
-: pre-processing of top wafer at MPI

-: 25 engineered BSOI wafers prepared at Tracit/Soitec
-: DSP, ≈ 420 μm overall thickness, 50 μm top layer



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The Issue…

March 26: after pre-processing at HLL 30+30 HLL wafers sent to Soitec for bonding and thinning

May 25: SOI Wafers back at HLL
-: 22 “prime” grade
-: 7 downgraded wafers with some scratches and TTV>2micron

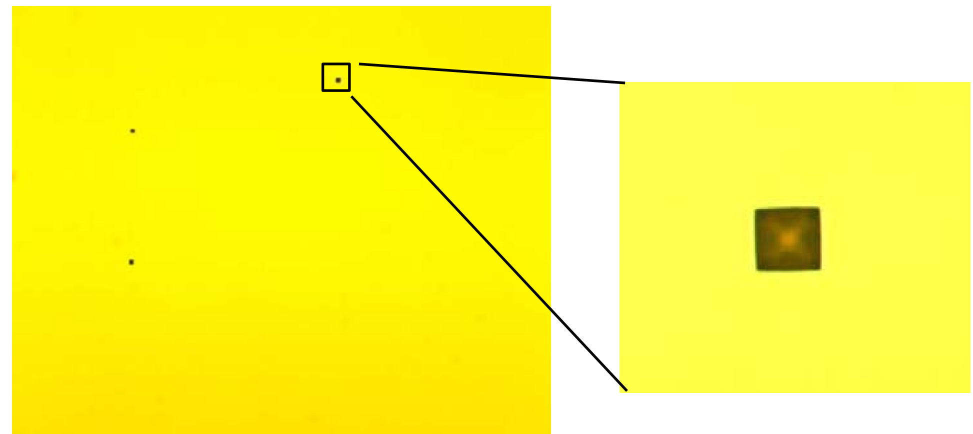
Incoming inspection:
-: some scratches seen even on “prime” wafers, handle side in general more affected
-: one larger scratch seen almost all of the top wafers
-: contamination level of top wafer “acceptable”!

→ start of processing at HLL
-: first oxidation
-: lithography with transfer of the alignment marks from BOX to handle wafer

Issue seen during back side photo resist coating:

-: pyramidal pits on the back side,
~20 micron lateral dim., ~ 15 micron deep

-: caused by:
1. pin holes in the screening oxide during front side thinning
2. Soitec simply “forgot” to grind back and polish the handle wafer.
Stack is still ~485 micron thick!



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After the re-work ….

July 24:

10 re-worked wafers sent back to HLL, 3 wafers were broken during repair

Incoming inspection:

1. Overall thickness now ~435 micron, 47 micron top layer
2. Top wafer surface mirror polished, almost no defects
3. Back side surface with a lot of (very shallow) scratches from back side grinding
4. Still one pit close to the wafer edge which was deeper than 50 micron before back grinding
5. **Small (~few microns) crystal dislocations, including slip lines, probably defects from the grinding procedure**

In Conclusion (as of today, August 4 …)

-: Re-work failed!!!

-: Scratches at the back side as well as the single "pit" at the wafer edge could be acceptable, but

-: Crystal defects are much more of concern than the fear about the contaminations in the original pits!

How to proceed?

-: The original (imperfect) wafers are now back from the first implantation and waiting for the first Nitride deposition. Since the wafer after re-work seem to be worse than before, try to continue with the original ones.

-: We are looking for a way to analyse the contaminations in the pits. This is not easy since we have to find a way to probe into the pits!!! Some options still under discussion …

On the other hand: We are looking at a contamination level (and with the detection limit) of 10^{10} at/cm^2, the area of a typical pit is ~$1.5*10^{-6}$ cm^2, assuming that the entire area within the pit could be detected and that we have in the order of 100 pits/cm^2, metal contaminations hidden in the pit will be only detectable, if they exceed 10^{14} at/cm^2. Below that they are invisible … we have to discuss internally, whether something invisible can still contaminate the process line

-: The issue is still under discussion and the processing is in hold during the summer break at HLL. Decision to be taken on August 24.

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