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HEIDELBERG

Switcher-B

Design Update

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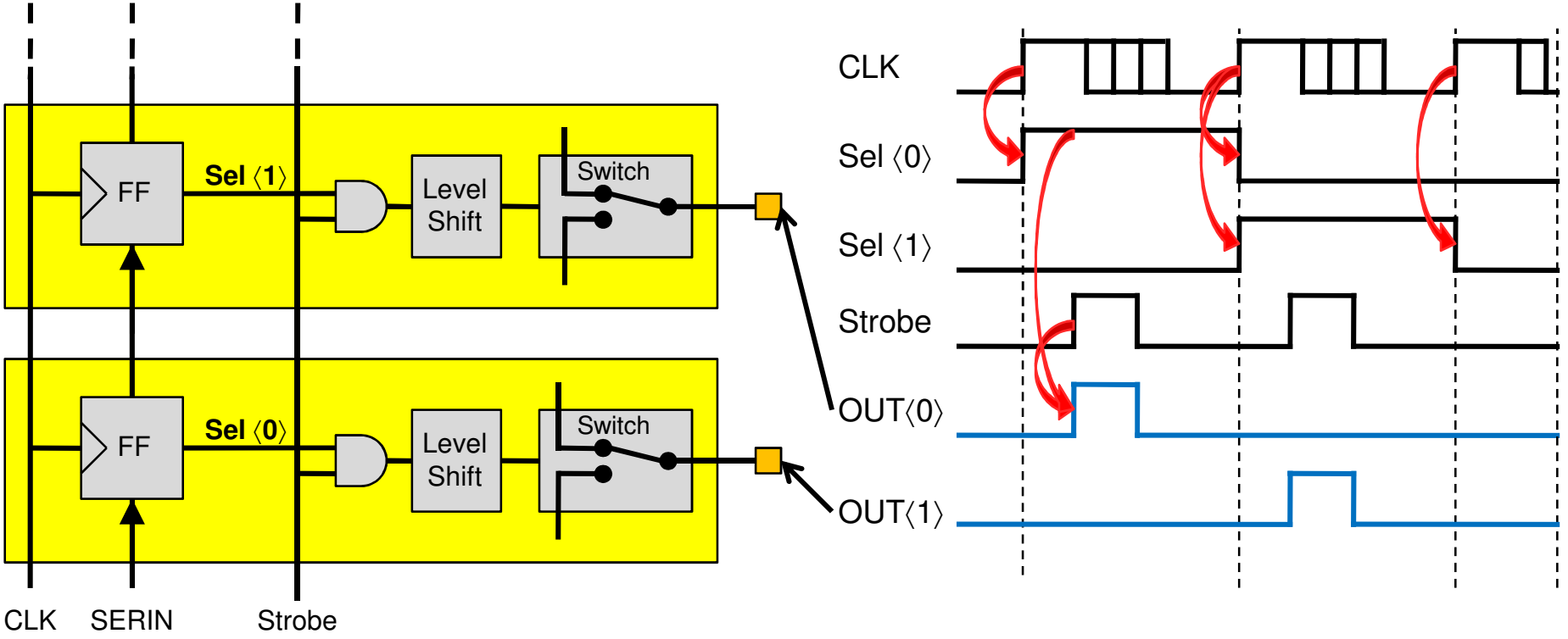
Timing of OLD Shift Register Readout



- Output = Sel⟨i⟩ AND Strobe → signals on neighbors cannot overlap
- Note: Can turn on 2 rows by injecting 2 ones in shift register
- BUT: - Some overlap may be wanted (for speed @ gates)
  - May want to skip rows (interleaved readout mode)

Proposed NEW Timing

- 3 Modes:

  1. Rising Edge (of Strobe for selected ch.) SETS output
     NEXT RISING edge (DEselected ch.) CLEARS output

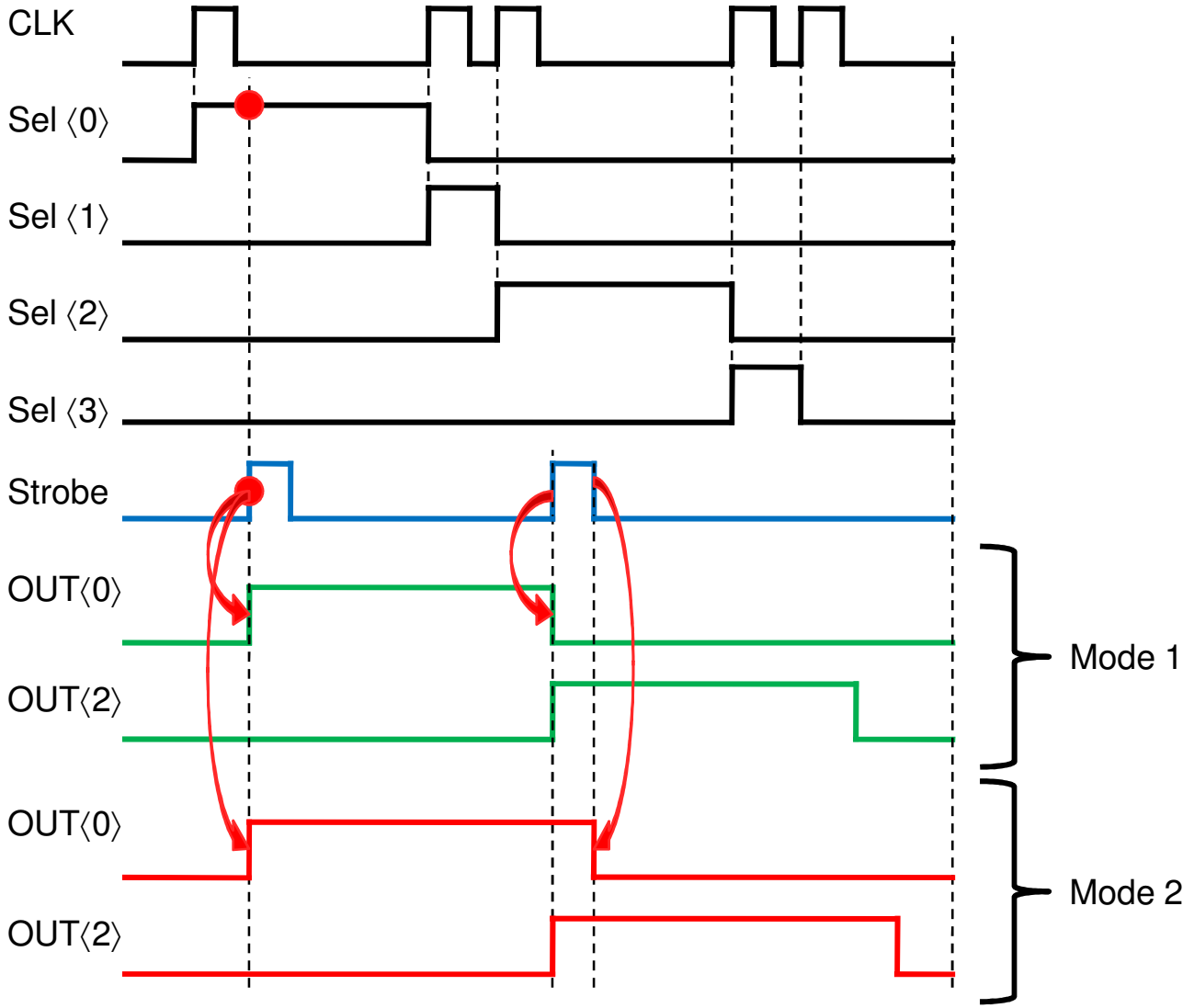
  2. Rising Edge SETS output
     NEXT FALLING edge CLEARS output

  3. Same as before (for Clear)

- Another possible Mode:

  4. SELECT SETS output
     RISING edge of Strobe CLEARS

Proposed New Timing (with channel skip)



New Timing Discussion

- Advantages:
  - Can skip channels
  - Can produce overlap

- Limitation:
  - Cannot produce an output ‘a little bit wider’ than sel (minimum width = sel + strobe)
    This is possible in solution (4), but there, timing is determined by two signals (ShiftClock, Strobe) instead of one.

- **Consequences for Control signals:**
  - **Must be able to inject 2 Ones in shift register (2 active rows)**
  - **Must be able to have asymmetric clocks**
  - **Must be able to fine-adjust Strobe timing**
  - **(if 4 is used): Relative timing of ShiftClock & Strobe critical**

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Other Circuit Modifications

- Switcher-B will use HV Switch from Switcher-4
  - High voltage swing
  - No risk of exceeding voltage limits of devices
  - Slower. Need quite large devices to drive 50 pF
- Level Shift will use AC coupling as in Switcher 3
  - No DC power
  - Faster
  - SEU risk small, maybe use Monoflop characteristic
- Internal additional voltages (required in drive circuit)will be generated by Bandgap Reference
- JTAG Interface will use External low voltage supply from DHP (1.8V) + Level shifter

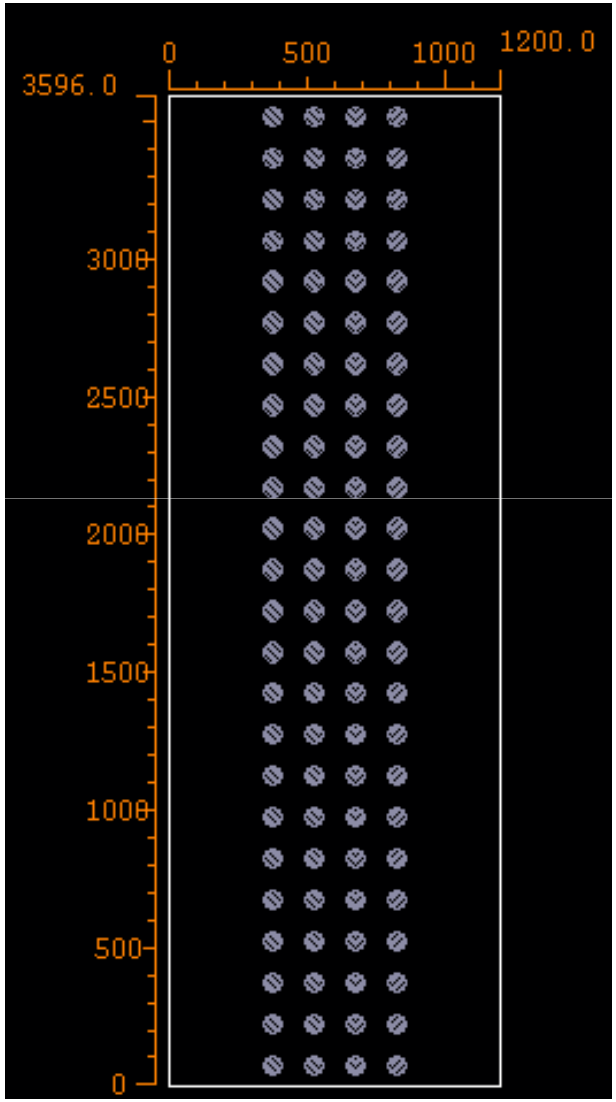
Circuit Status / Schedule

- New Enable Circuit:
  - Simple Circuit has been found & simulated, using only NOR gates
- JTAG Interface is under way. Quite some work, as we do not have rad. Hard Lib for synthesis.
  - Do interface by hand OR
  - Make a small library (← preferred)
- Simple Verilog Code is ready
- Bandgap Schematic done, Simulation very promising
- AC Coupling schematic done
- Schedule:
  - Next MPWs: 10.8 (Europractice) and 17.8 (AMS) – too early
  - 2.11 → 8.1. back – safe

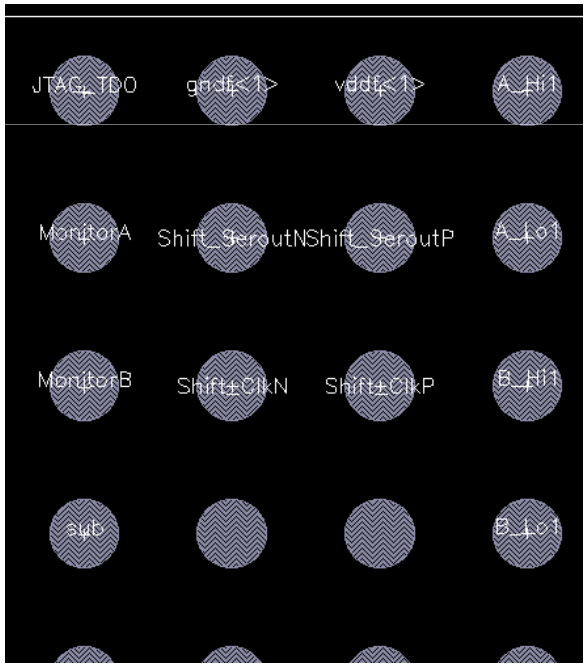
Pins / Signals

Signal	Type	Pins	Traces	Function
CLK	LVDS	2	2	Shift Clock
Serin	LVDS	2	2	
Serout	LVDS	2	-	
Strobes	LVDS	2 + 2	2 + 2	
Vddd, gndd	Floating Supply	2 × 2	2	
Vhi / Vlo	Switch Voltages	4 × 2	4	
Sub	Lowest voltage	1	1	
Monitor	Optional	1	1	
JTAG IO	CMOS	4	4	TCK, TMS, TDI, TDO
JTAG_VDD	JTAG IO Supply	1	1	
Sum		29	20	

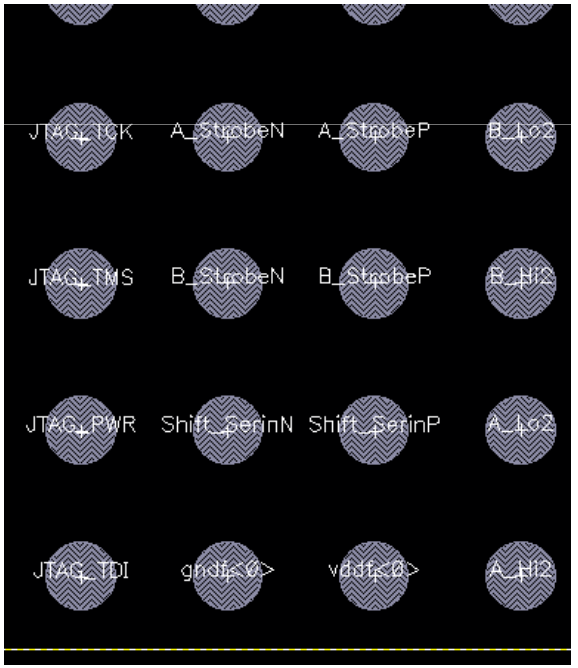
Chip Geometry



- Geometry is unchanged:
  - 32 channels, each for GATE and CLEAR
  - 3.6mm × (1.2mm + x)
  - Bump pitch 150µm × 150µm
  - Chip has 4 × 24 pins, (top/bot 4 × 4 for control)



Top

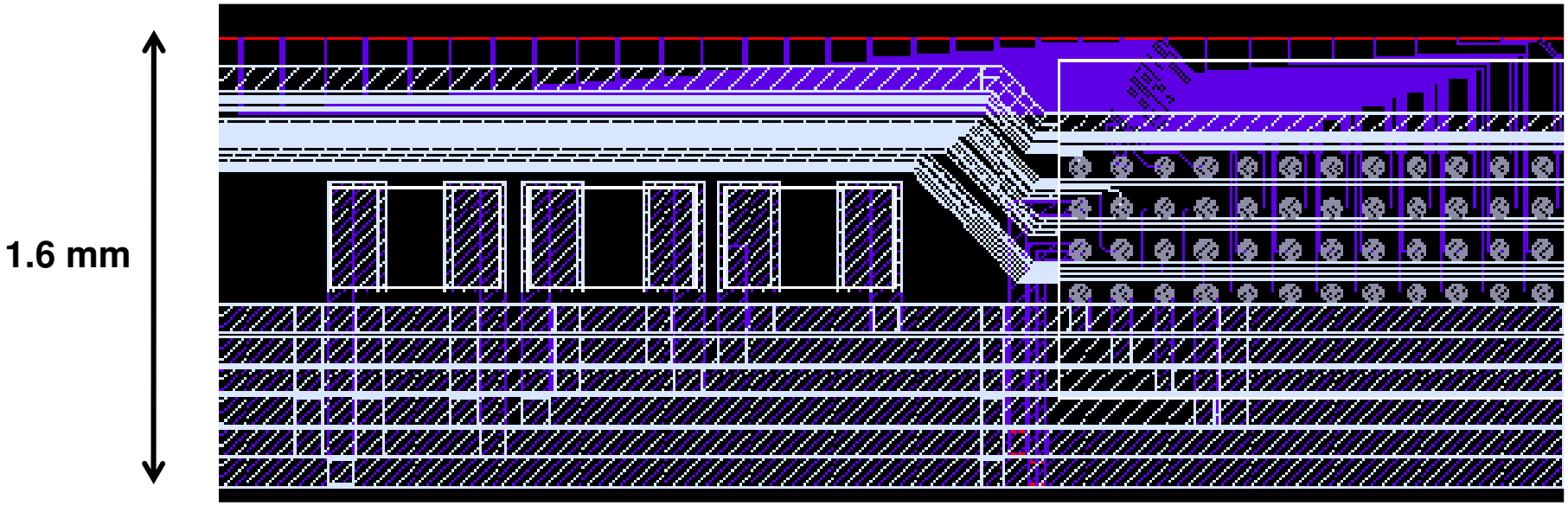


Bottom

Balcony Layout

- Christian has established a full DRC and LVS rule file for the HLL Technology

- He has finished the layout of the module side
  - 1.6mm Wide
  - 2 metal levels required
  - Estimated delay bottom – top ~ 1ns



Thank you