UNIVERSITÄT
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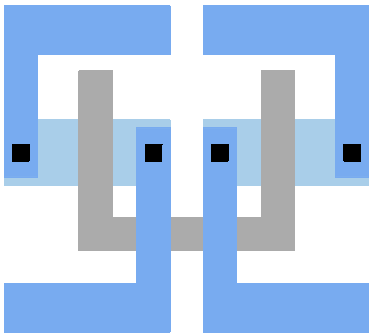
Switcher and DCD Status



Christian Kreidl
Ivan Peric
Peter Fischer

christian.kreidl@ziti.uni-heidelberg.de

Belle 2 PXD

EVO-Meeting

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Switcher

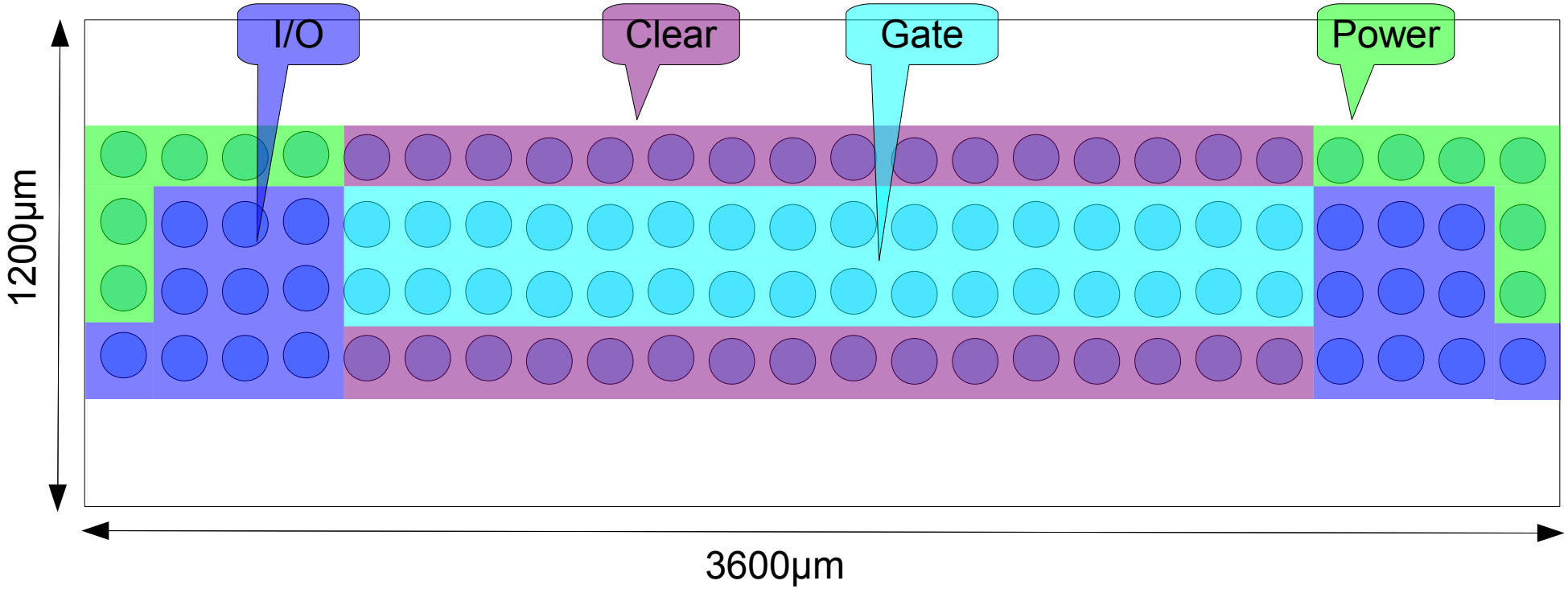
Switcher-B Summary

- AMS 0.35µm high voltage technology
  - 1200µm x 3600µm chip size
  - 150µm bump pitch, 70µm Al-pads
  - 96 pads (32 Gate, 32 Clear, 14 Power, 16 I/O)
  - solder bumps or under bump metallization not available for miniasic
- 32 channels (DEPFET rows)
  - each channel has two outputs (Gate, Clear)
  - max 20V swing
  - GateHi, GateLo, ClearHi, ClearLo Power Inputs
  - channel selected sequencially with shift register
  - outputs of channel controlled by strobe signals
  - shift registers of neighboring chips can be daisy chained
  - shift clk, serin, serout, strobes are LVDS signals
  - build-in decoupling of Clear and Gate to DEPFET-source potential
  - capacitive coupling of control and output stage to reduce static power

Switcher-B Summary

- LVDS
  - uses 3.3V digital supply
  - configurable termination resistor and output current
- JTAG interface
  - testing and configuration of chip
  - uses 1.8V supply from DHP
  - configuration bits are triplicated and secured with majority voter
  - SEU can be detected by reading back registers

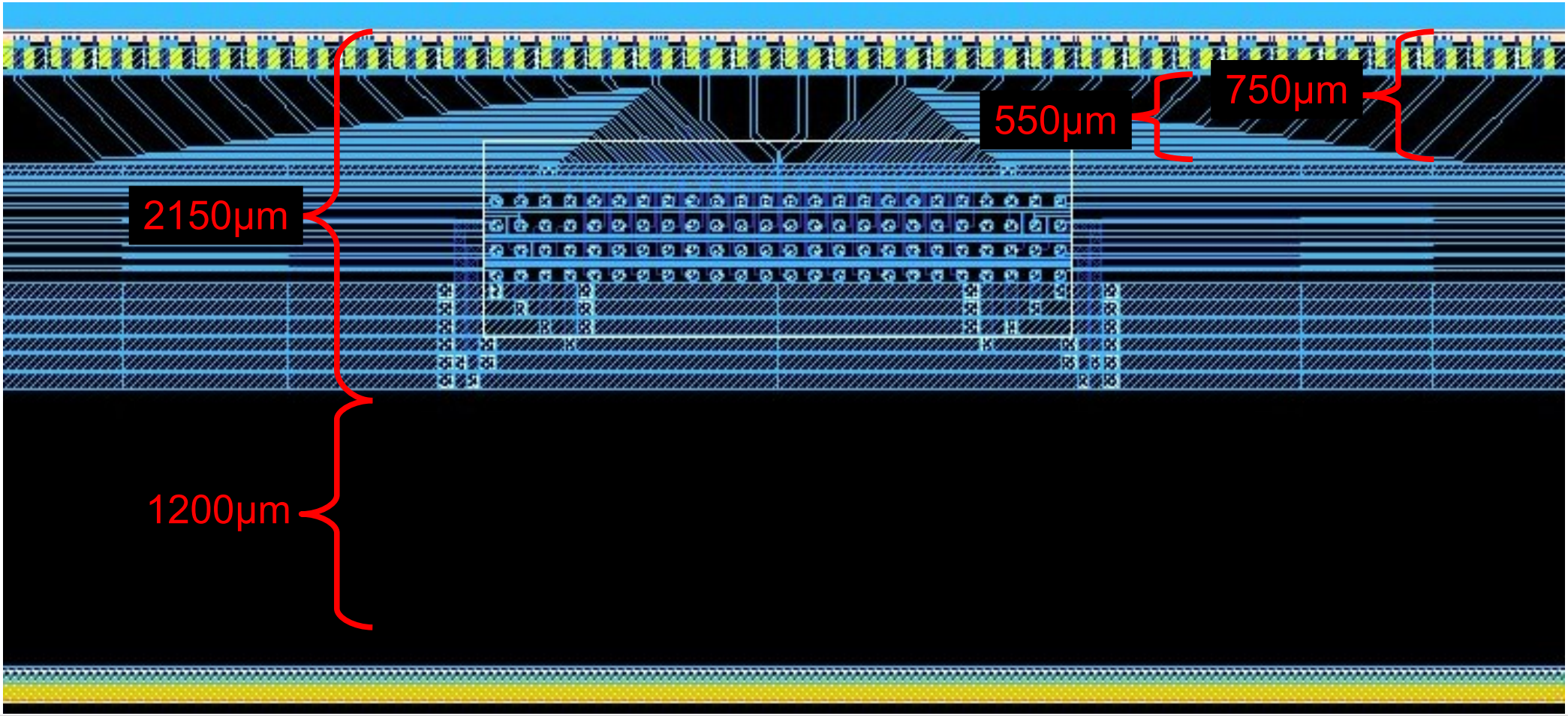
Switcher-B Pad functionality



Switcher Bump Pad Layout

Switcher Balcony PXD6

- both metal layer used in parallel to reduce R where possible
- PXD6 design will use free space for power busses
- balcony design fits in 2mm final module by shrinking power bus
  - 3rd metal layer (copper) will be available to reduce R

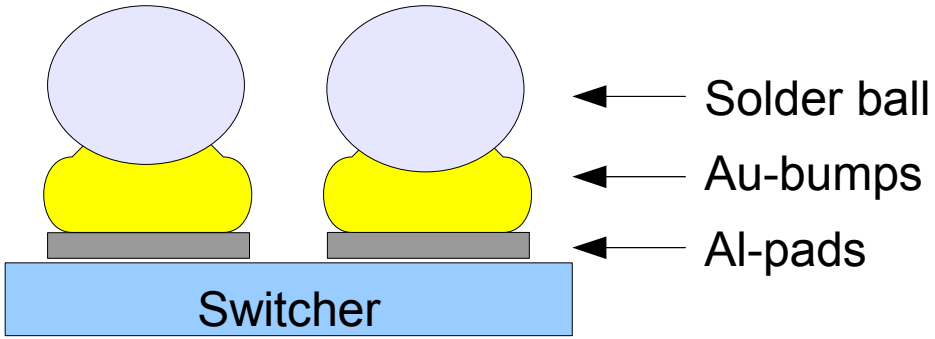


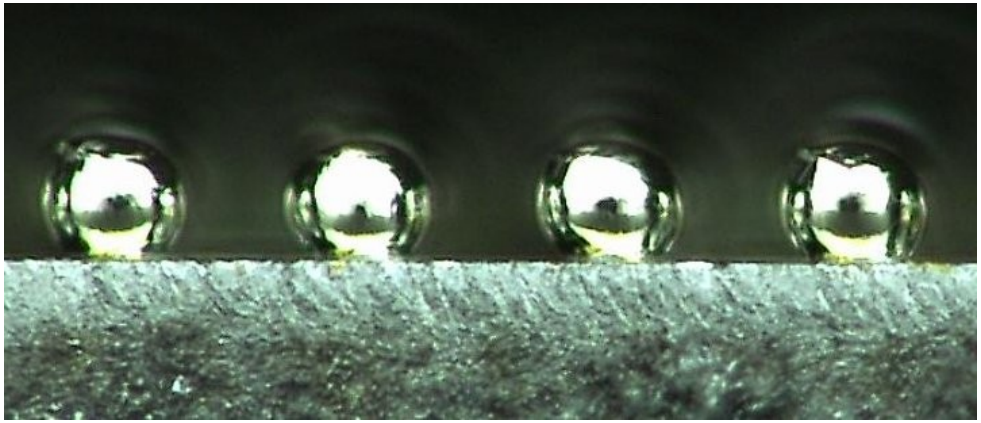
R + C

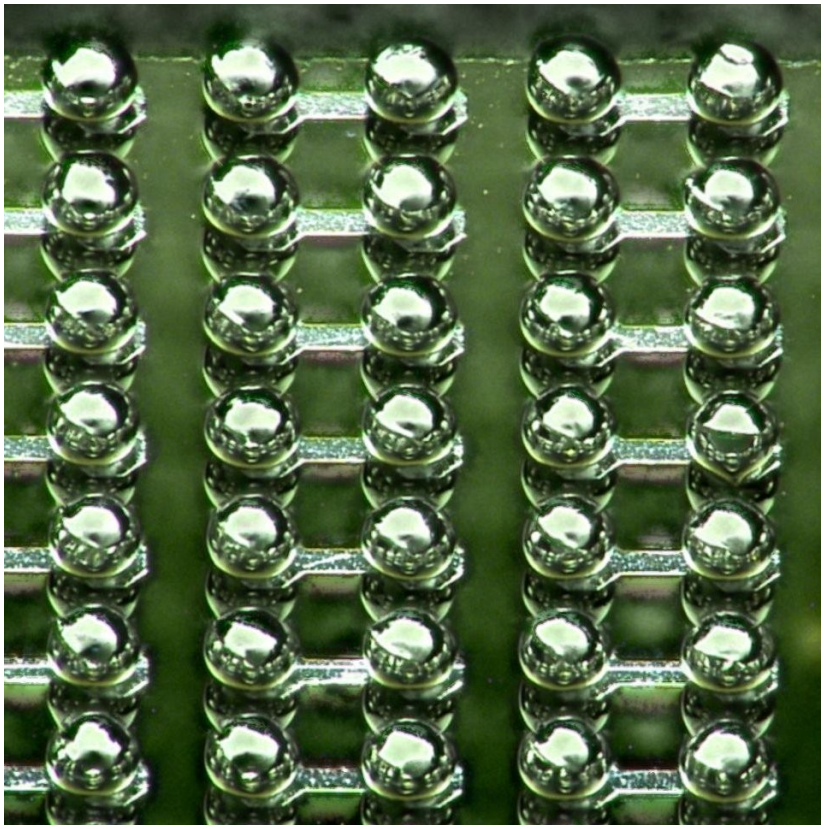
- rough estimation calculated
  - more detailed simulation and extraction ongoing
- worst case on longest PXD6 module (Z100 type)
- control busses
  - ~5cm length
  - 2 metal layers parallel where possible
  - tRC= ~3.6ns
- fanout from switcher to matrix
  - longest line ~6.2mm
  - 2 metal layer, 3rd metal not available due to small trace width
  - adds ~8pF to matrix capacitance
  - tRC = ~830ps (10% ↔ 90%) for 58pF
- power bus
  - ~5cm length
  - PXD6: 300µm width, 2 metal layer, 15mΩ/sq: 2,5Ω
  - final module: 75µm width, 3 metal layer, 3,75mΩ/sq: 2,5Ω

Bumping

- commercial solder bumping not available for switcher
- use coined gold studs as under bump metallization
- place solder bumps ontop using PacTec technology
  - 55µm placed ball diameter



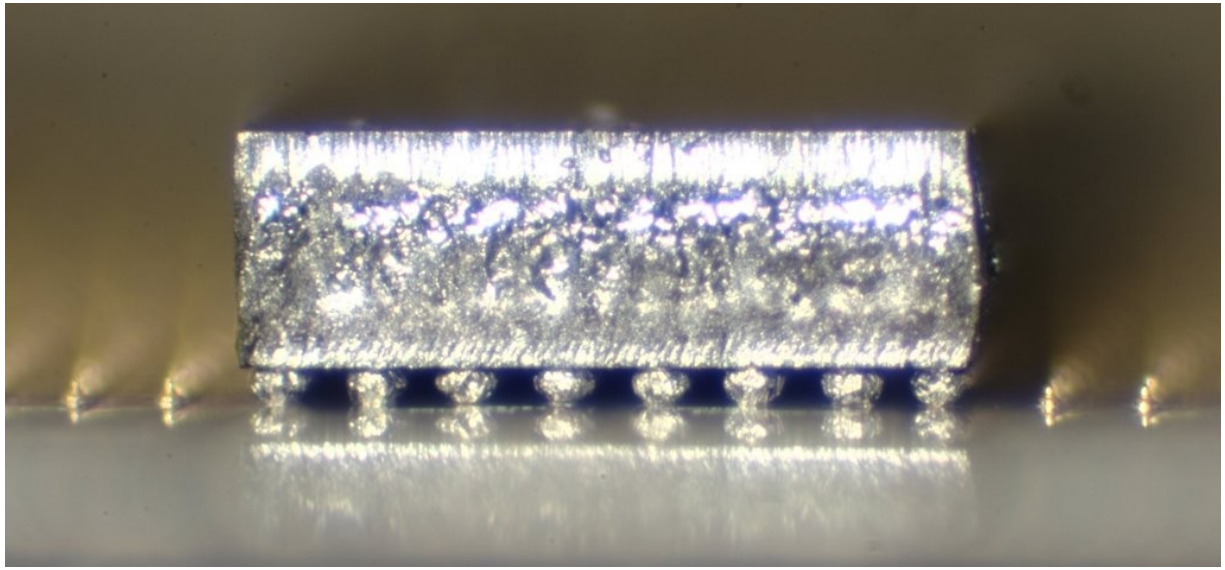




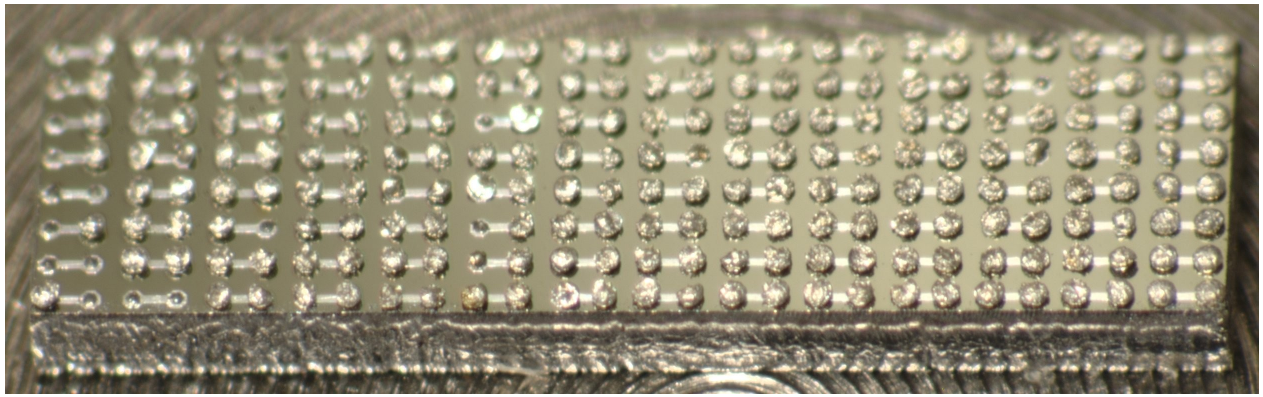
side and top view of dummy chip with PacTec solder ball placed ontop of coined gold bumps

PacTec solder bumping

- send some samples with coined gold bumps to PacTec
- received solder balled samples
- successfully soldered
- successfully desoldered



side view of one soldered chip on a tripple substrate

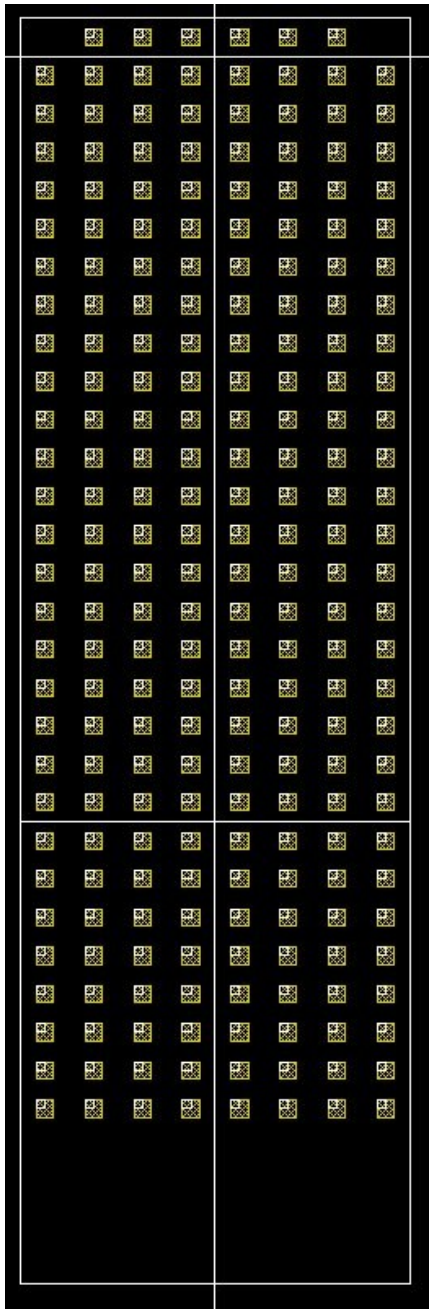


top view of an desoldered chip

DCD

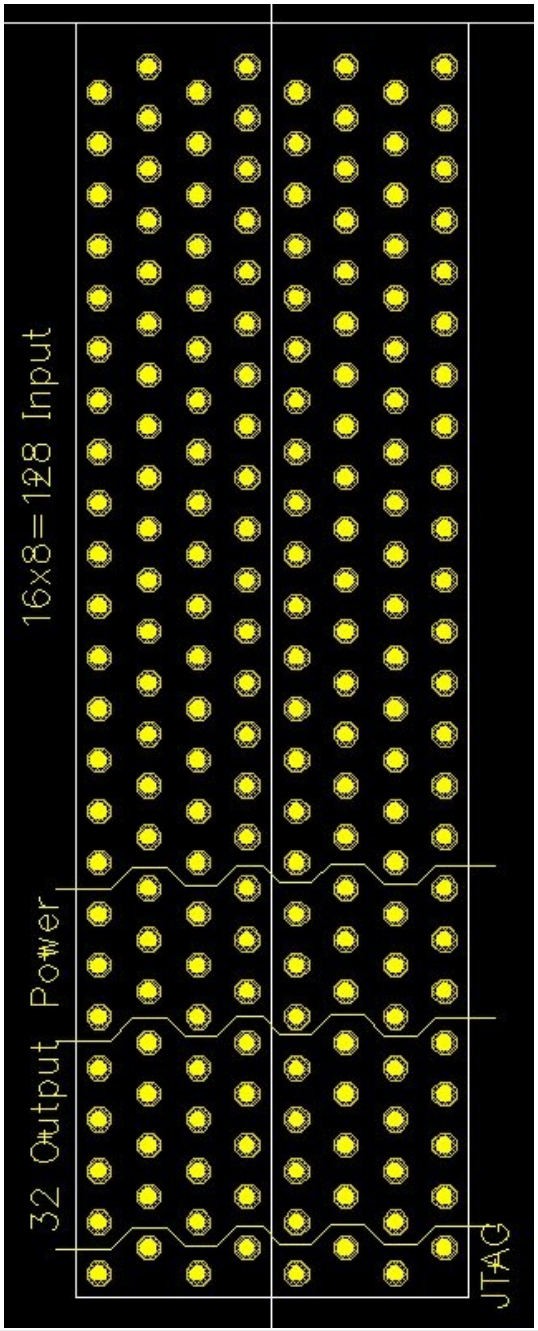
DCD geometry

- received the design rules for commercial solder bumping of DCD
  - 200µm bump pitch, 140µm gap
  - bumping subcontractor
  - no force when bumping: electronics below pad ok
- current DCD geometry
  - 1x3 size miniasic (1525µm x 5000µm)
  - UMC 0.18µm technology
  - 160 Inputs, 190µm pitch in x, 150µm in y
    - 5 DCD for PXD6
    - 7 DCD for final design (1000 drains)
- not suitable for bumping by UMC



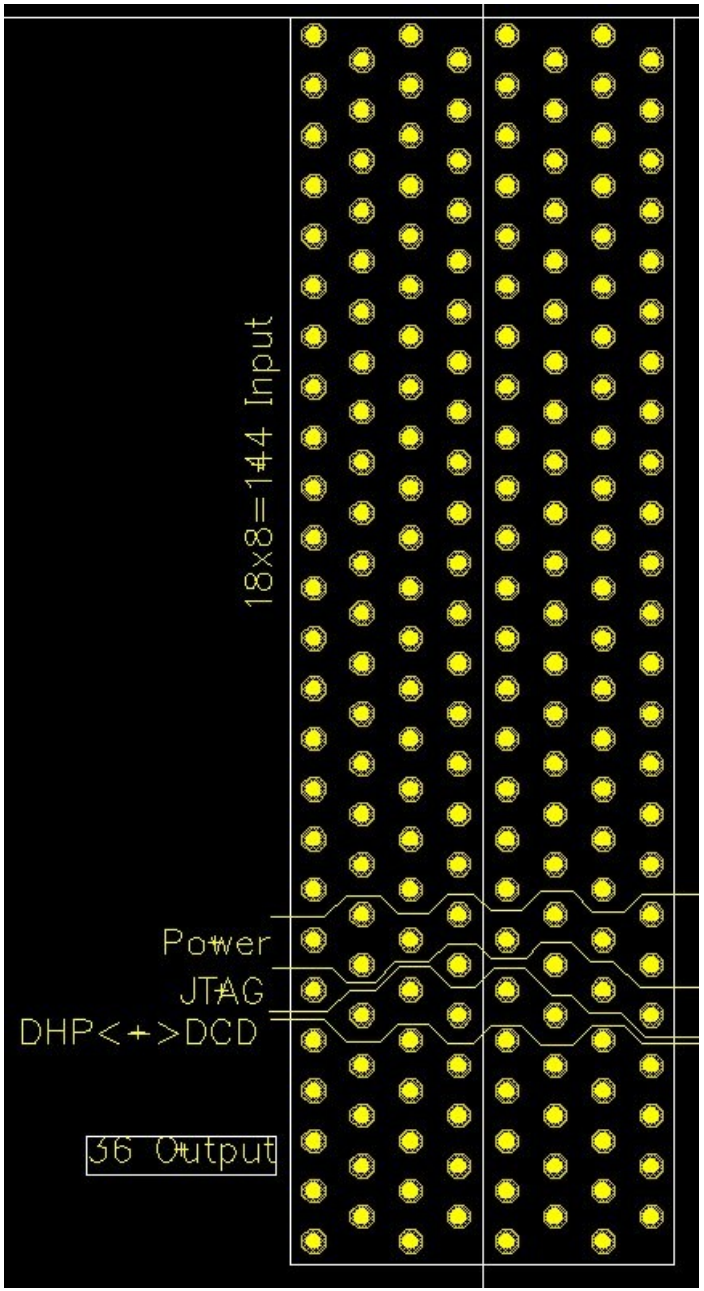
DCD solderball goemetry

- 1x3 size with UMC solderbumps
  - DRC clean bump layout
  - 128 Inputs only
    - 6 DCD for PXD6
    - 8 DCD for final design (1000 drains)
  - too few pads for power and control signals
  - space on module wasted by gap between chips



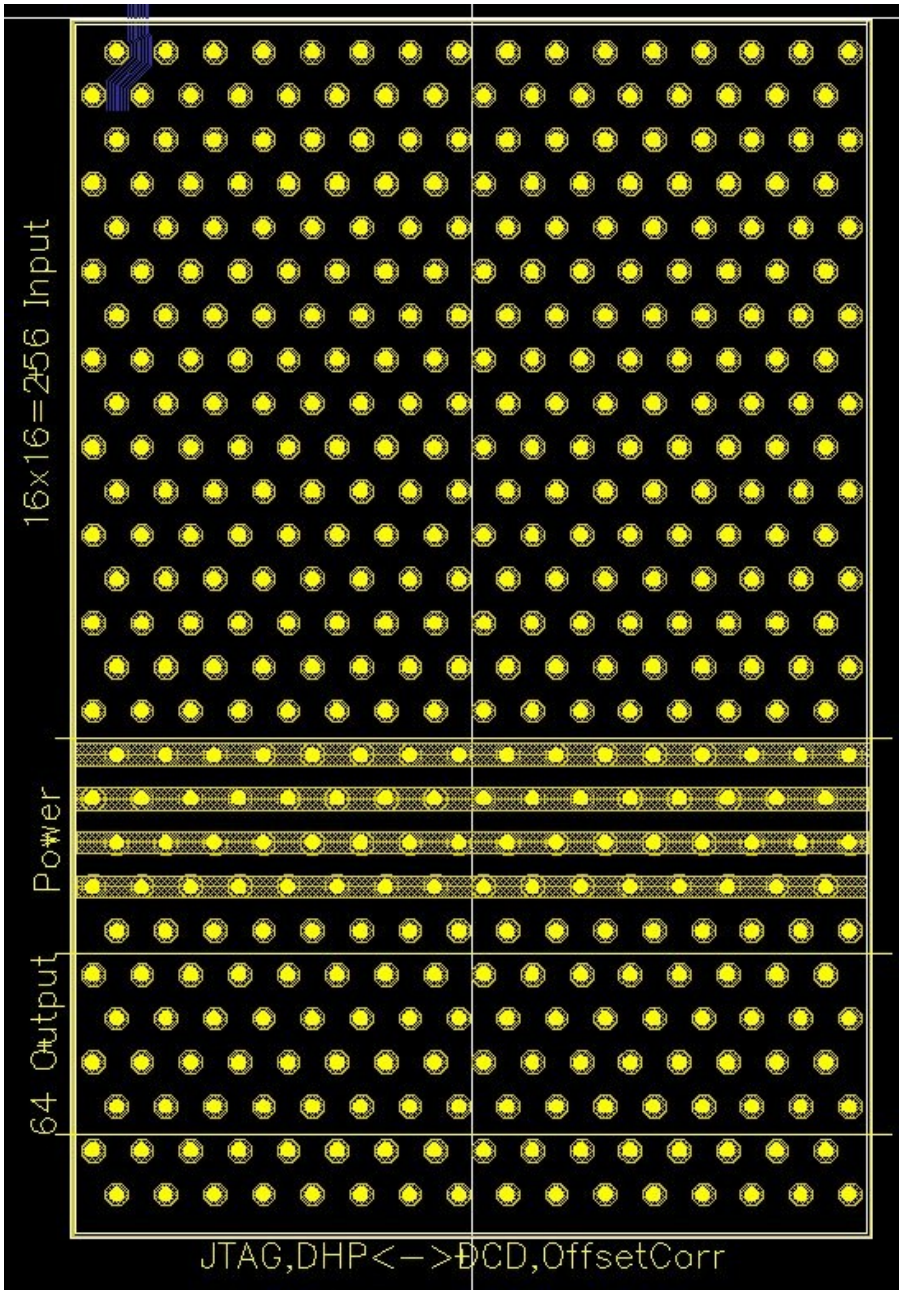
DCD solderball goemetry

- 1x3 size with UMC solderbumps
  - 144 Inputs
    - 6 DCD for PXD6
    - 7 DCD for final design (1000 drains)
      - 1 DCD less
  - DRC violated by 1µm per bump
    - problem with solder reflow?
    - should not be problem for under bump metallization chemistry
    - question: get chips with UBM only and place solderballs with PacTec machine?
      - likely not possible, because MPW runs are not flexible
  - even less pads for power and control signals then previous 128 input design

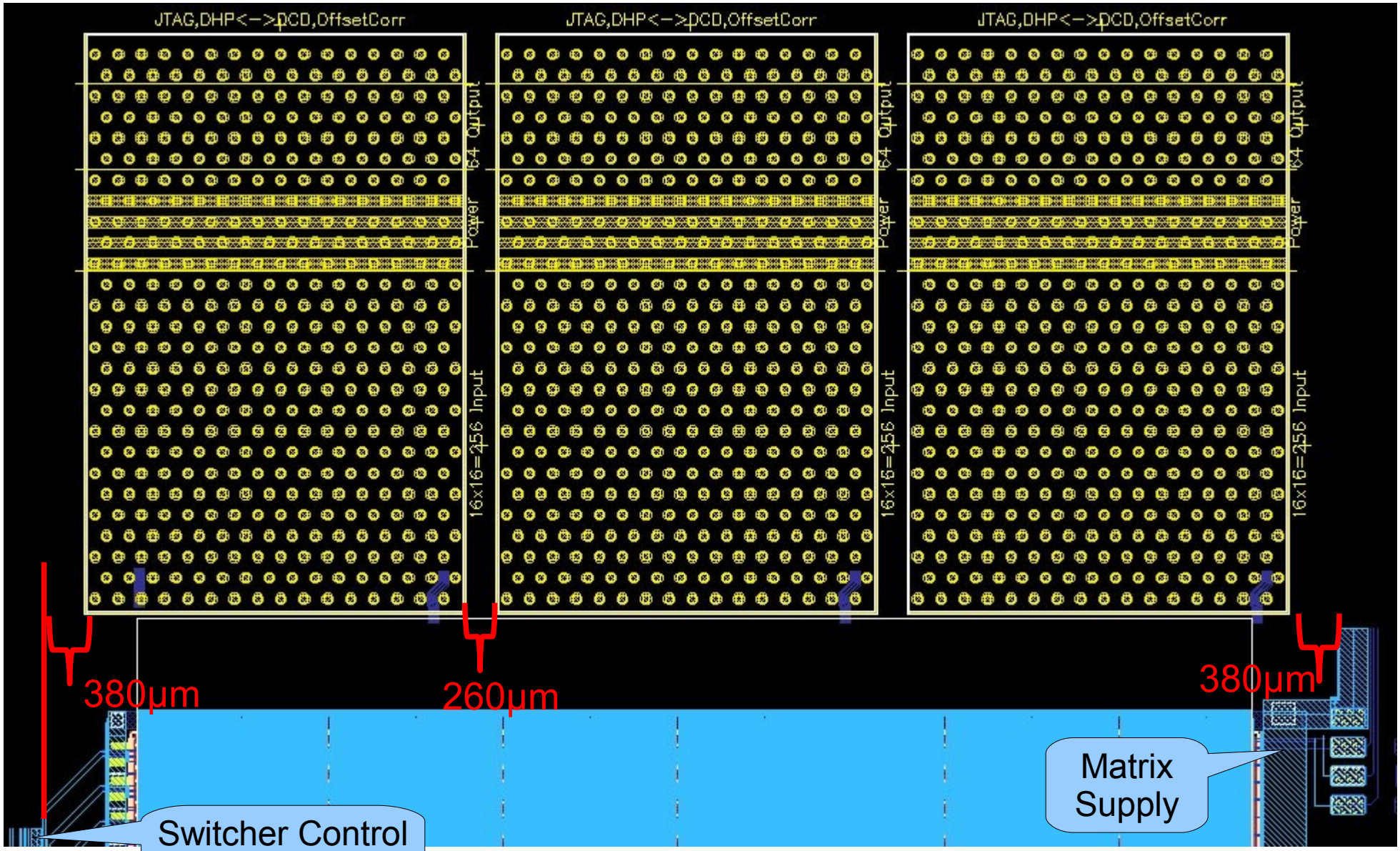


proposed DCD geometry

- new geometry proposal
  - 2x3 miniasic: 3280µm x 5000µm chip size
  - bump pitch: 200µm in x, 180µm in y (staggered), DRC clean design
  - 7th metal layer available for connecting bump pads to input cells
    - 6th metal layer free: routing and wide power busses → low voltage drop
  - 256 Inputs
    - 3 DCD for PXD6
    - 4 DCD for final design (1000 drains)
  - input cell size: 200µm x 130µm
    - gain space for onchip decoupling or offset correction memory
    - lower voltage drop across cell array
  - plenty of pads for power and control



proposed DCD at PXD6 Array



proposed DCD at final module

- 4 DCDs
  - 3280µm design width
  - cutting edge: 55-65µm
  - gap between chips >200µm
  - space needed: 13720µm
- active area 12500µm width
- 1220µm wider than active area: 610µm left and right
  - left side ok: 750µm space between active and switcher control busses
  - right side:
    - ~350µm occupied for matrix supply (Source, Bias), could be smaller with copper layer
    - 470µm needed for the right DCD if chips are left-aligned
- Increase active area by 6 colunms to use all DCD channels?
  - 4 DCDs x 256 Inputs = 1024 possible drains

Thank you!