HALBLEITERLABOR DER MAX-PLANCK-GESELLSCHAFT

Low noise measurements

of EDET structures with SPIX setup

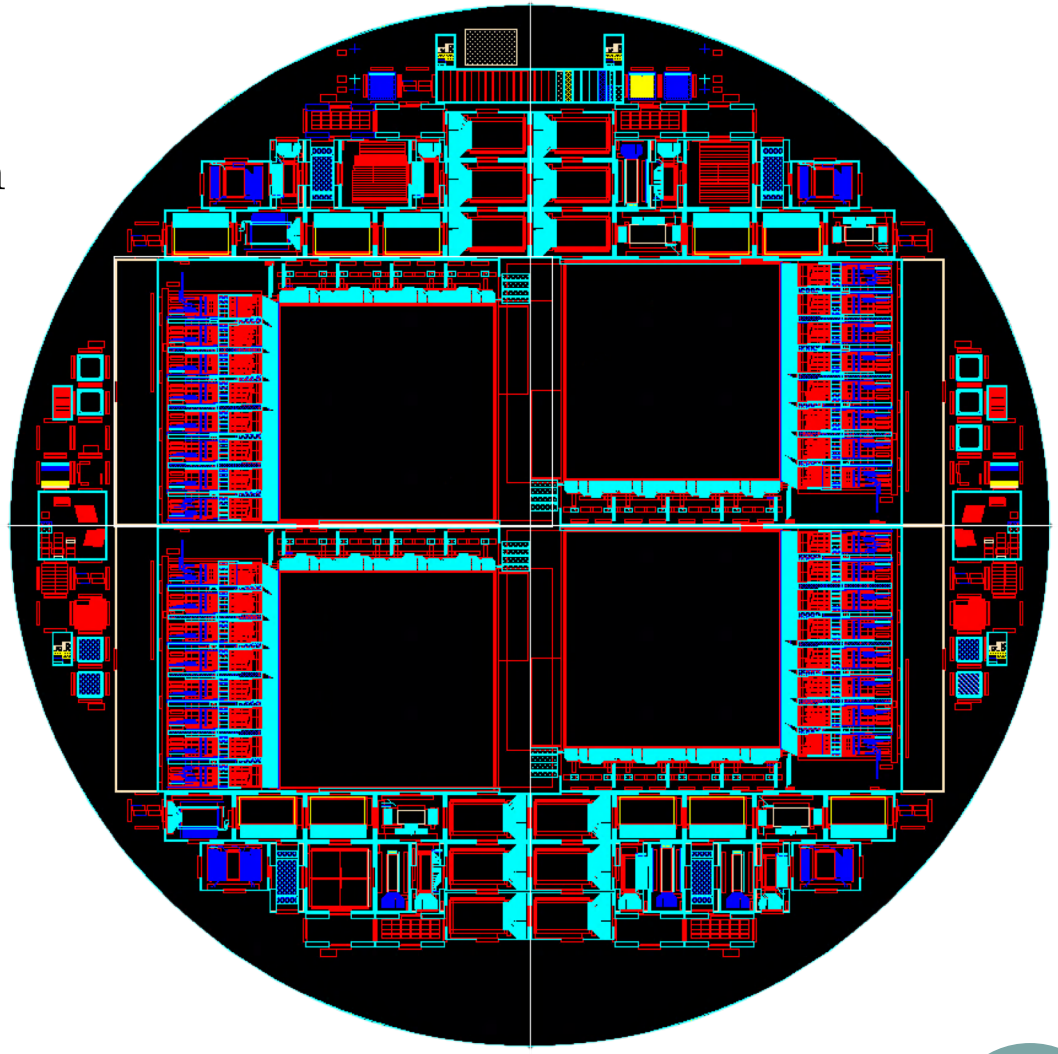
22nd International Workshop on DePFET
Detectors and Applications

10/04/2018

Mitja Predikaka

EDET production

- 4 WAFERS
  - W09 – 50 μm
  - W10 – 30 μm
  - W11 and W12 – 450 μm
- BIG MATRICES
  - 4 per wafer
- SMALL MATRICES
  - loads per wafer
- SINGLE PIXEL DEVICES
  - 4 + 2 per wafer



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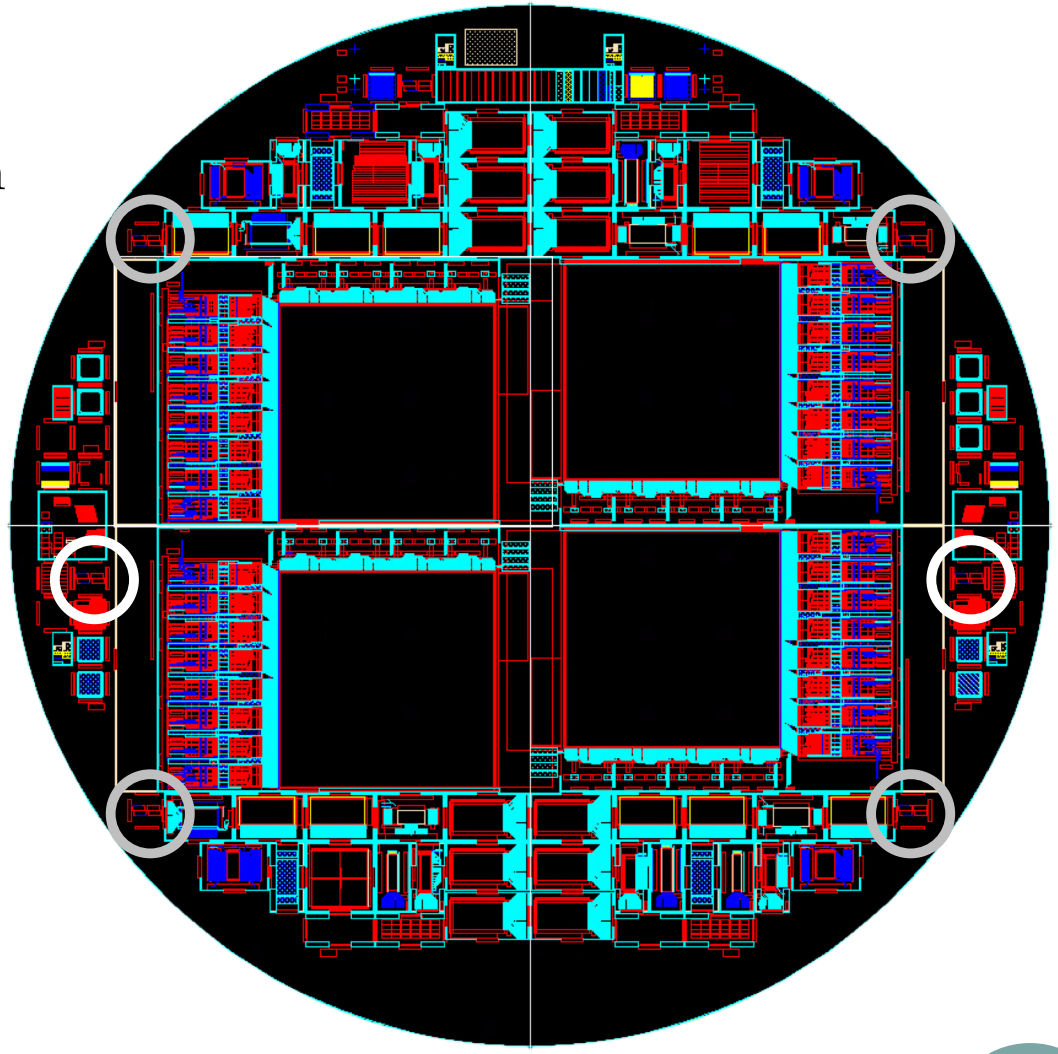

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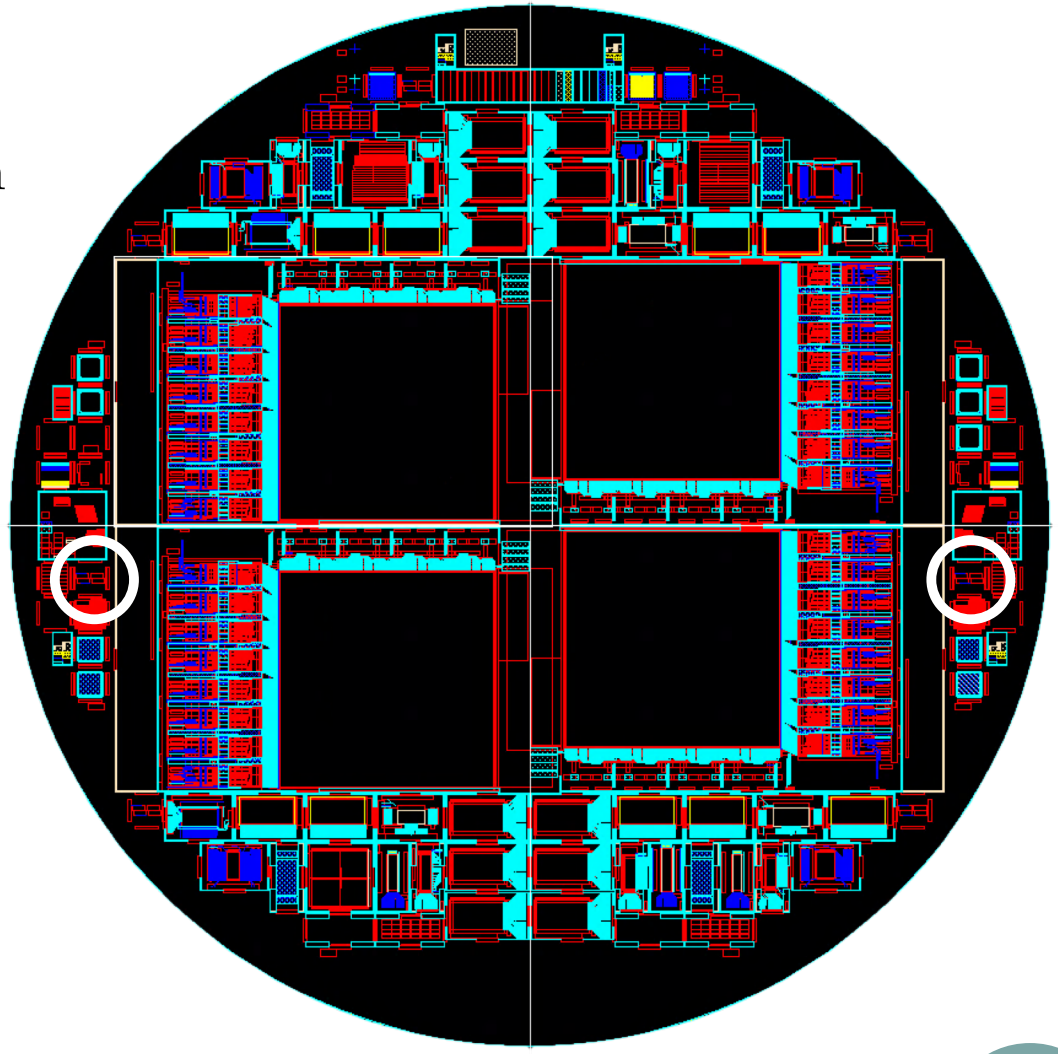

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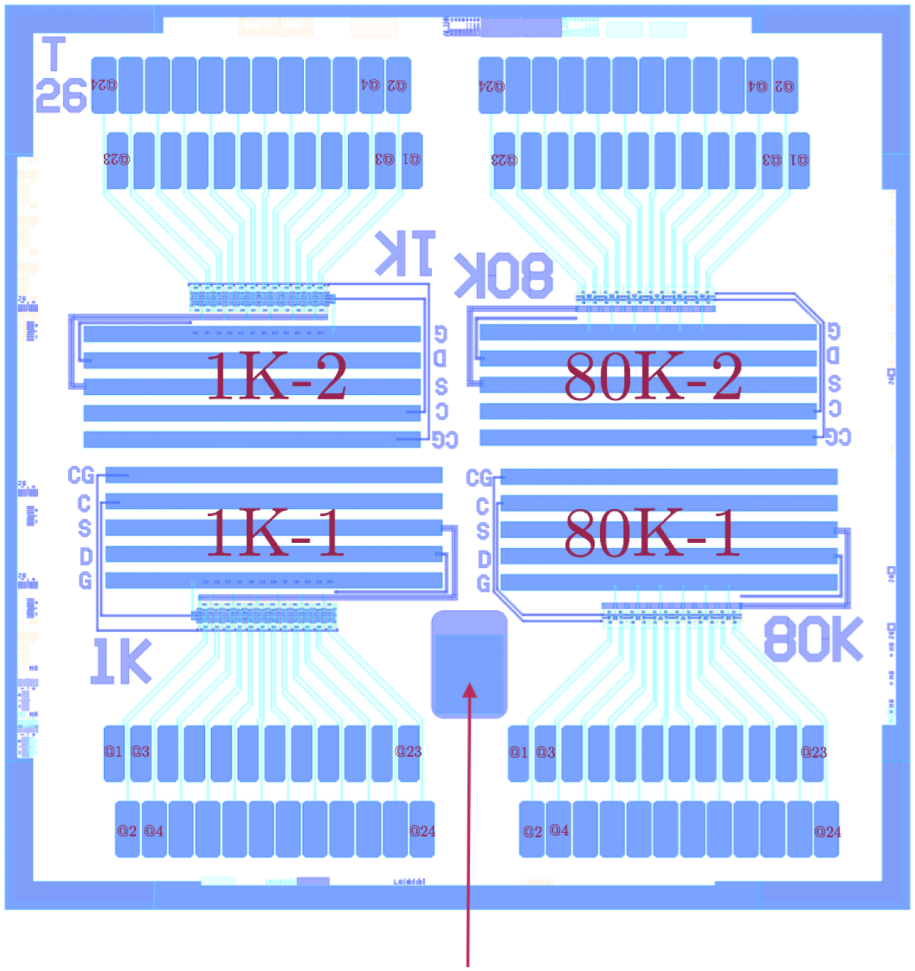

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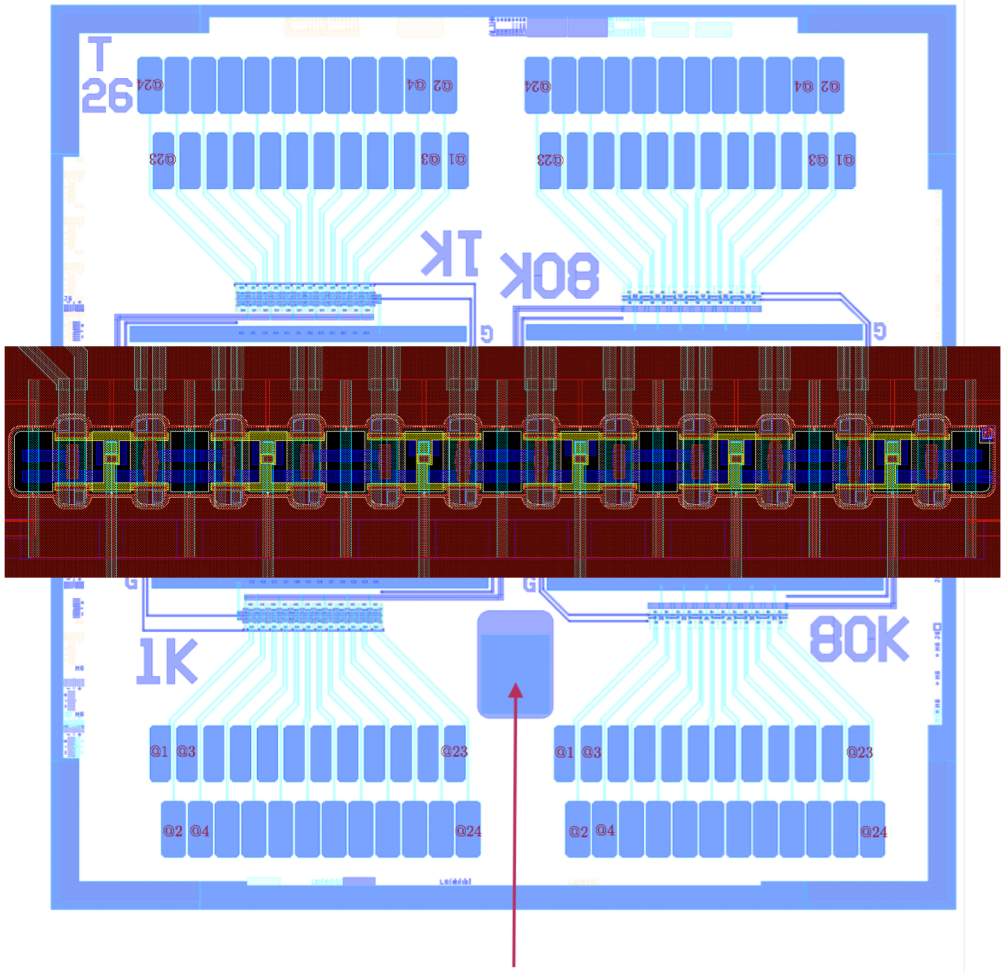

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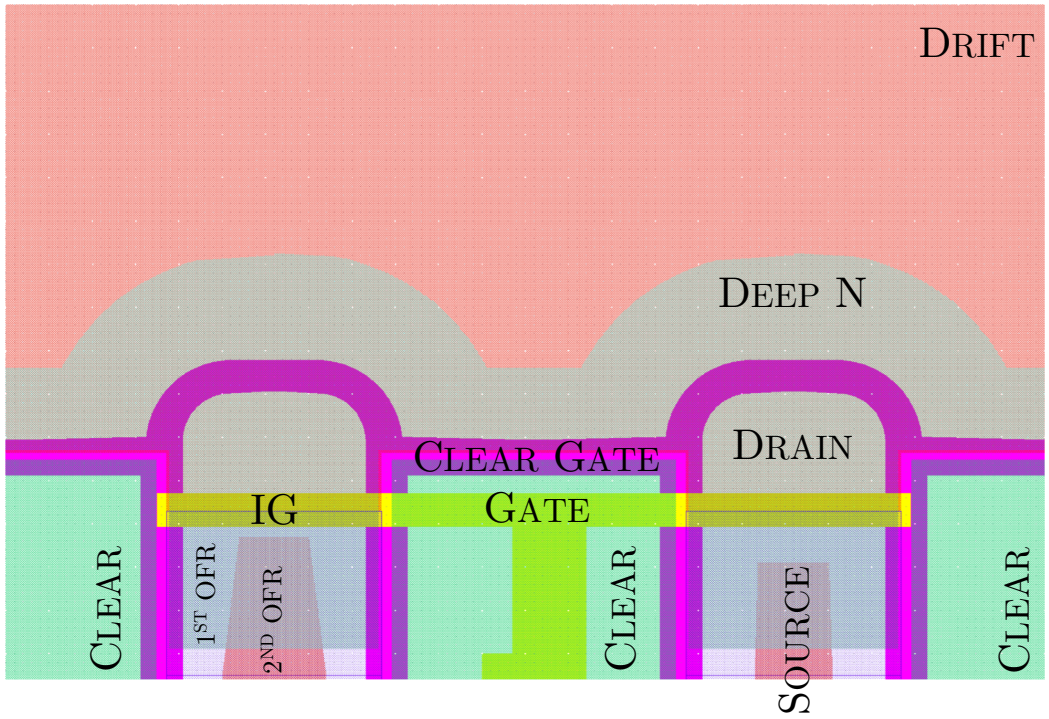
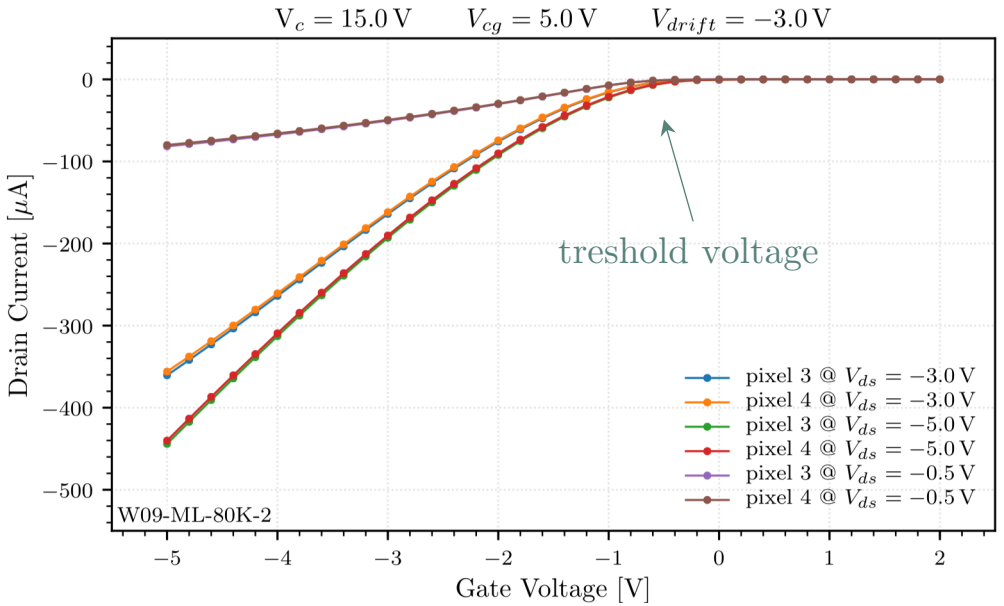


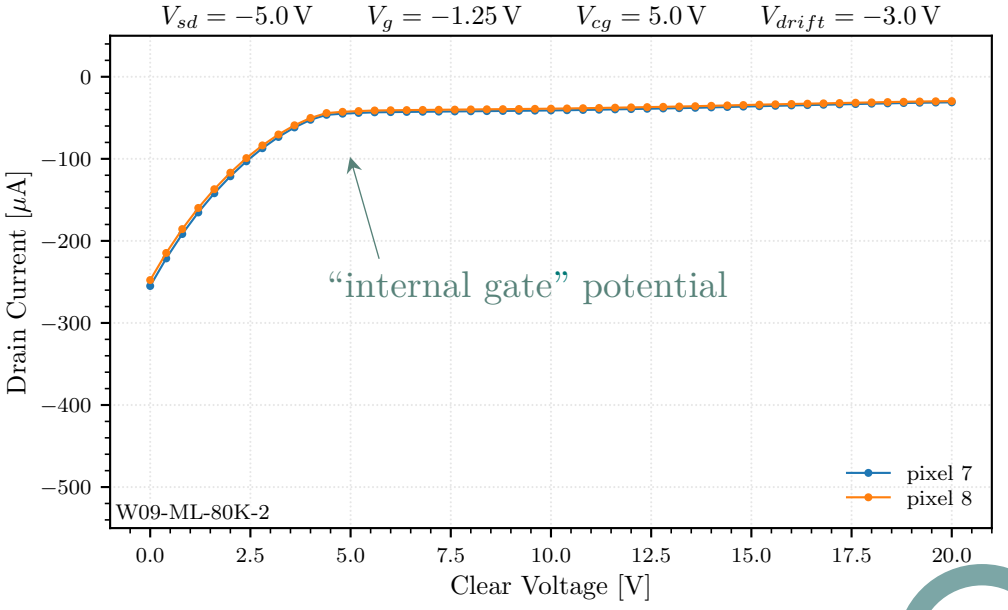
INTERNAL GATE is under the GATE
1ST OVERFLOW REGION is around the SOURCE
2ND OVERFLOW REGION is under the SOURCE

Static measurements

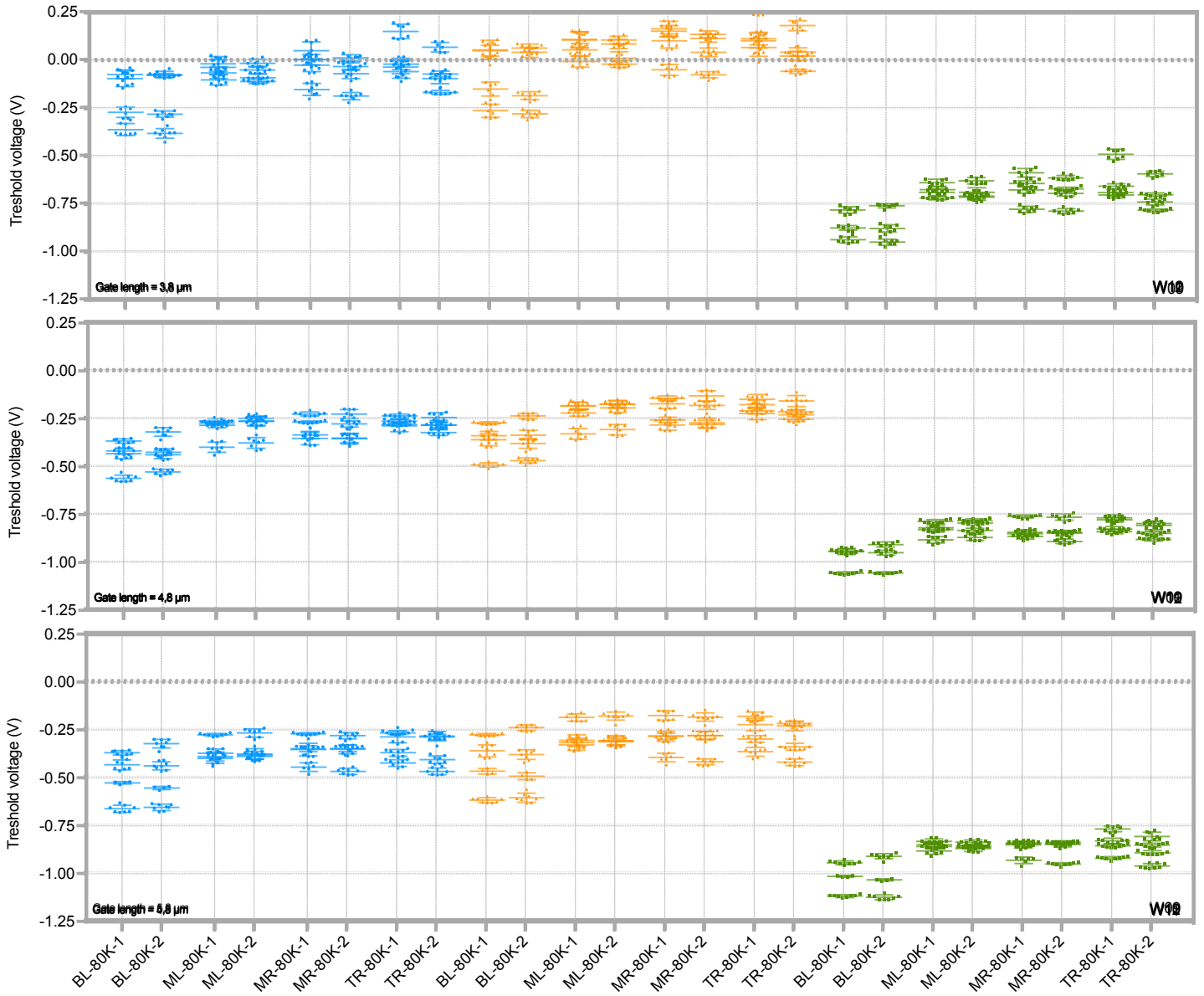
- gate sweep
  - V_{DS} = -[0.5, 3, 5] V
  - V_G = -5 V to 2 V (sweep)
  - V_{drift} = -3 V
  - V_C = 15 V
  - V_{CG} = 5 V



- clear sweep
  - V_{DS} = -5 V
  - V_G = -1.25 V
  - V_{drift} = -3 V
  - V_C = 0 V to 20 V (sweep)
  - V_{CG} = 5 V



Static measurements – all

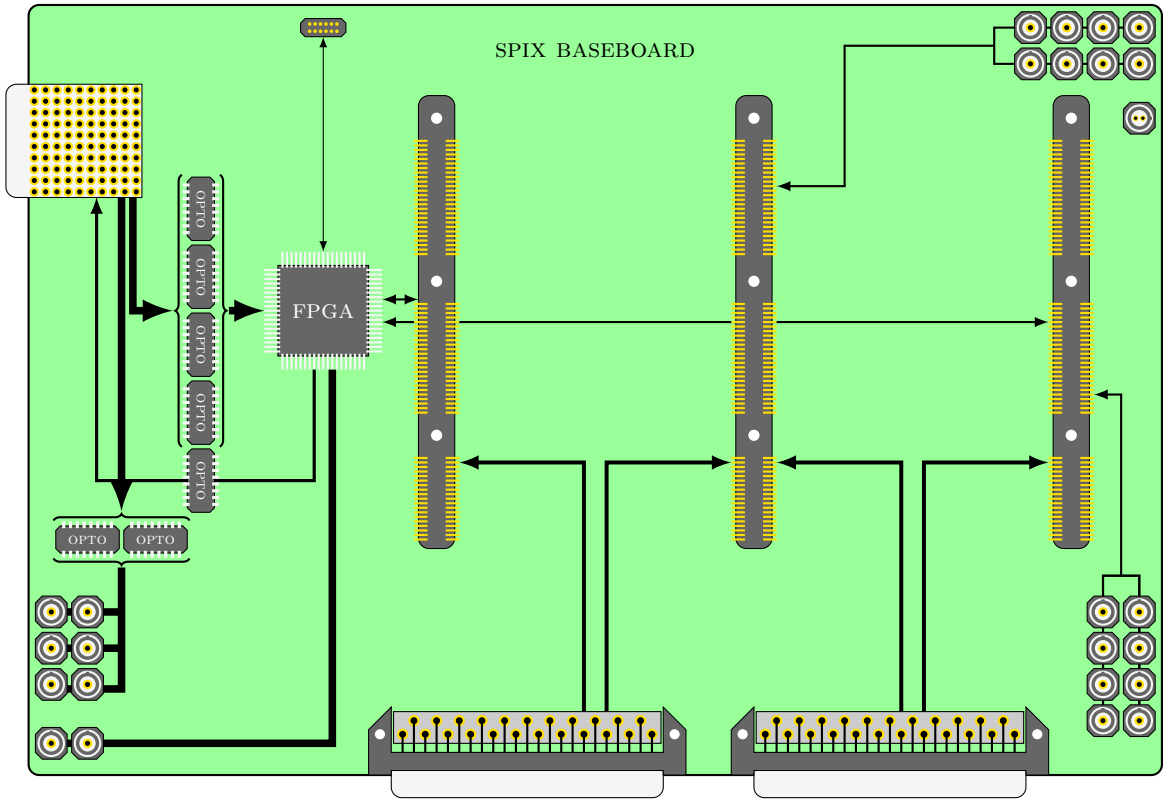


Single PIXel setup

operating principle

Design concept:

MODULARITY



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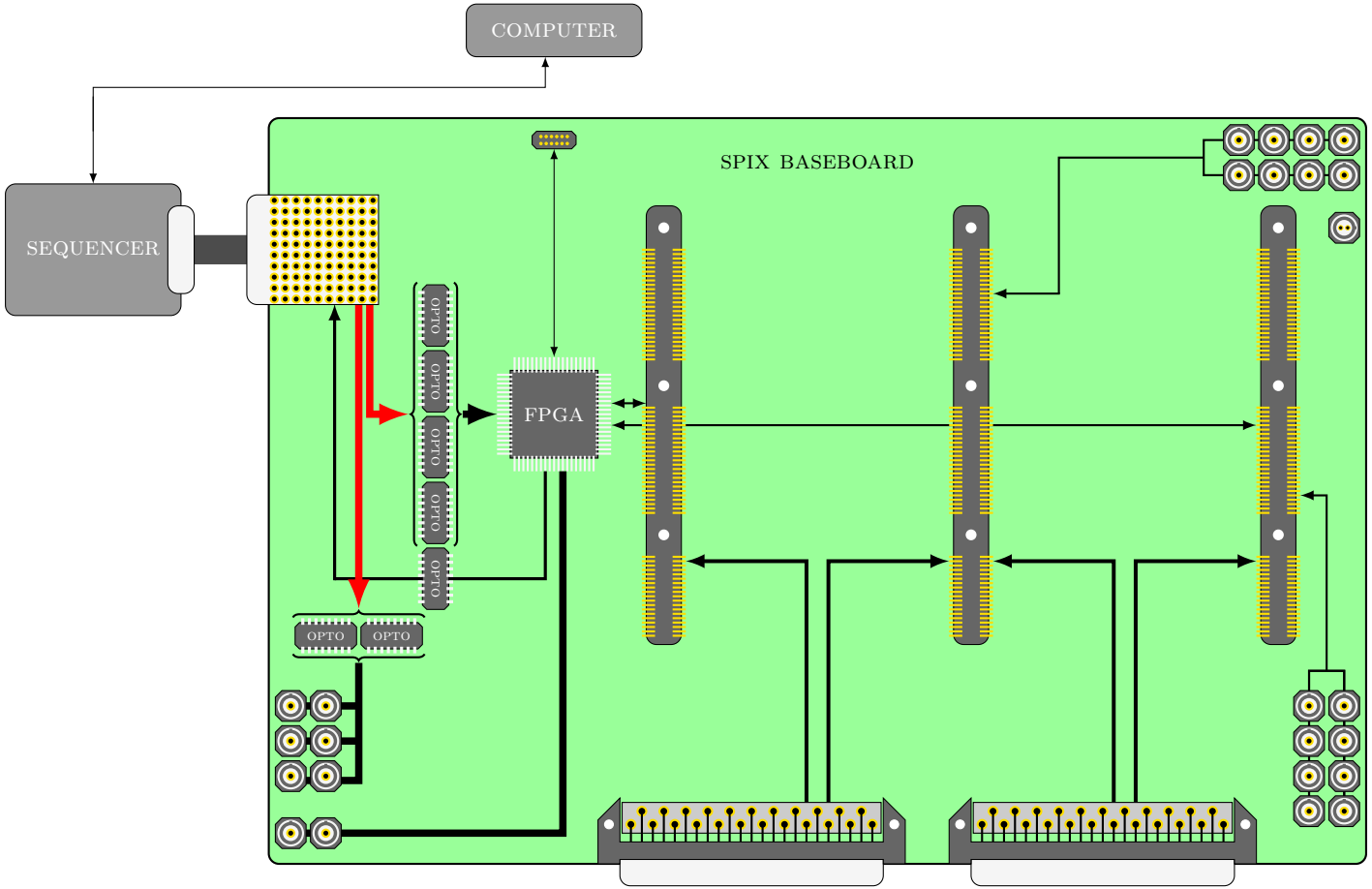

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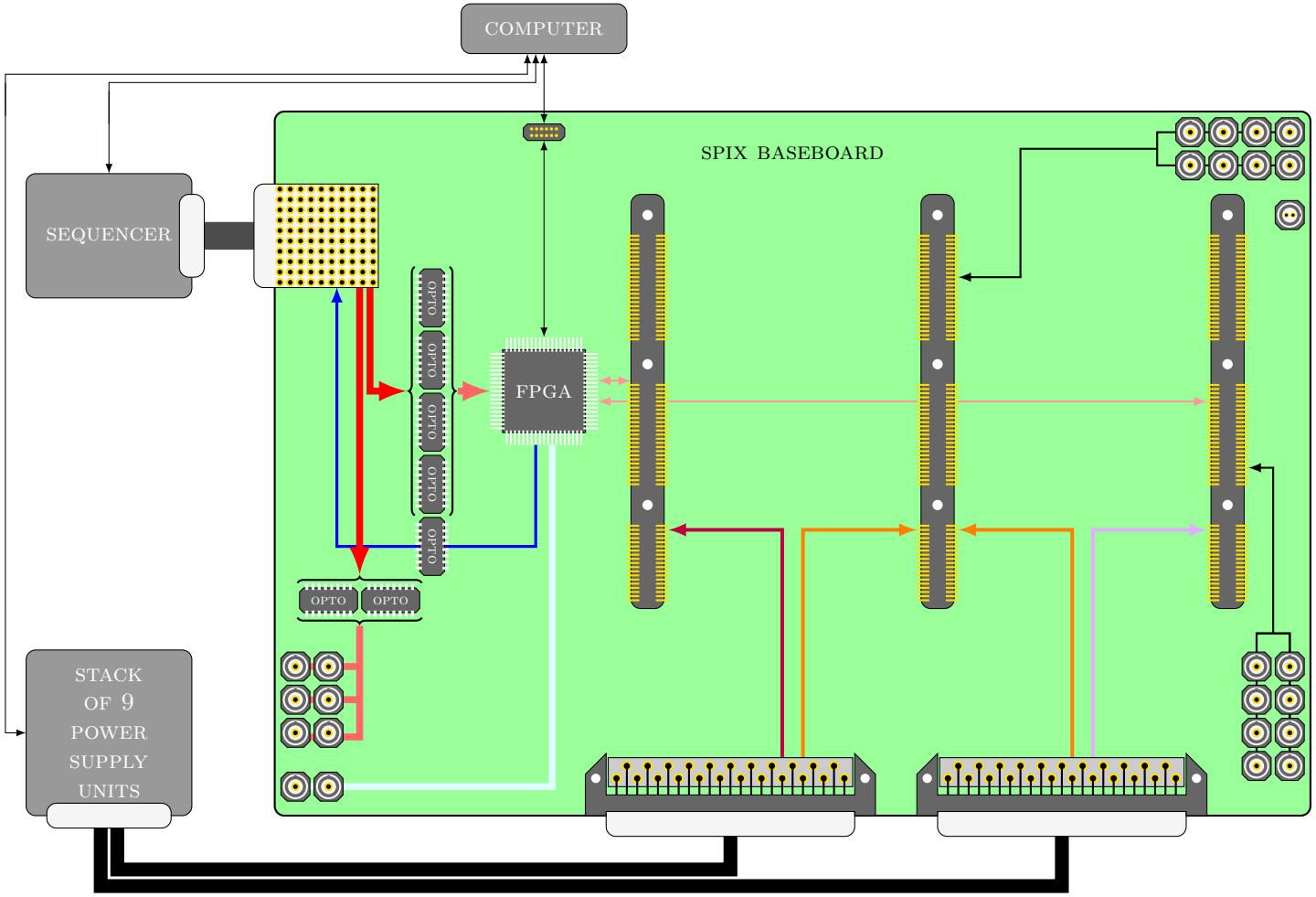

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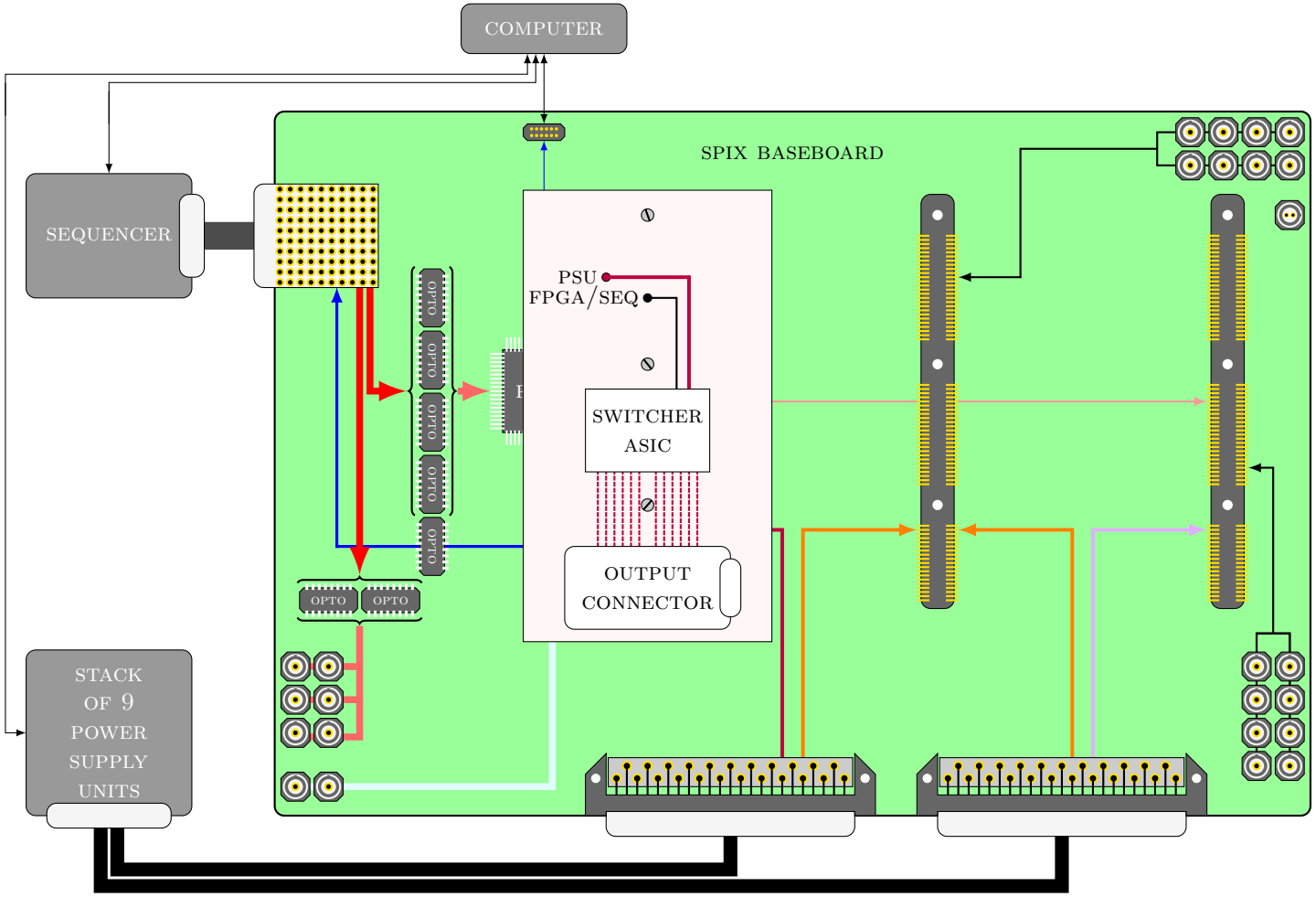

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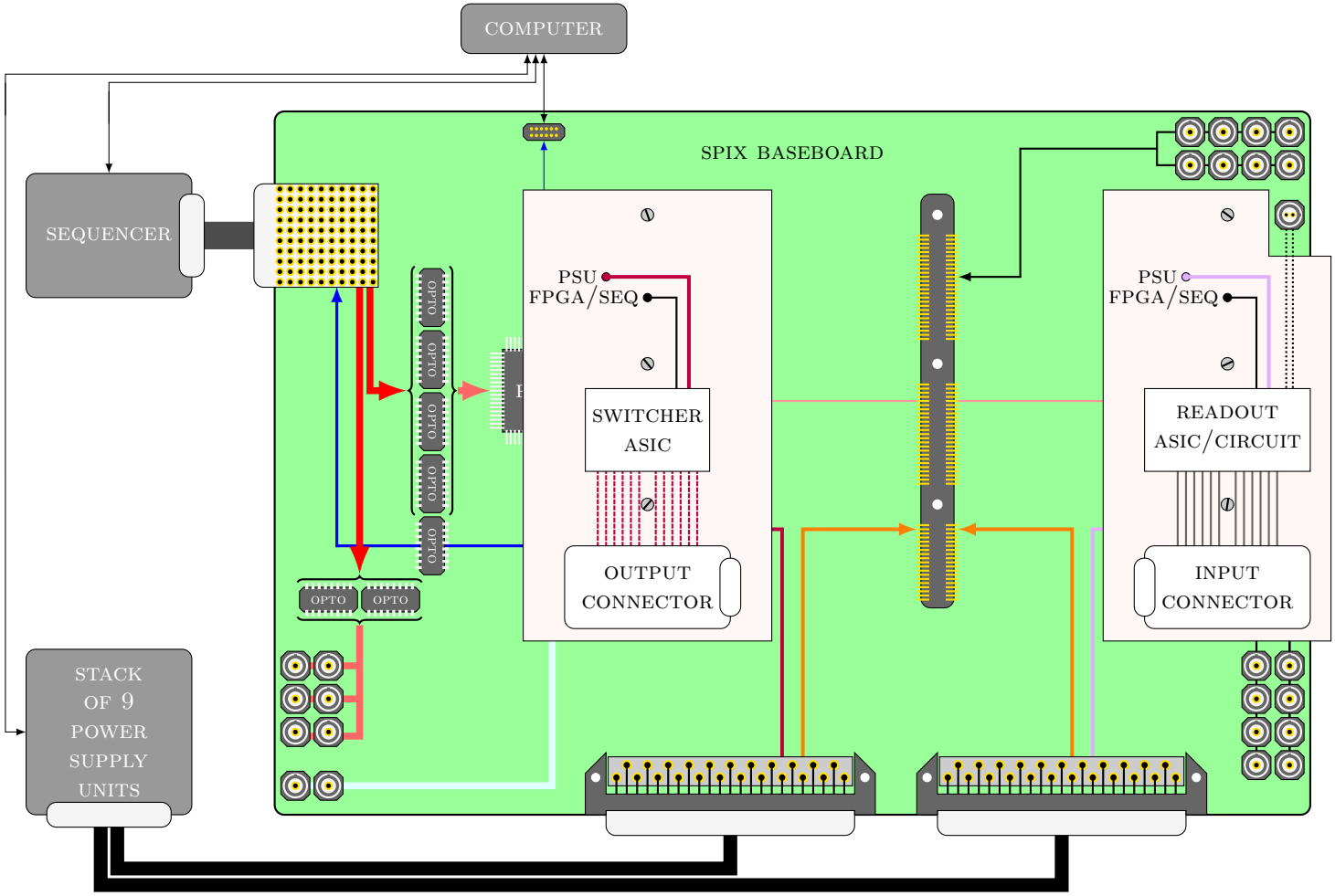

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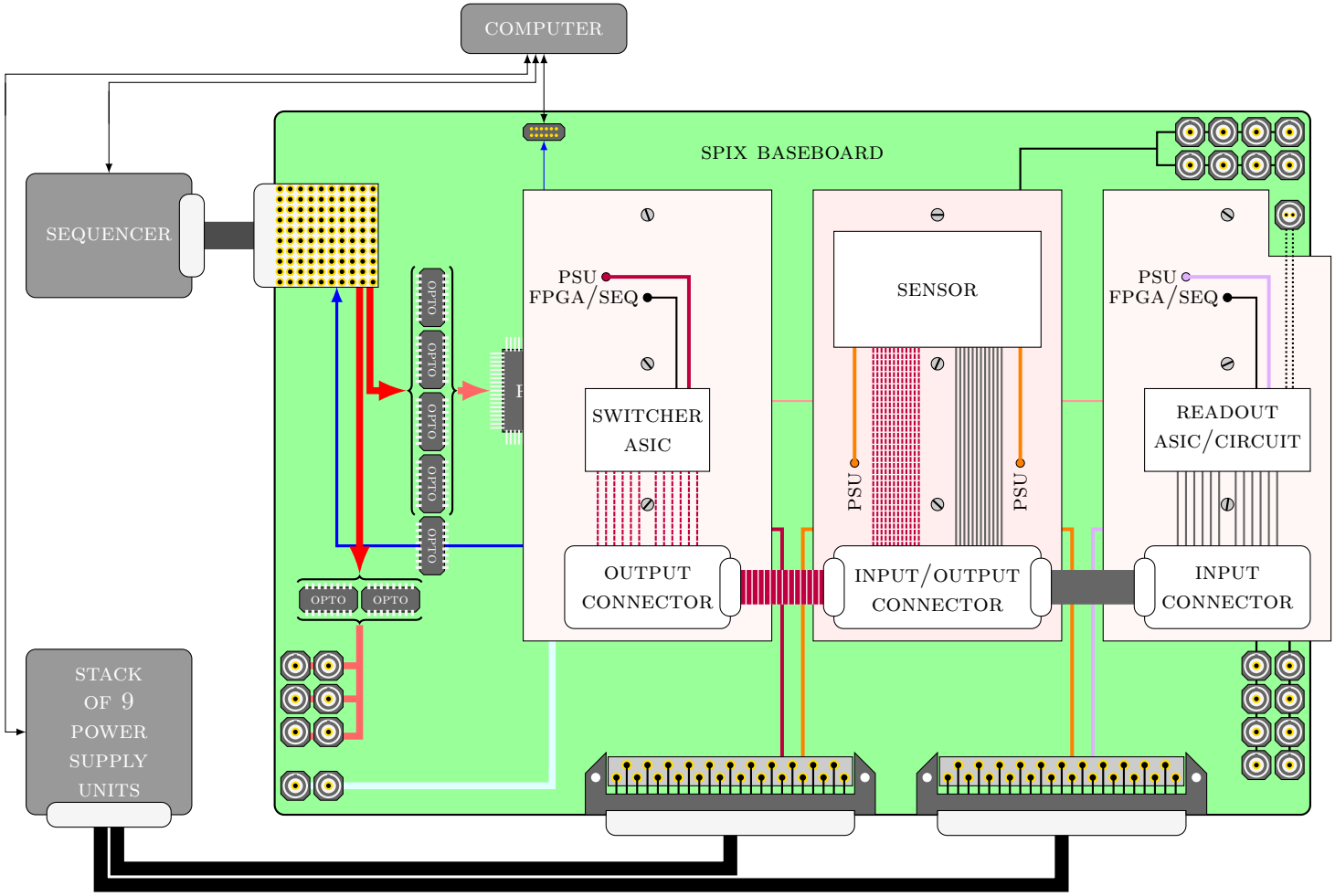

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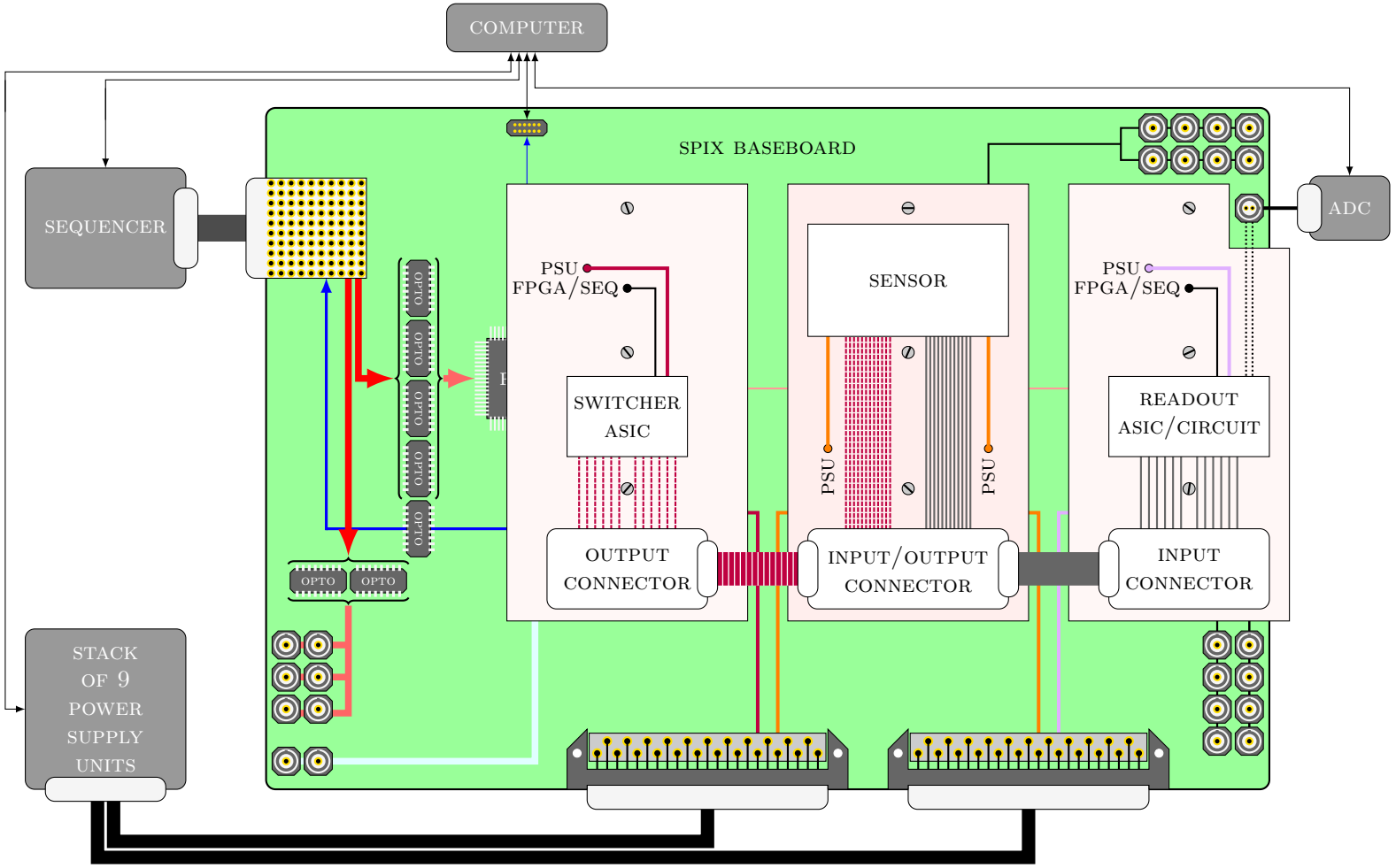

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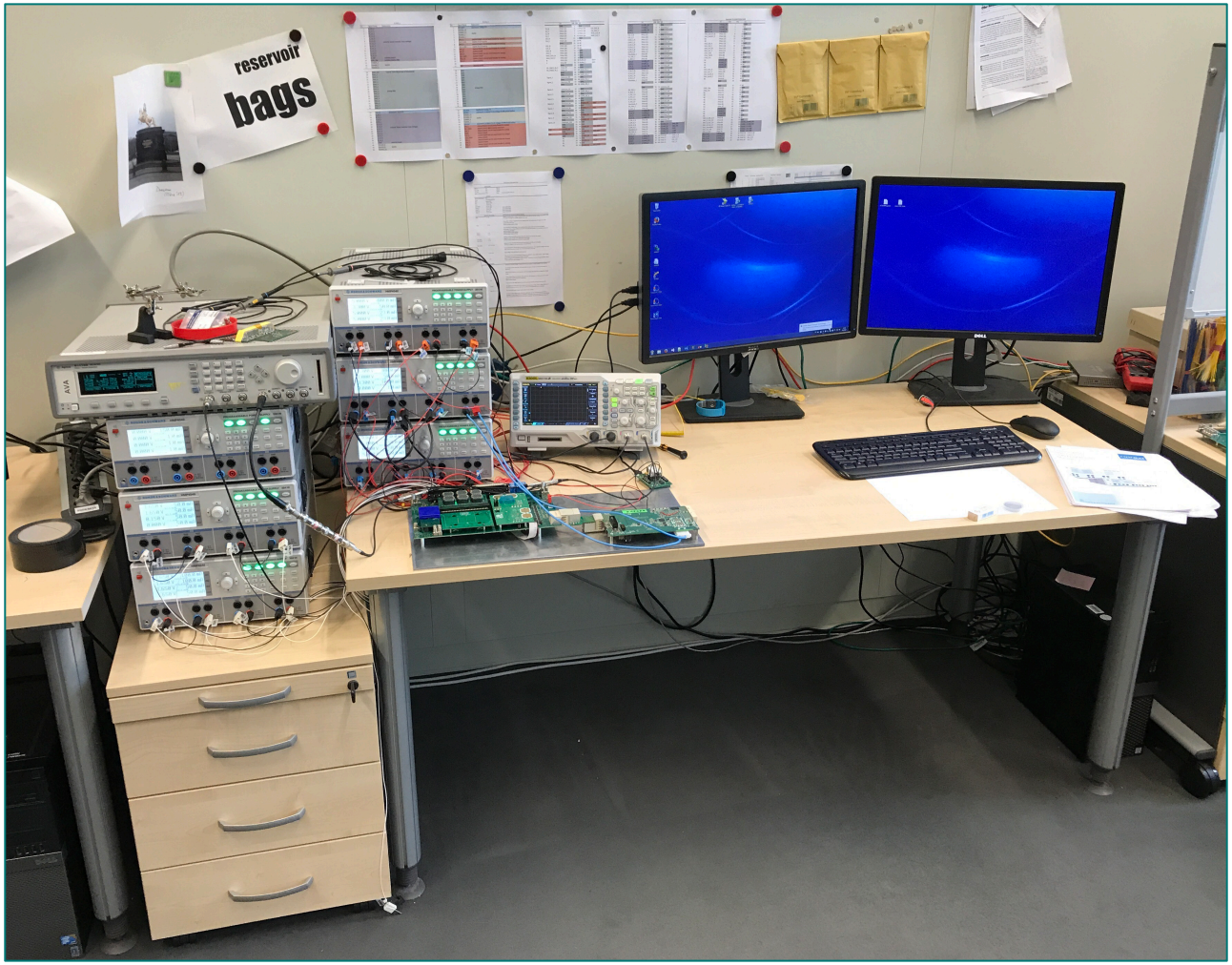
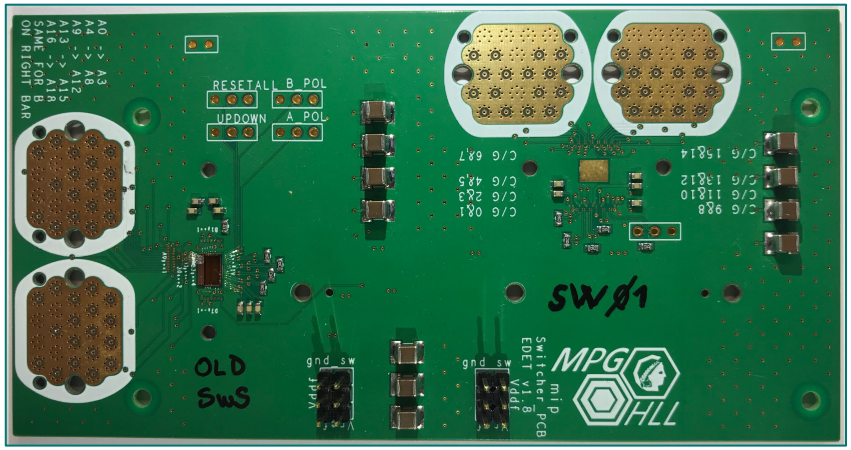


Single PIXel setup

EDET childboards - steering

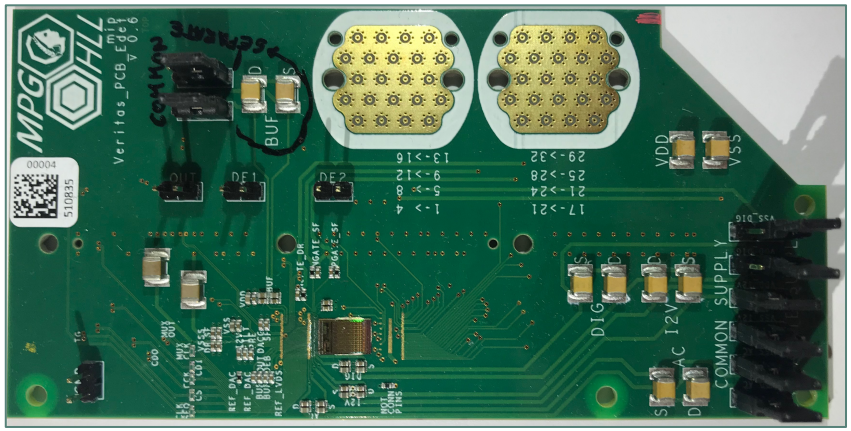
- SWITCHER BOARD
  - 18 channels with SWITCHERS
  - 15 channels with SWITCHERB
  - tested with SWITCHERS
    - from old and new production
  - plenty in stock
    - 3 with old production SWITCHERS
    - 1 with new production SWITCHERS
  - might be used for debugging of SWITCHERB for BELLEII (and EDET?)

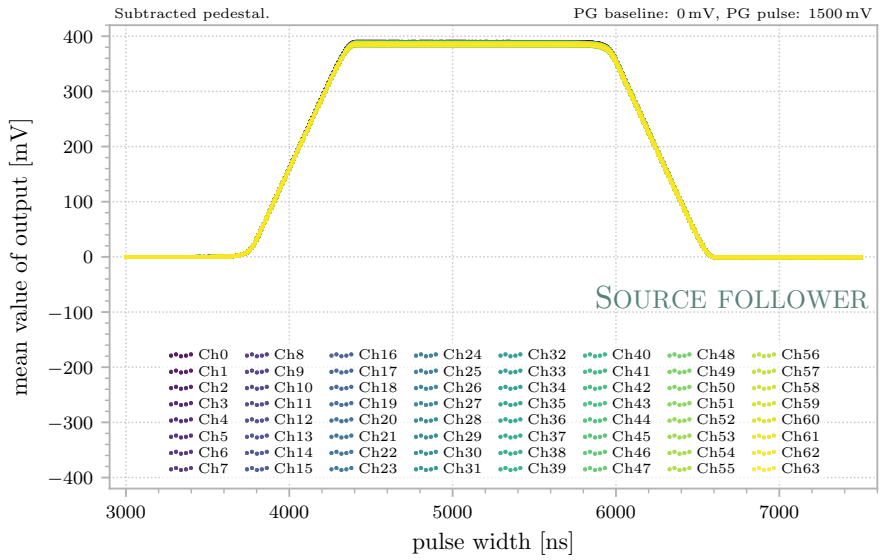


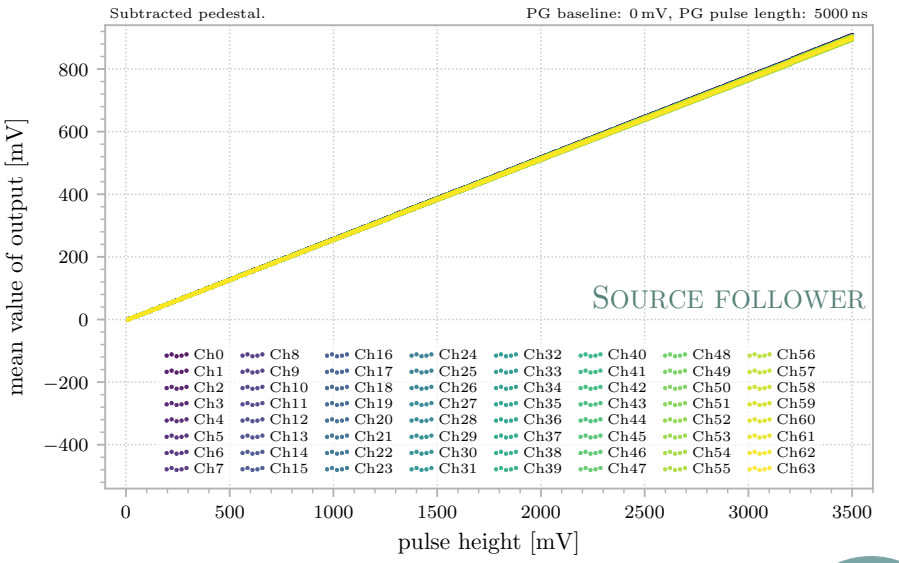
Single PIXel setup

EDET childboards - readout

- READOUT CHILDBOARD
  - uses VERITAS ASIC
    - source follower and drain readout modes



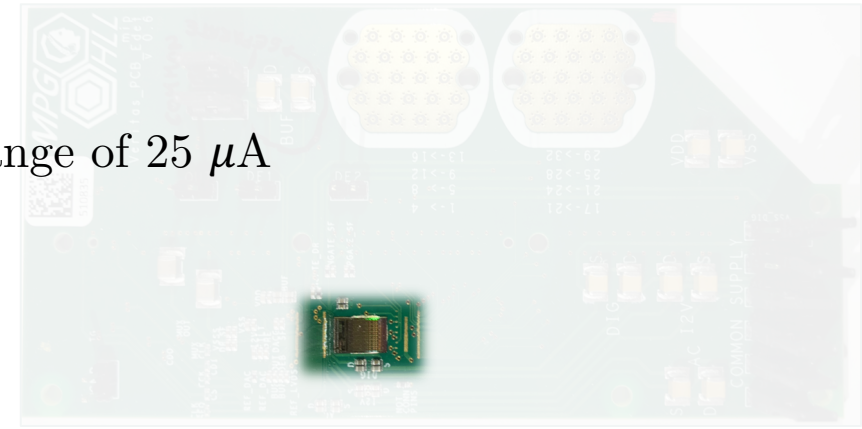


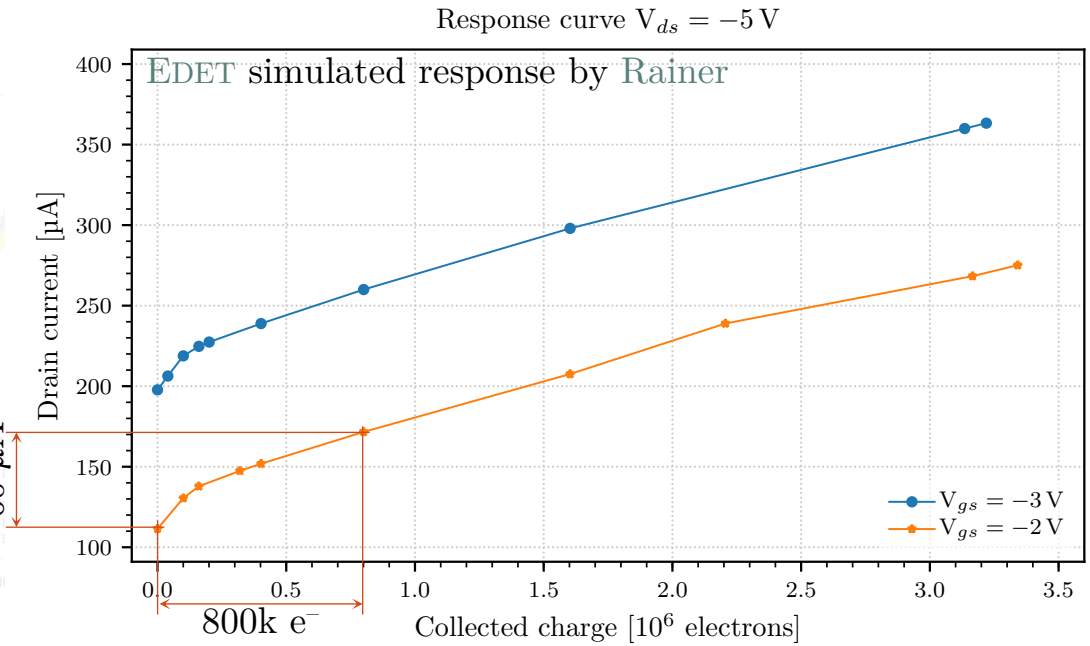


Single PIXel setup

EDET childboards - readout

- READOUT CHILDBOARD
  - uses VERITAS ASIC problem
    - input dynamic range of 25 μA
    - source follow
      readout modes

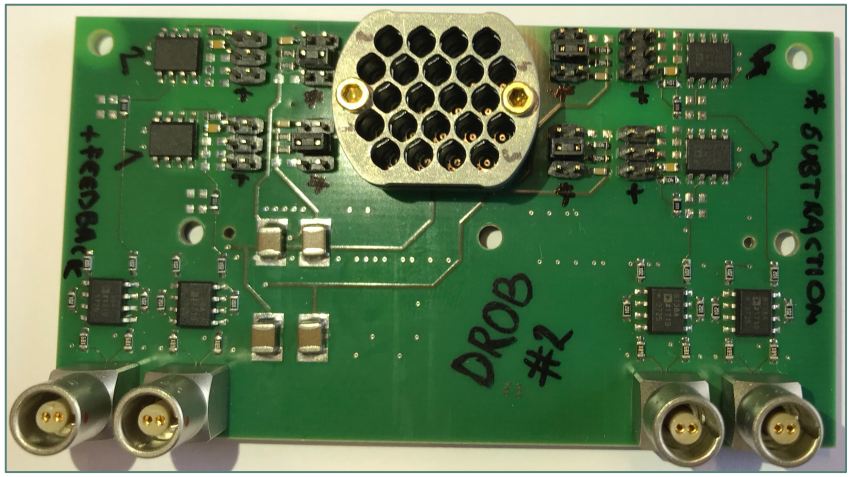


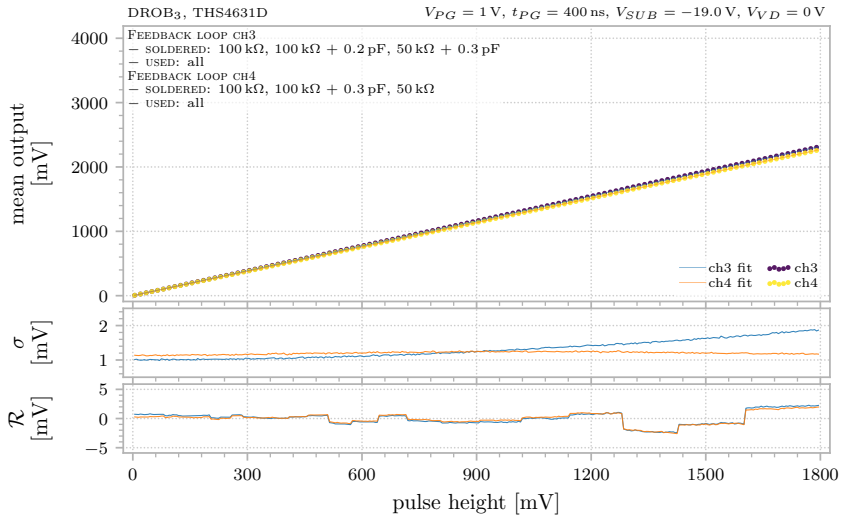


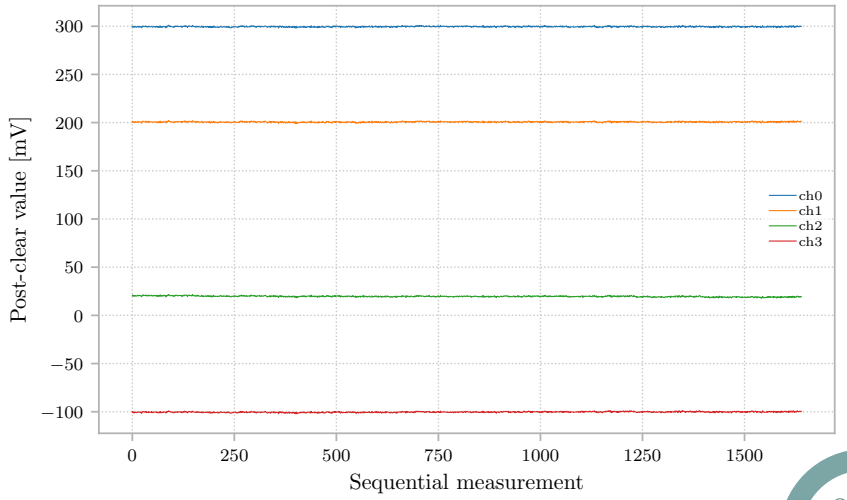
Single PIXel setup

EDET childboards - readout

- DRAIN READOUT BOARD
  - 4 discrete channels
  - changeable gain settings
    - tested with PG between 60 μA and 240 μA
  - changeable 1st and 2nd stage OPAMPs
  - highly susceptible to parasitic capacitances







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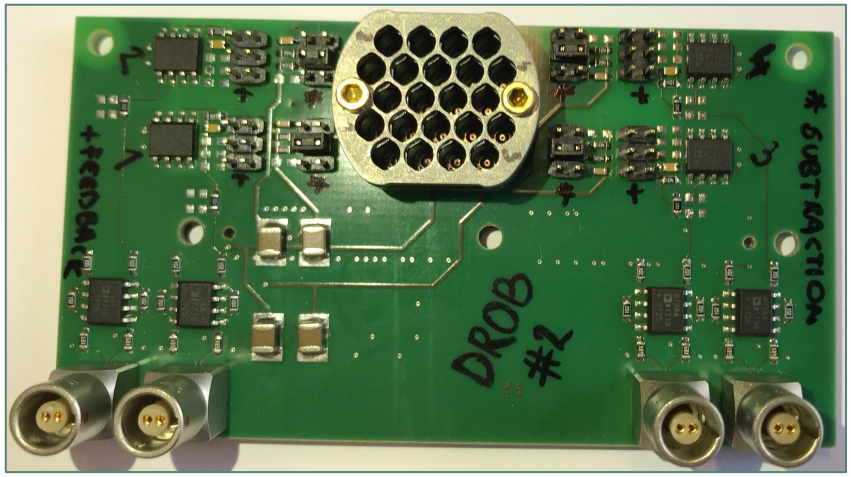
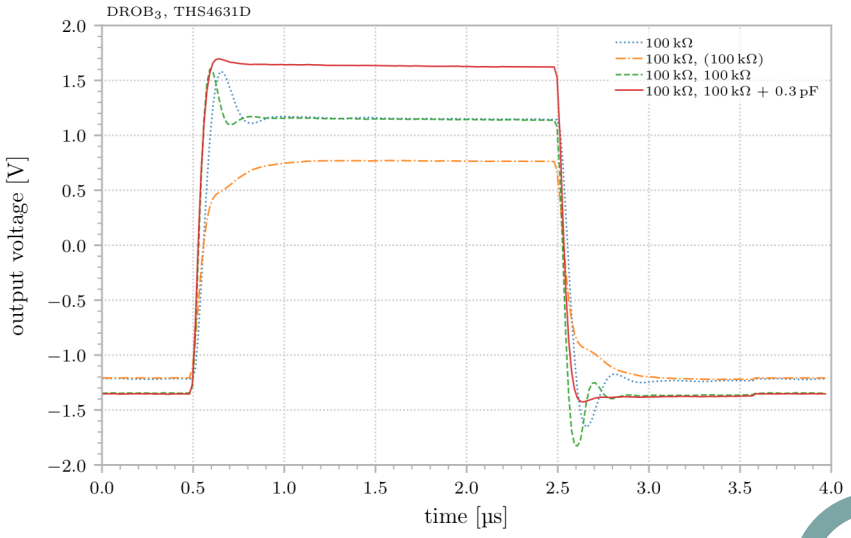
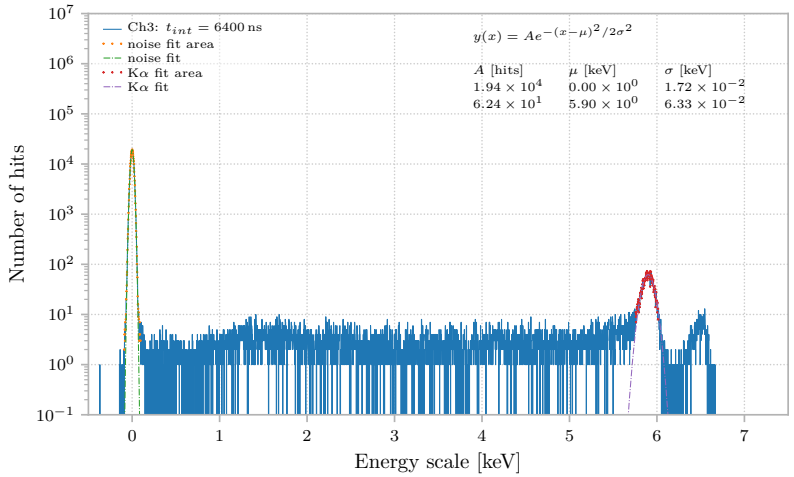




Preliminary results

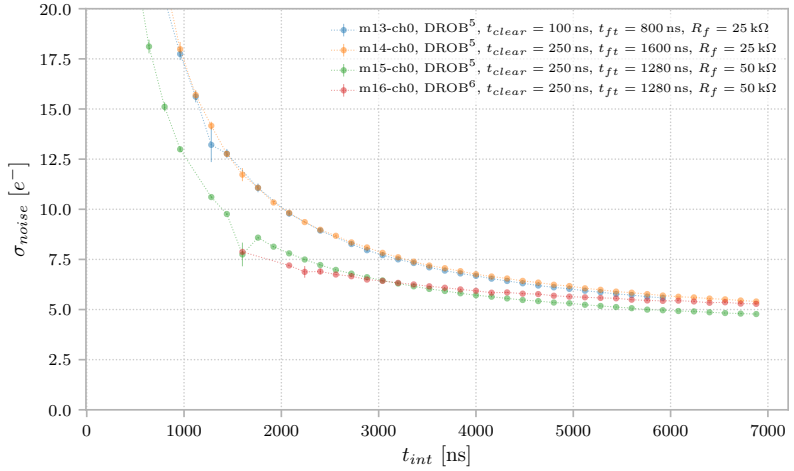
on non-depleted thick spix EDET structures

^{55}Fe spectrum



Drain	0.0 V		W12–BL–80k1
Source	5.0 V	d:	450 µm
Clear ON	23.0 V	Px:	24
Clear OFF	8.0 V	Ch:	3
Clear Gate	6.5 V	W:	5.8 µm
Gate OFF	15.0 V	L:	21.2 µm
Gate ON	2.1 V	φ:	3.6°
Drift	-5.0 V		

Noise vs. integration time



Not only electronic noise dominated:

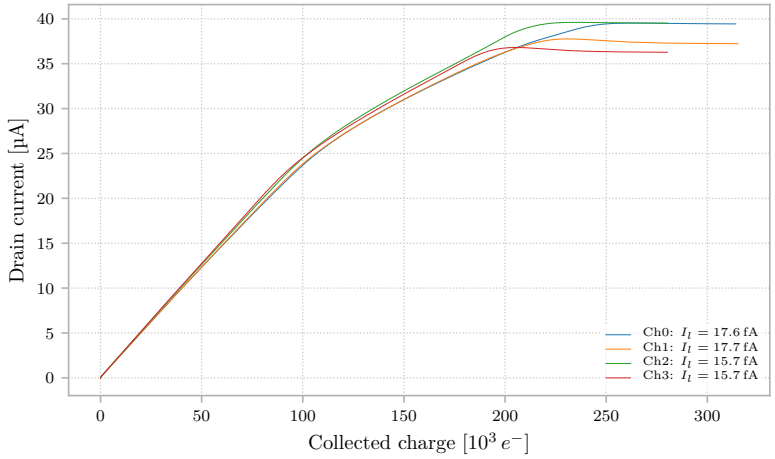
$$i \propto \frac{1}{\sqrt{R_{feedback}}}$$

Change of $R_{feedback}$ from 25 kΩ to 50 kΩ gives 12.5 % improvement in contrast to 29.2 %

Preliminary results

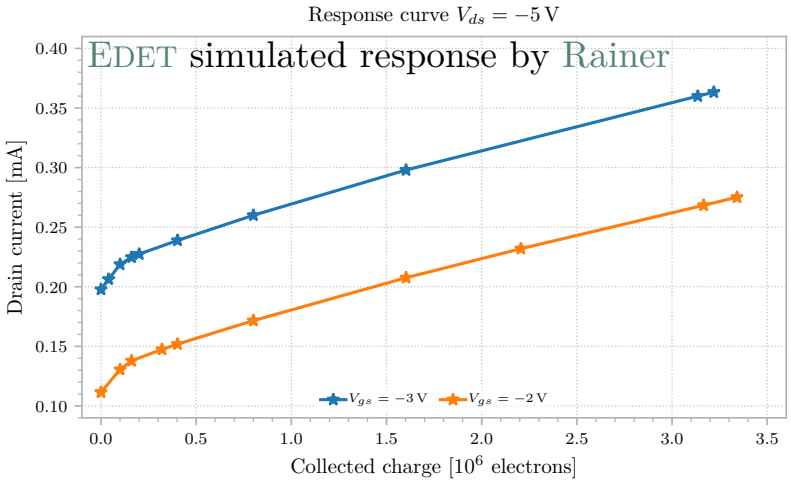
on non-depleted thick spix EDET structures

Measured Dynamic Range



Drain	0.0 V		W12–BL–80k1	
Source	5.0 V	d:	450 µm	450 µm
Clear ON	23.0 V	Px:	17 & 18	19 & 20
Clear OFF	8.0 V	Ch:	0 & 1	2 & 3
Clear Gate	6.5 V	W:	5.8 µm	5.8 µm
Gate OFF	15.0 V	L:	21.2 µm	21.2 µm
Gate ON	2.1 V	φ:	3.6°	7.2°
Drift	-5.0 V			

Simulated dynamic range



Since leakage current is linear in time it is perfect, albeit slow, mechanism to use for investigation of dynamic range.

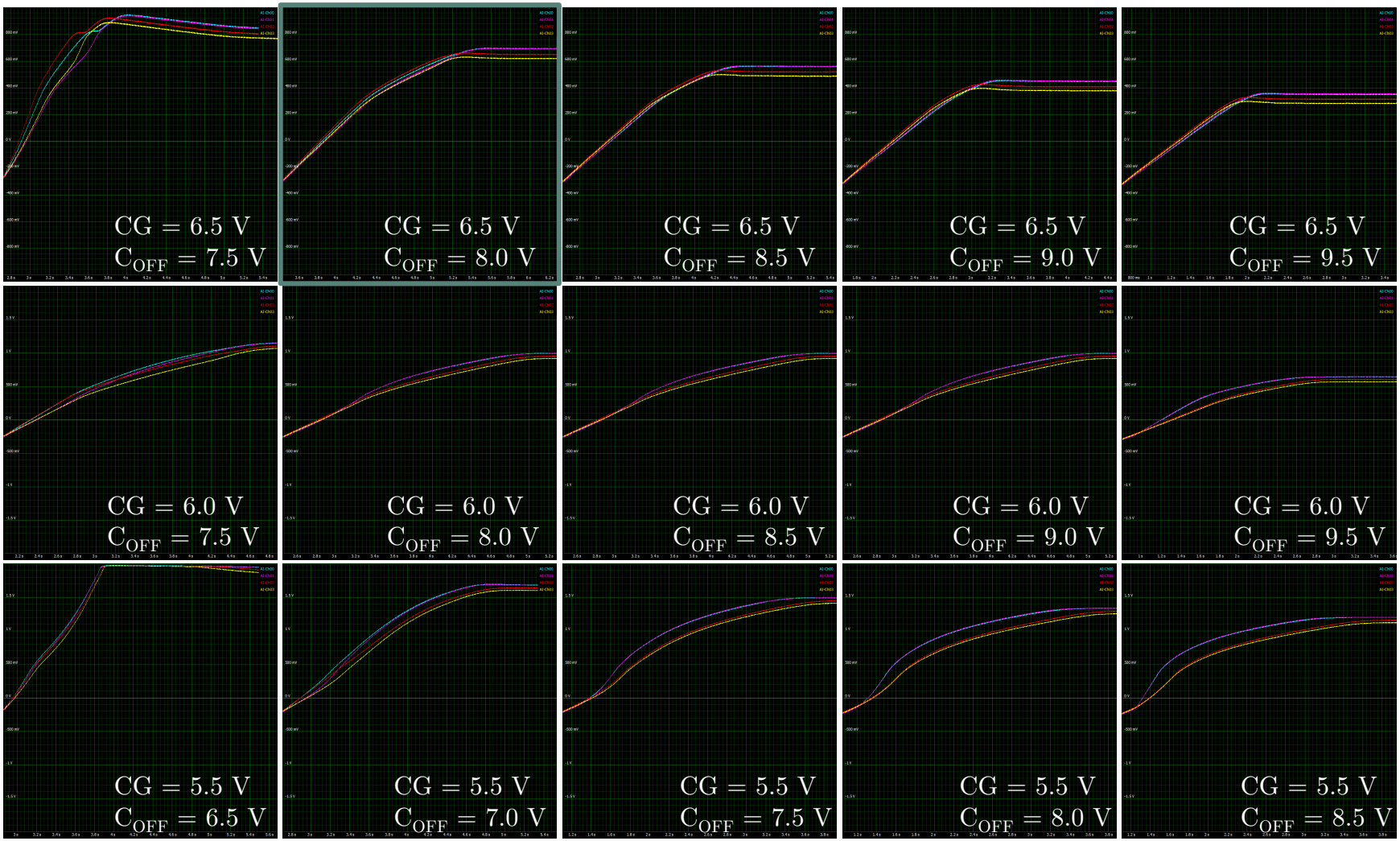
$t_{exp} \sim 3$ s

MISSING A FACTOR OF AT LEAST 5 IN CHARGE HANDLING CAPACITY.

REASONS?

Operating range

of non-depleted thick spix EDET structures



d	Px	Ch	W	L	φ
450 µm	17 & 18	0 & 1	5.8 µm	21.2 µm	3.6°
450 µm	19 & 20	2 & 3	5.8 µm	21.2 µm	7.2°

Operating range

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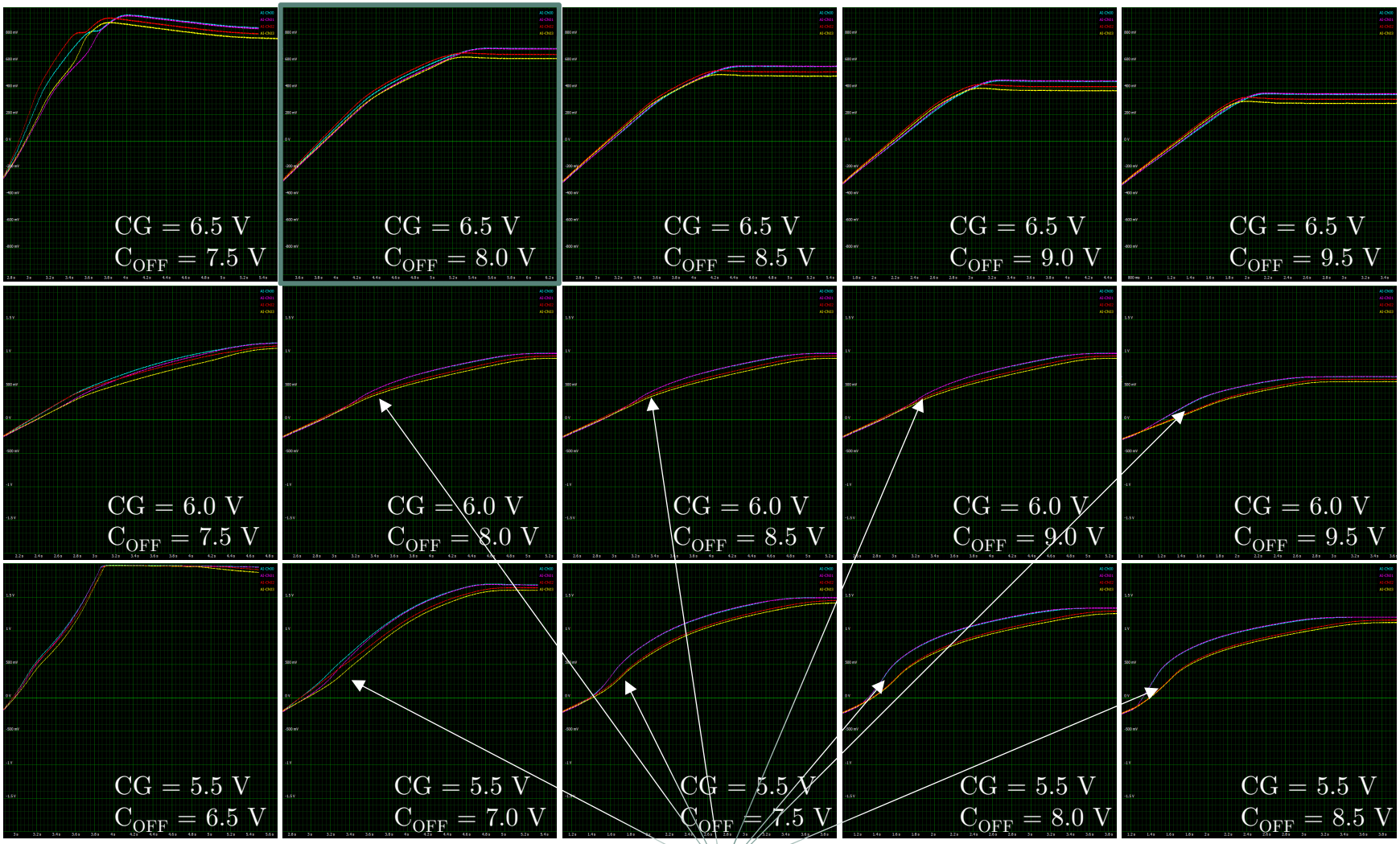
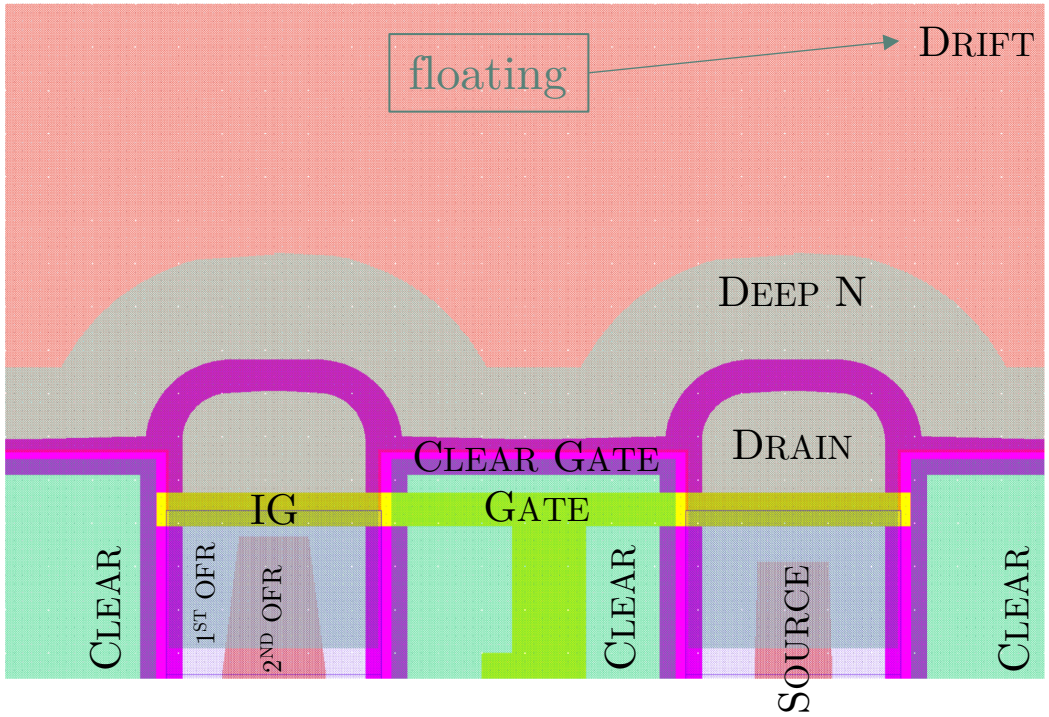


Increase of g_q?! → Potential pocket

Operating range - investigation

of non-depleted thick spix EDET structures

- no dependence of drain current on applied drift voltage
- missing contact between metal line and drift implantation
- potential pocket under drift
- only way for e^- generated under drift to arrive to IG is under clear



1 low clear voltage creates a barrier that e^- cannot overcome

2 high clear voltage puls the e^- into the clear

= small operation window in between

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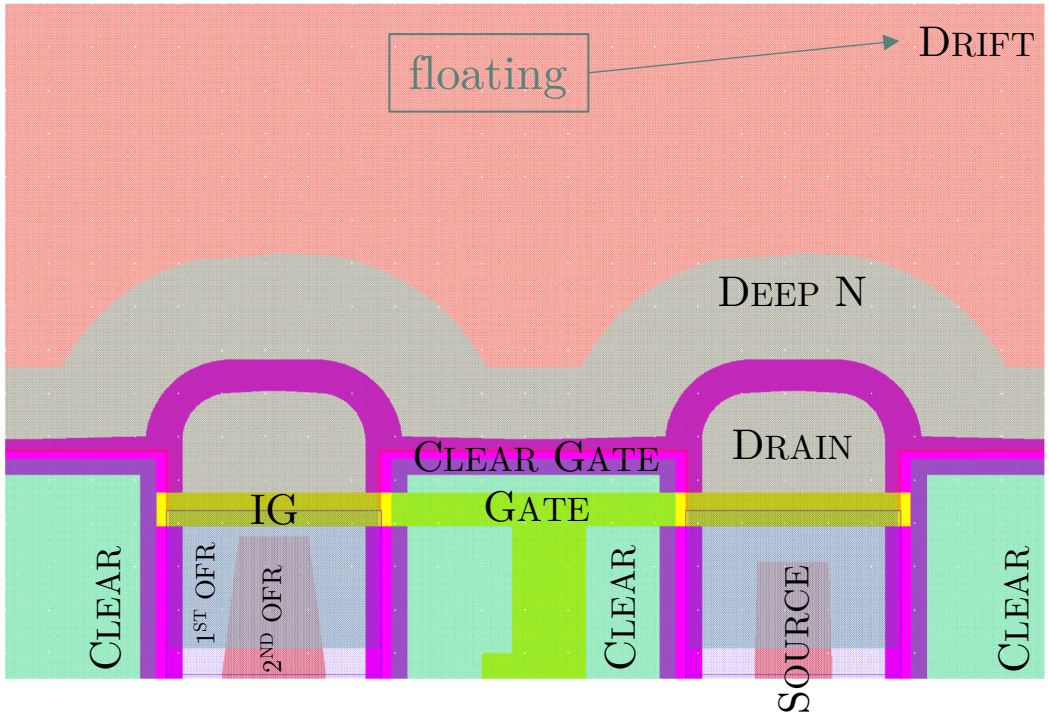

Possible solution: use of the thin structures with backside implantation, so that drift will be pulled by the backside voltage instead of clear gate

Summary & Future plans

- EDET SPIX structures work albeit the problems
- preliminary measurements of dynamic range match the "volume" of internal gate to the one of simulations.

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- repeat the measurements on small matrices
- find edges of operation parameters
- speed up the measurements by pulsed light source
- do the radiation hardness measurements
- simulate the design in Synopsys TCAD

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THANK YOU

BCK

Static measurements – analysis