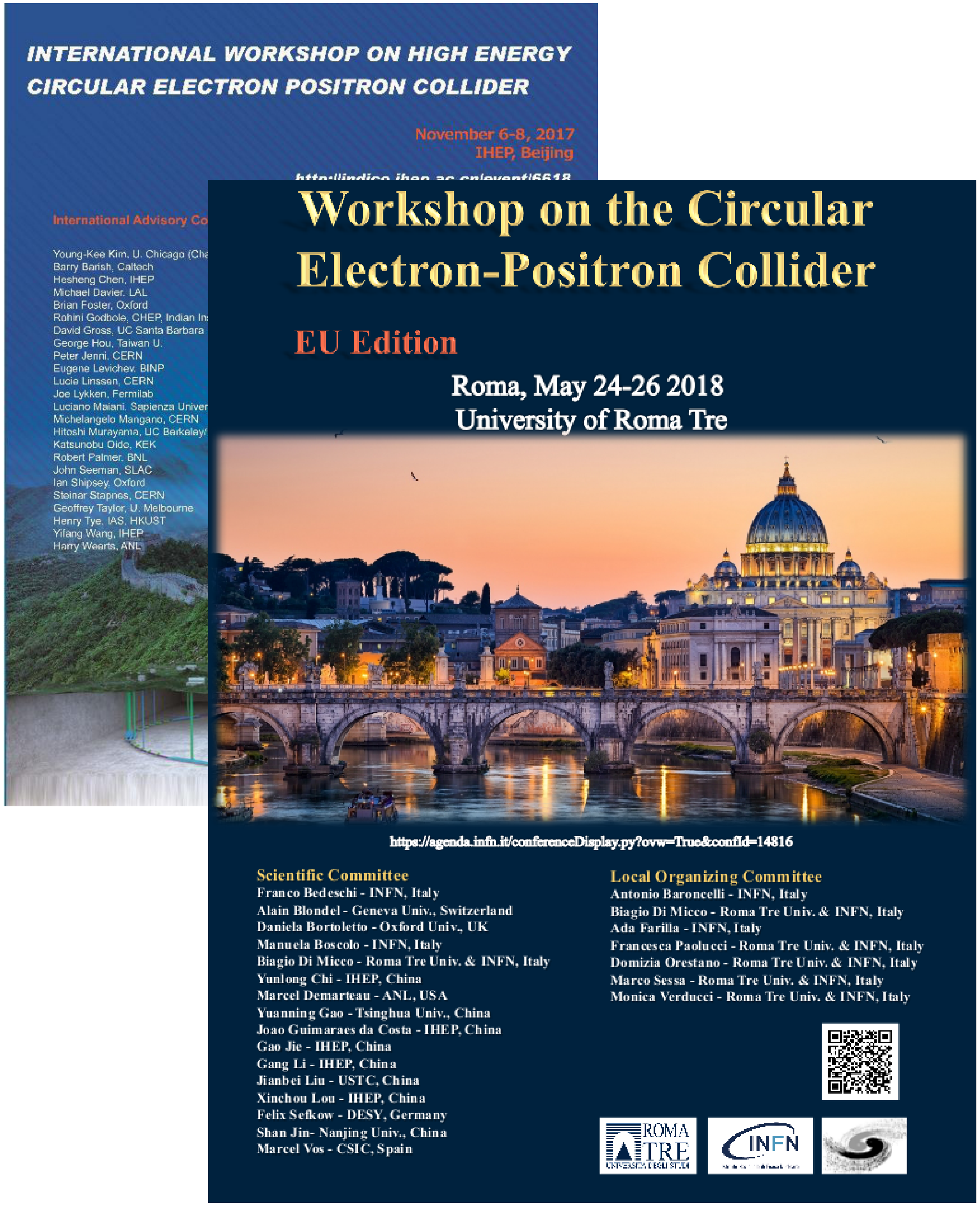
DEPFET for future e^+e^- colliders

Primarily ILC, with a brief status of CLIC, CEPC, FCCee...
Established technologies vs. promising R&D paths...

Marcel Vos IFIC (U. Valencia/CSIC), Spain

Marcel.Vos@ific.uv.es

Circular colliders



FCCee: CERN to host e^+e- collider in 100 km tunnel

CEPC: Chinese proposal for a large circular e^+e^- collider

Chinese project looking to internationalize → first European workshop in May

DEPFET is a good candidate for an FCCee or CEPC detector

CLIC status

CLIC staging

- start with “low” energy: 380 GeV

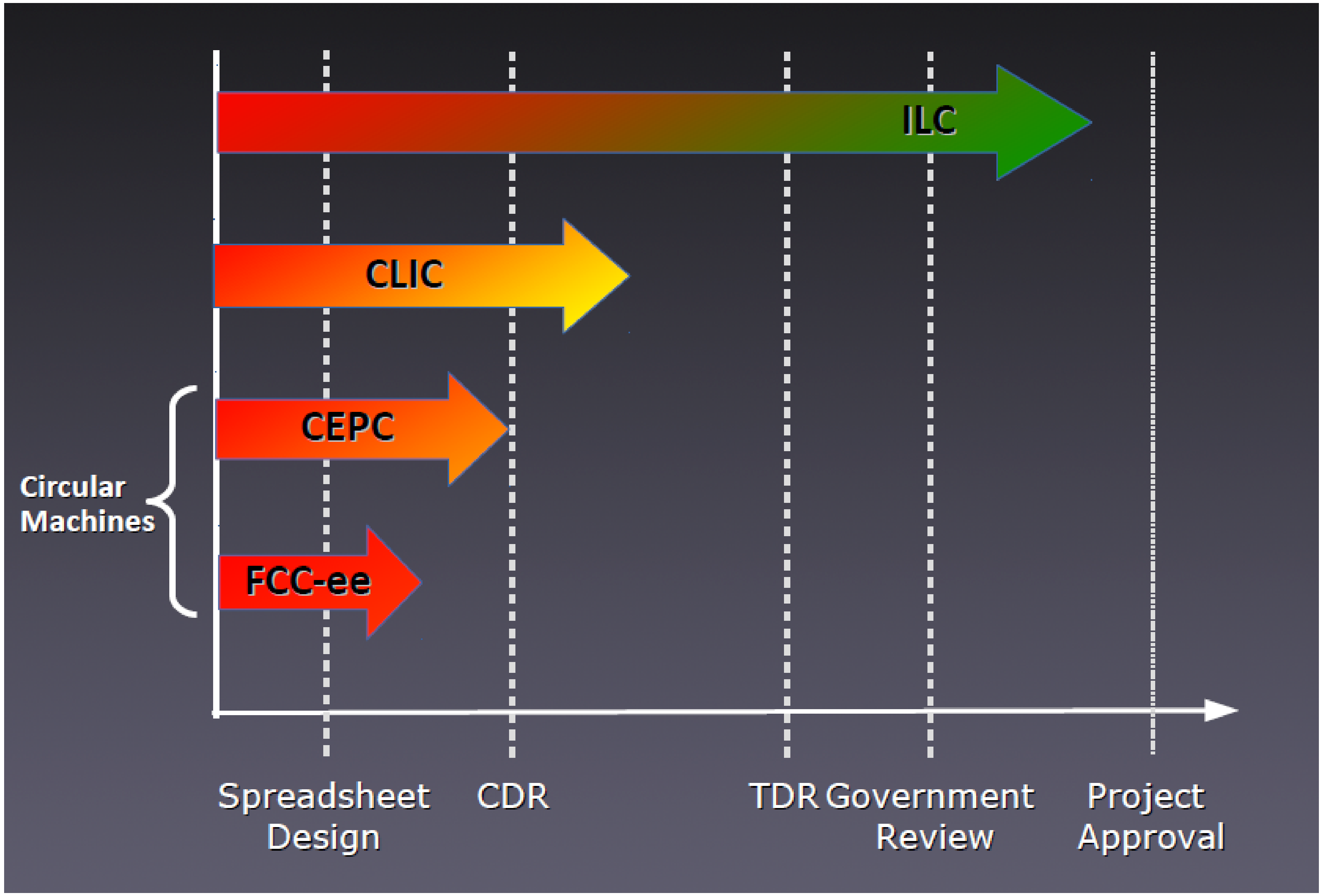
  precision Higgs and top physics in an “affordable” machine

- move to 1.5-3 TeV (as required by new physics reach)

Challenging combination of small beams (→ significant background) and short (0.5 ns) bunch spacing requires fast read-out (slim hybrid pixels, monolithic CMOS)

CERN-2016-004

Readiness



Marcel Stanitzki

European strategy update due in 2019/20

ILC TDR in 2013 → government decision before 2019

CLIC CDR in 2012 → CERN decision by 2020

FCCee/hh and CEPC CDR before 2019 (design, cost, time)

ILC staging

Staging: 250 GeV initial machine

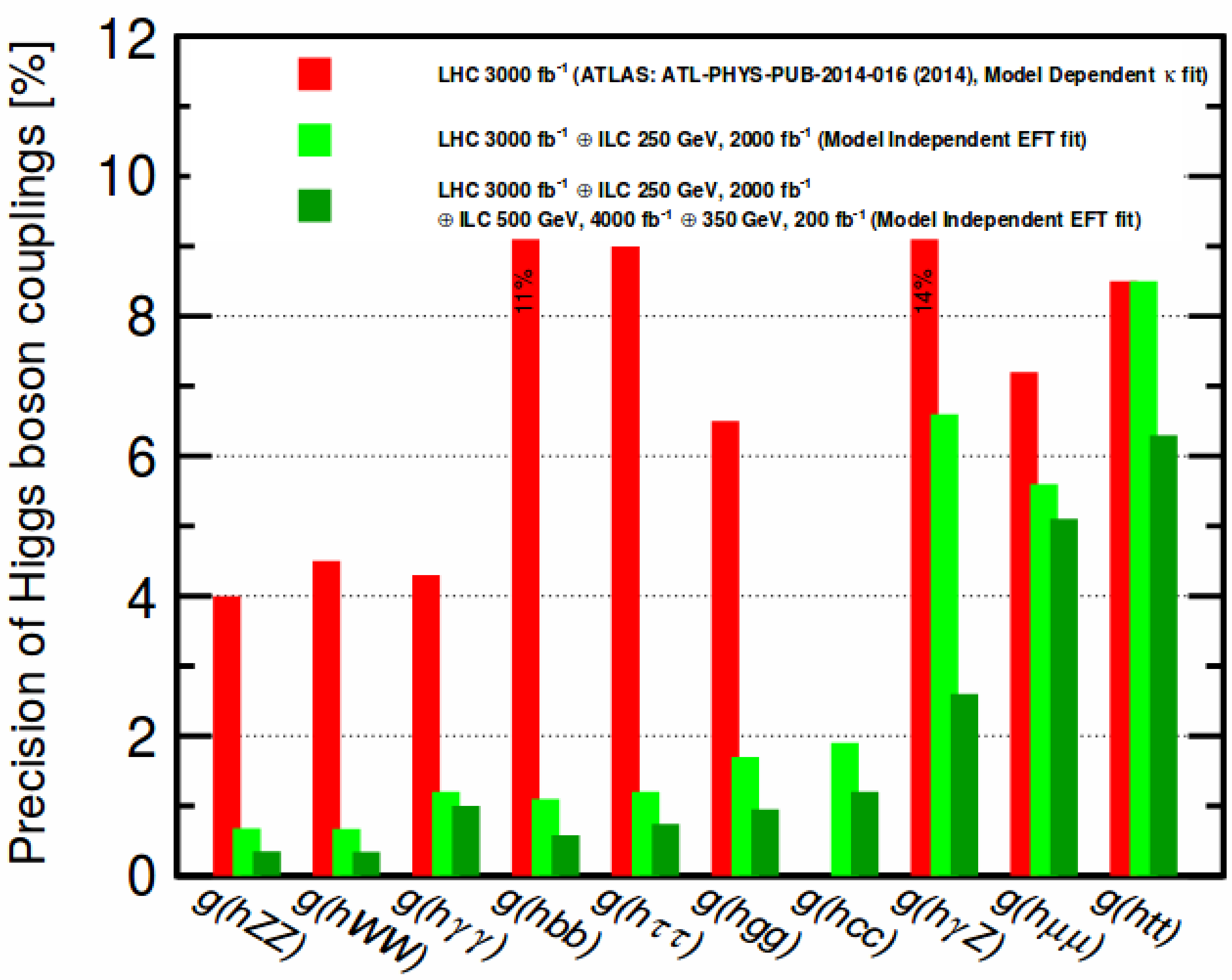
Physics case from LCC physics group: arXiv:1710.07621

Focused program to measure
Higgs couplings.

Good sensitivity to BSM effects
through the Higgs boson.

Less ambitious (no more top physics)

More overlap with circular machines



From “International Linear Collider” to “Japanese Higgs Factory”

ILC status

Proposal for 250 GeV ILC is in government review in Japan

Looking for international contributions
- high-level US-Japan meetings
- successful visits to Germany and France
- other European countries (ES, IT, UK) planned

Japanese decision is "an input to the European strategy update" (KEK management)

http://newsline.linearcollider.org/2018/02/01/successful-visit-to-europe-one-big-step-for-ilc-realisation/

ILC status

https://physicstoday.scitation.org/doi/10.1063/PT.3.3867

Momentum is growing to revive the International Linear Collider (ILC) as a contender for the next big particle-physics machine [...] thanks to a confluence of scientific, political, and financial developments.

Scientific: RF technology progress to achieve considerable cost saving
Focus on initial stage, Higgs factory at $\sqrt{s}$ = 250 GeV
Better view of the time line and scope of hadron colliders

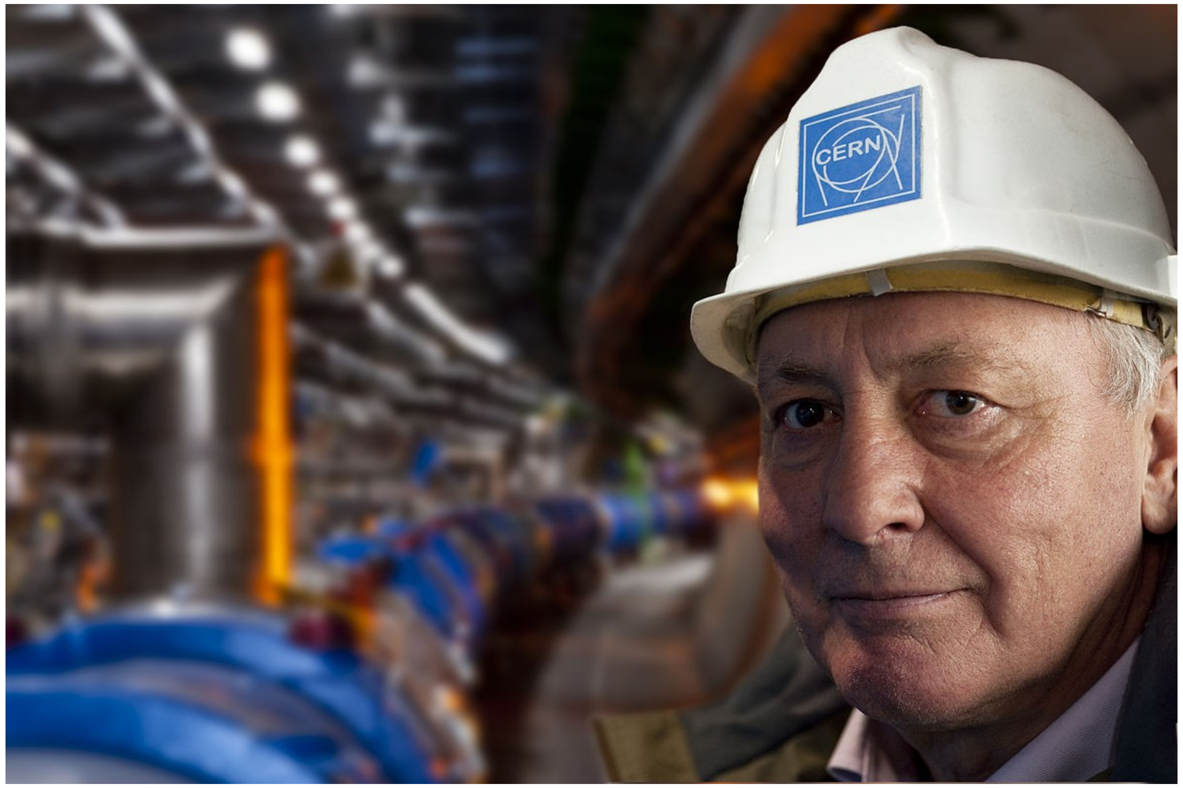
Financial: initial project cost reduced to 5 Billion (40% reduction wrt TDR)

Political: ILC is approved by Japan Association of High Energy Physicists (June 2017)
ILC is endorsed by Int'l Committee for Future Accelerators (ICFA, Nov. 2017)

Now, a clear signal from Japan that it wants to go ahead with the machine would put it back in the running. But that signal has to come this year, or European particle physicists will chart their future without the ILC.

ILC status

"What's needed is a move from neutrality," says CERN's Lyn Evans, director of the Linear Collider Collaboration, which coordinates global research on the ILC and CLIC. "Things are slow and opaque in Japan. It's a diode. We give information in, but get nothing out." The same thing happened with discussion of a contribution from Japan to the LHC, he recalls. "Suddenly, out of the blue, one came."



Decision?

Joint ILC/CLIC workshop at CERN February 2019

(decision between ILC and CLIC?)

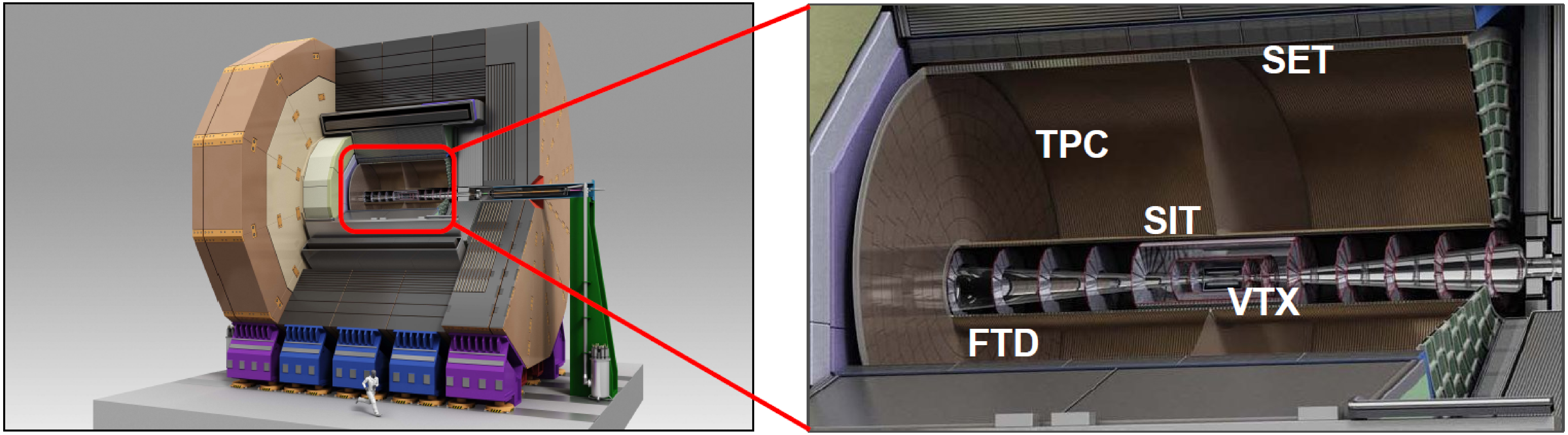
European Strategy update “open symposium”, May 2019

(Japanese position must be clear by this date)

European Strategy update “drafting session”, January 2020

(formulate conclusion)

Detector concepts



ILD → CMOS MAPS, DEPFET, FPCCD, SOIPIX

Adequate presence: VXD convener (M.V.) + Forward Tracker Disks (I. Vila)

SiD → single BX time stamping with 3D-integrated devices or Chronopixels

Precision vertexing

Mainstream R&D for silicon pixel detectors for HL-LHC is primarily about robustness:

- detect O(1000) tracks every 25 ns, survive a fluence of 10^{16} n/cm^2

The ILC* offers a motivation to build the next generation of precision devices:

- Inner radius: 30 mm → 15 mm
- Spatial resolution: 10 μm → 3-5 μm
- Material budget: 1% X_0 → 0.1% X_0
- Timing precision: 25 ns → 300 ns/1 μs/100 μs**

*CLIC is somewhere between the two extremes. It requires 10 ns time stamping to deal with backgrounds and relaxes some of the other specifications

**The timing requirement remains object of debate: SiD requires 300 ns (single BX), ILD envisages a combination of very precise, relatively slow layers mixed and fast, coarser-grained layers.

DEPFET candidacy

A paper that proves that DEPFET ladders with 20 x 20 mm² pixels and 100 ns frame rate can meet the ILC requirements

TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 6, NO. 1, SEPTEMBER 2010 1

DEPFET active pixel detectors for a future linear e^+e^- collider

The DEPFET collaboration
(www.depfet.org)
O. Alonso, R. Casanova, A. Dieguez
Universitat de Barcelona, Spain
J. Dingfelder, T. Hemperek, T. Kishishita, T. Kleinohl, M. Koch, H. Krüger, M. Lemarenko, F. Lütticke, C. Marinas, M. Schnell, N. Wermes
Bonn University, Germany
A. Campbell, T. Ferber, C. Kleinwort, C. Niebuhr, Y. Soloviev, M. Steder, R. Volkenborn, S. Yaschenko
Deutsches Elektronen-Synchrotron, Hamburg, Germany
P. Fischer, C. Kreidl, I. Peric, J. Knopf, M. Ritzert
Heidelberg University, Germany
E. Curras, A. Lopez-Virto, D. Moya, I. Vila
Instituto de Fisica de Cantabria (CSIC-UC), Santander, Spain
M. Boronat, D. Esperante, J. Fuster, I. Garcia Garcia, C. Lacasta, A. Oyanguren, P. Ruiz, G. Timon, M. Vos*
Instituto de Física Corpuscular (UVEG/CSIC), Valencia, Spain
T. Gessler, W. Kühn, S. Lange, D. Münchow, B. Spruck
Giessen University, Germany
A. Frey, C. Geisler, B. Schwenker, F. Wilk
Göttingen University, Germany
T. Barvich, M. Heck, S. Heindl, O. Lutz, Th. Müller, C. Pulvermacher, H.J. Simonis, T. Weiler
KIT Karlsruhe, Germany
T. Krausser, O. Lipsky, S. Rummel, J. Schieck, T. Schlüter
Ludwig-Maximilians-University, Munich, Germany
K. Ackermann, L. Andricek, V. Chekelian, V. Chobanova, J. Dalseno, C. Kiesling, C. Koffmane, L. Li Gioi, A. Moll, H. G. Moser, F. Müller, E. Nedelkovska, J. Ninkovic, S. Petrovics, K. Prothmann, R. Richter, A. Ritter, M. Ritter, F. Simon, P. Vanhoefer, A. Wassatsch
MPI Munich, Germany
Z. Dolezal, Z. Drasal, P. Kodys, P. Kvasnicka, J. Scheirich
Charles University, Prague, Czech Republic

***Abstract*—The DEPFET collaboration develops highly granular, ultra-transparent active pixel detectors for high-performance vertex reconstruction at future collider experiments. The characterization of detector prototypes has proven that the key principle, the integration of a first amplification stage in a detector-grade sensor material, can provide a comfortable signal to noise ratio of over 40 for a sensor thickness of 50-75 μm. ASICs have been designed and produced to operate a DEPFET pixel detector with the required read-out speed. A complete detector**

I. Introduction

Experiments at a future linear e^+e^- collider [1], [2] (LC) requires extremely precise reconstruction of the reaction products to perform precision physics programs to study the electroweak symmetry breaking mechanism and physics beyond the Standard Model. Key figures of merit for the detector performance, such as the jet energy resolution, momentum

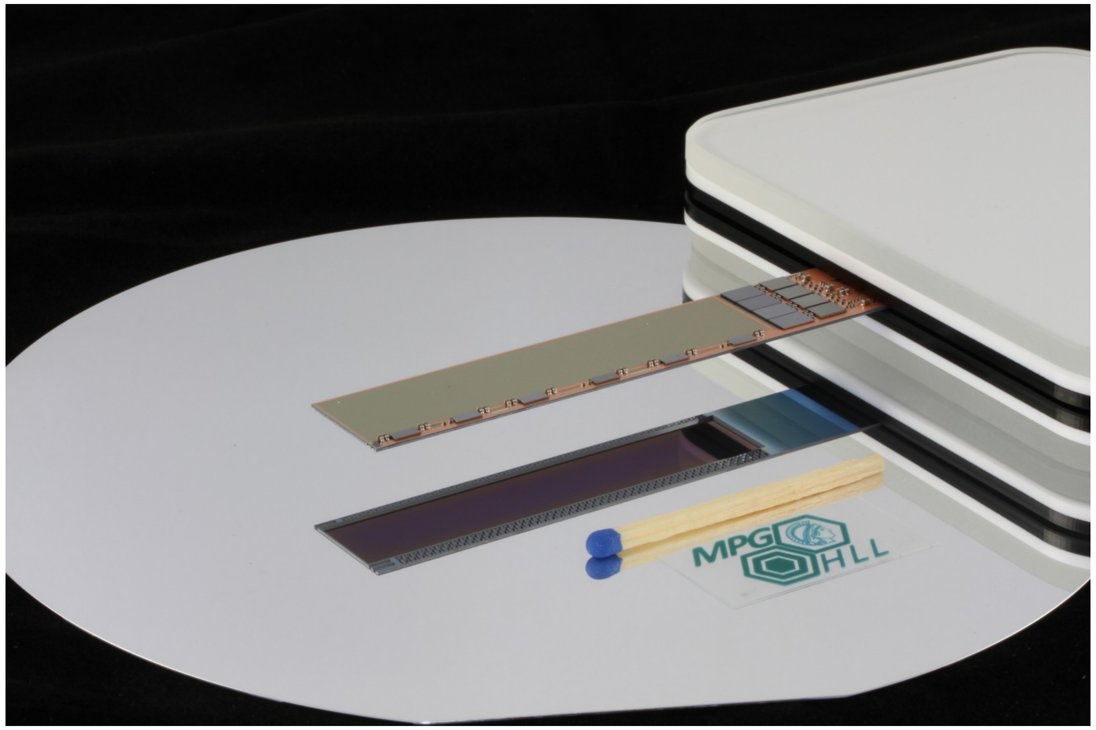
Note the date: 2010!!!

DEPFET

Successful completion of the Belle II PXD will be a major feat

The PXD ladder has many features (in-pixel amplification, electronics integrated on ladder, self-supporting ladder, material budget) I would not have believed 10 years ago

As our ECFA reviewer put it: “the most complex piece of silicon I’ve ever seen!”



The future of hybrid technology

High-density Interconnects:

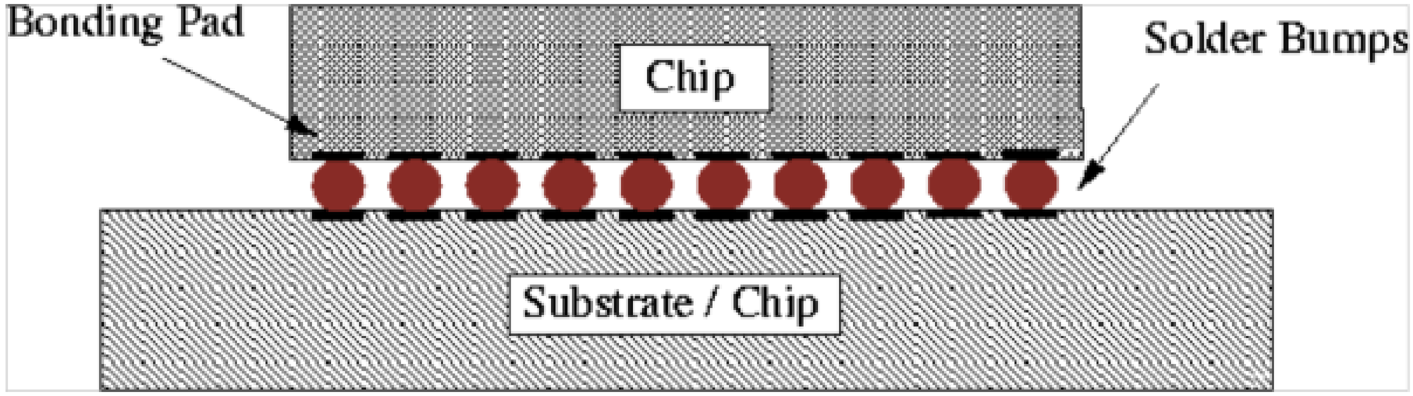
ATLAS, CMS: > 100 x 100 μm² pixels

TimePix, LHCb VELO upgrade: 55 x 55 μm² pixels

CLICpix2: 25 x 25 μm² pixels

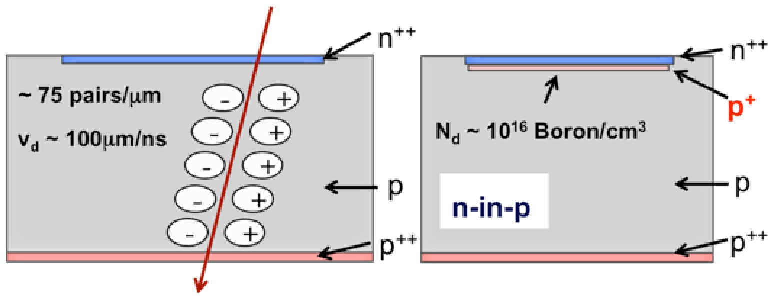
ASIC now part of the RD53 production

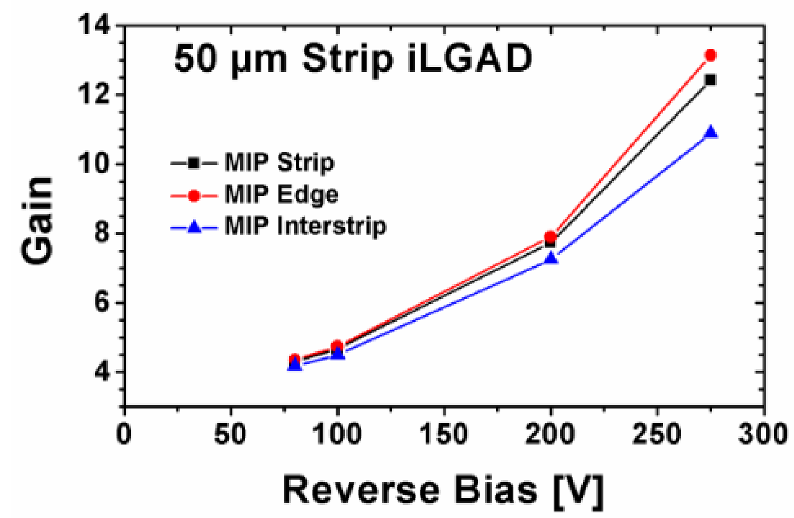
Bump-bonding at 25 μm pitch done by SLAC
CLICdp R&D project with IZM starting

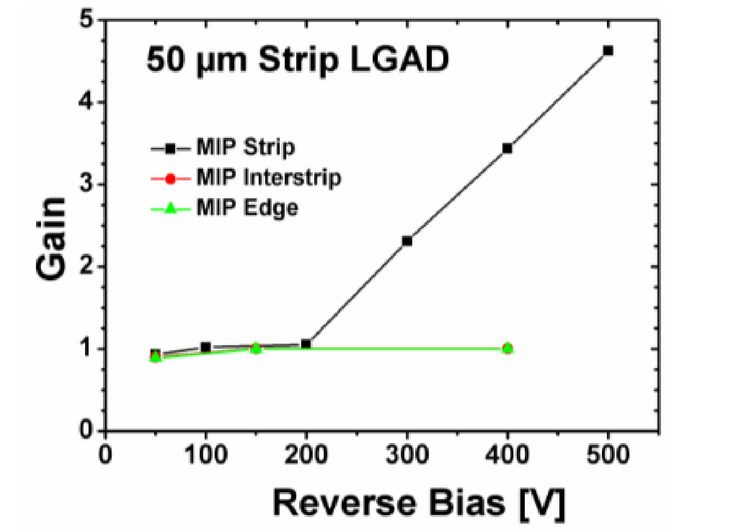


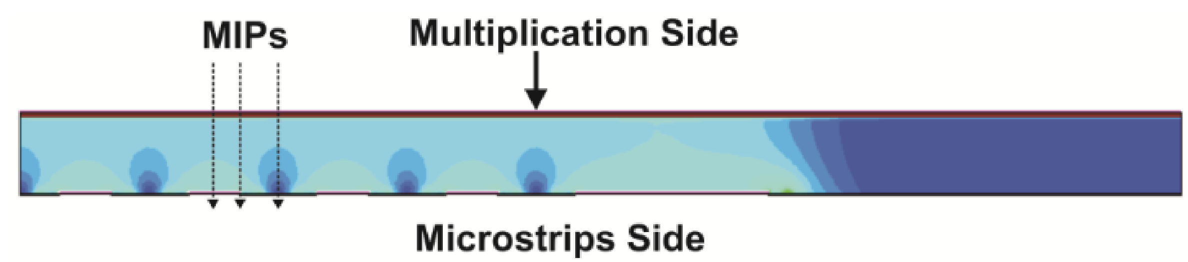
4D tracking?

The advent of ultra-fast position-sensitive silicon detectors…









LGAD =

Low-Gain Avalanche Detectors

iLGAD = inverted LGAD

(uniform gain, higher cost)

Technology development CNM Barcelona/RD50

P. Fernandez, et al, Simulation …, NIM A658 98-102 (2011).

G. Pellegrini et al., Technology …, 2013 Hiroshima Conference, NIMA 765 (2014)

Ultra-Fast Silicon Detectors, Santa Cruz, Florence 2012 (60-100 ps)

Characterization, Turin/CNM/UCSC, arXiv:1312.1080 (20 ps)

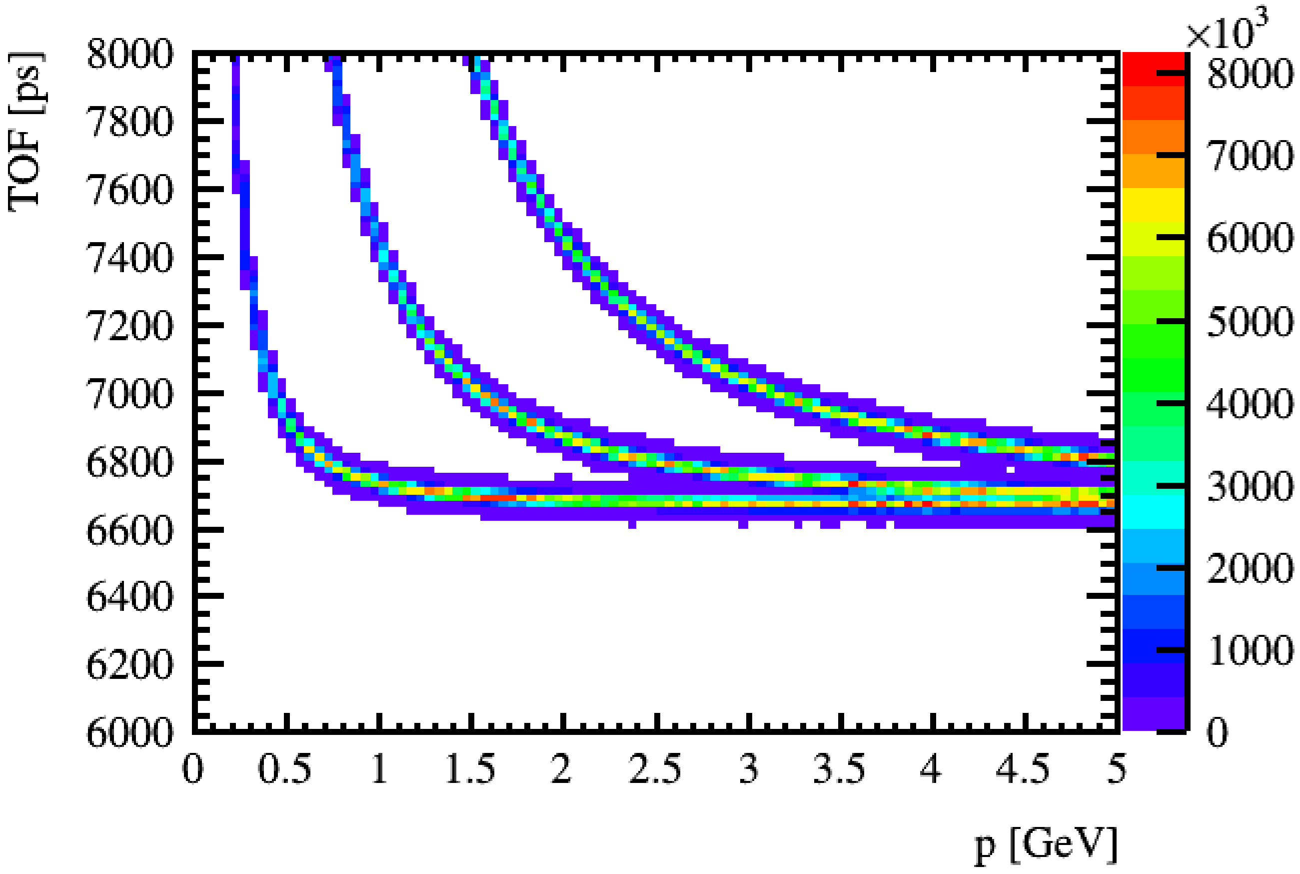
The hype spreads, several groups (10 ps)

4D-tracking in ILD

ILD design and specifications largely ignore the possibility of TOF for PID

Should we re-think the role of the time dimension?

Example of TOF at 2 m from IP versus momentum, with an optimistic 10 ps time resolution



ILD integrated design

4D-tracking → 4D particle flow

Last tracking layer with timing

(SET & FTD7, ETD or first ECAL layer)

Specification: 100 ps, 50 ps, 10 ps?

CMOS proof-of-principle

STAR Heavy Flavour Tagger
Based on MIMOSA CMOS sensor
Operated successfully 2014-2016
Multiple detectors built!

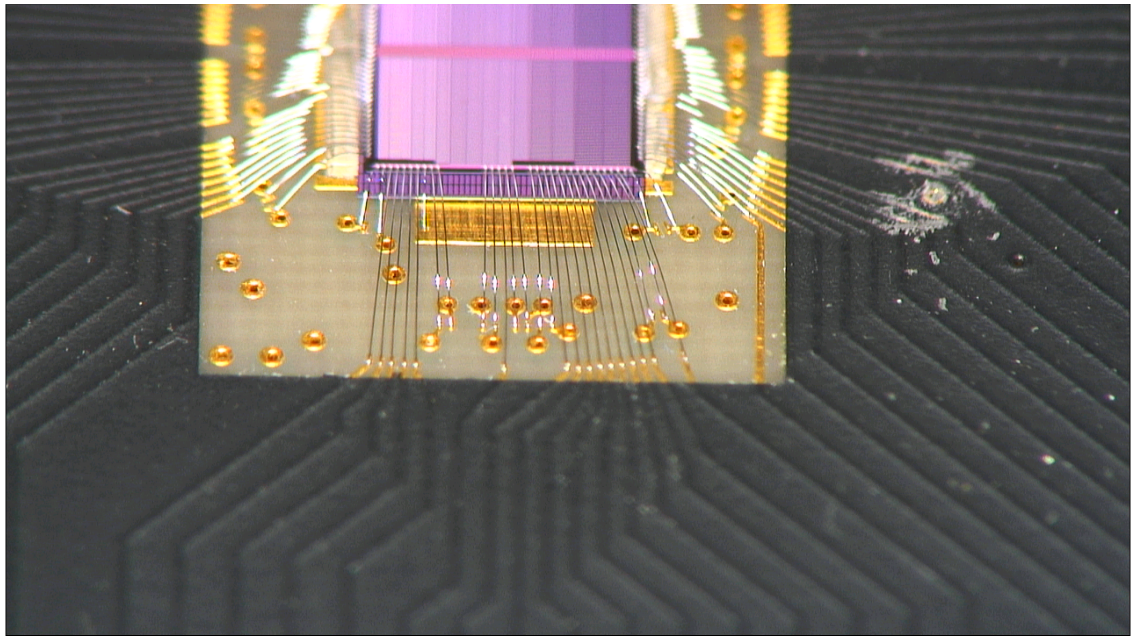
Note: positive experience with air cooling in STAR and Belle II

HVCMOS/HRCMOS

High Voltage or High Resisitivity CMOS process embraced by HEP
→ allows for a sizeable depleted region
→ contained signal, fast collection
→ multiple wells allow for in-pixel functionality

Development now driven by many groups:
ALICE-ITS (ALPIDE@CERN → CLIC)
CBM-MVD (MIMOSIS@IPHC → ILD)
ATLAS upgrade (HRCMOS → ?)
Mu3e...

Can CMOS devices replace μ-strip detectors in the ILD tracker? (SIT, SET, FTD)
CLICdp positively evaluated the possibility of all-pixel CMOS tracker (ALPIDE-based design)

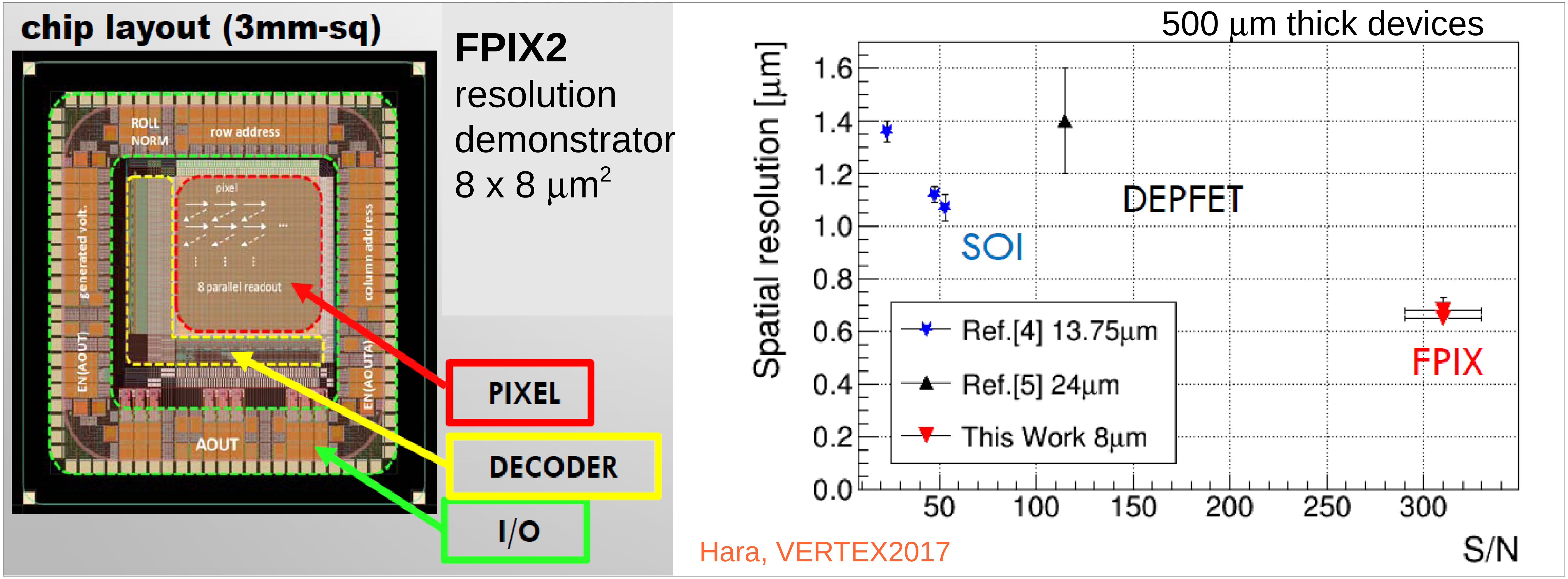


ILD tracking (today)
Strasbourg CMOS MAPs are suited for silicon inner tracker SIT
Extend to SET?

Marcel.Vos@ific.uv.es

Double SOI pixel detectors

Double silicon-on-insulator (DSOI) solves main SOI problems:
back-gating, trapping and cross talk



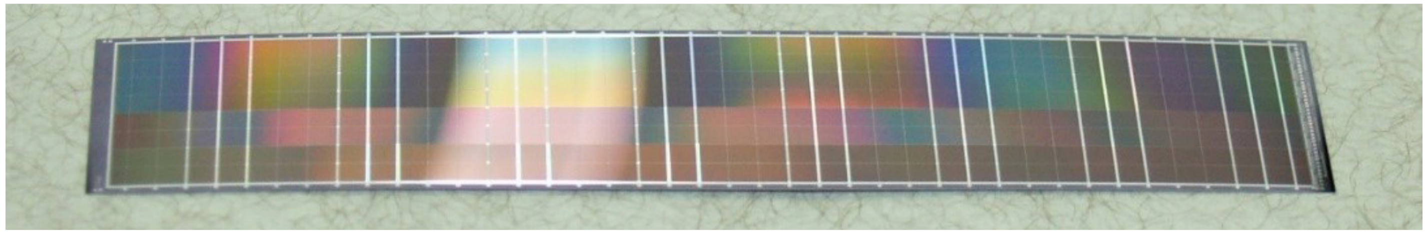
SOFIST: in-pixel time-stamping with 25 x 25 μm^2 pixels

...is anxious to take over

FPCCD

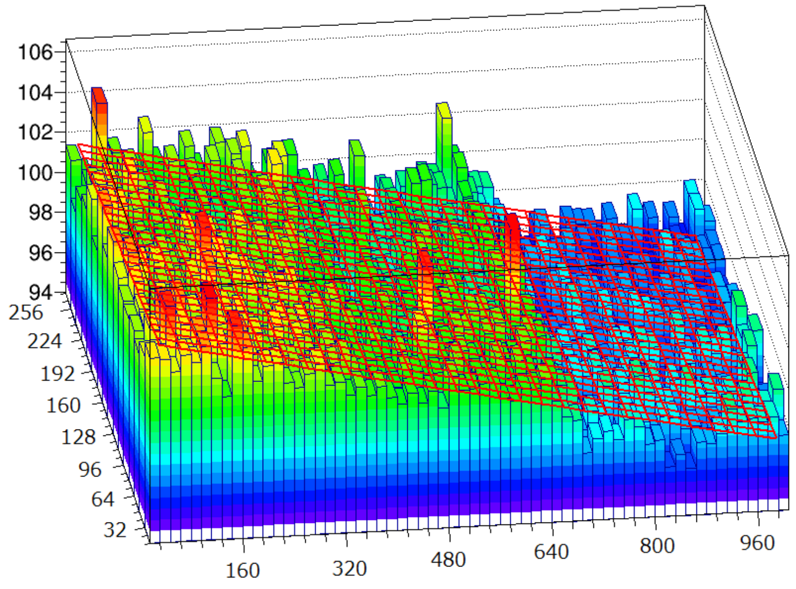
CCDs with extremely small pixels (5 x 5 μm^2):

– granularity makes up for relatively slow read-out



Fabricated by Hamamatsu Photonics, tested at KEK/Tohoku

Cryogenic operation (-40° C) required to reduce dark current → active (CO_2) cooling system



Non-ionizing radiation affects Charge Transfer Inefficiency → neutron irradiation to 2 x 10^{10} n_{eq}/cm^2

yields CTI ~ 6 x 10^{-5}

Can be improved by factor 9 by filling traps (LED illumination) → enough for 3-years at 250 GeV

Marcel.Vos@ific.uv.es

R&D time line

It's still a long time before the ILC experiments install their vertex detector

Technology choice around 2025

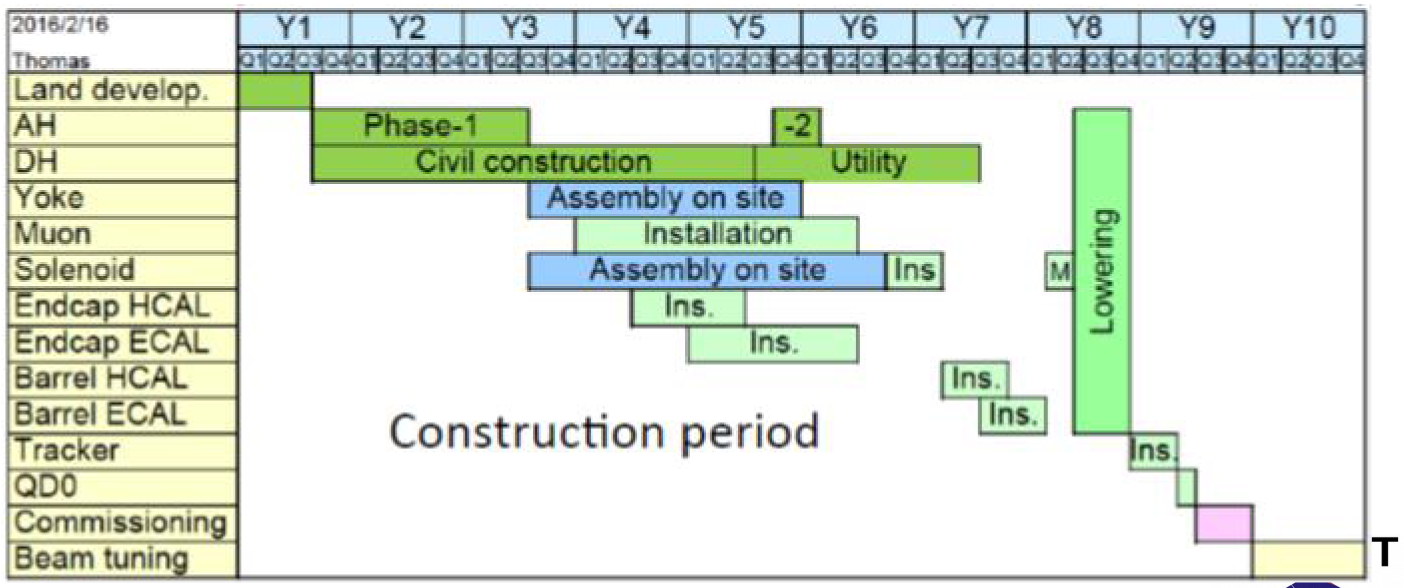
(shoot-out or combination of different technologies)

Emerging technologies have plenty of time to mature

Auguste Besson

–Reverse Calendar:

- Data taking: ~2030-32
- Commissionning / beam tuning ~ 1 year ?
- Integration and vertex detector construction ~ 1- 2 years ?
- chip prototyping/validation/production ~ 2 years
- Technology choice : ~ 2025 ?
- Define the procedure/criteria to chose the technology: several years before ? ~ 2023 ?



Are we still competitive?

Don't take it for granted

While DEPFET was busy building the PXD, the competition has made progress:

- MAPs are "proven" technology
- depleted MAPs are fast
- (double) SOI has working small-scale prototypes

A technology decision is not expected until ~2025

There is time for others to mature, and for DEPFET to react

- Detailed ILC detector design (barrel + disks)
- Renewed R&D (improved core performance, integrated cooling, ….)

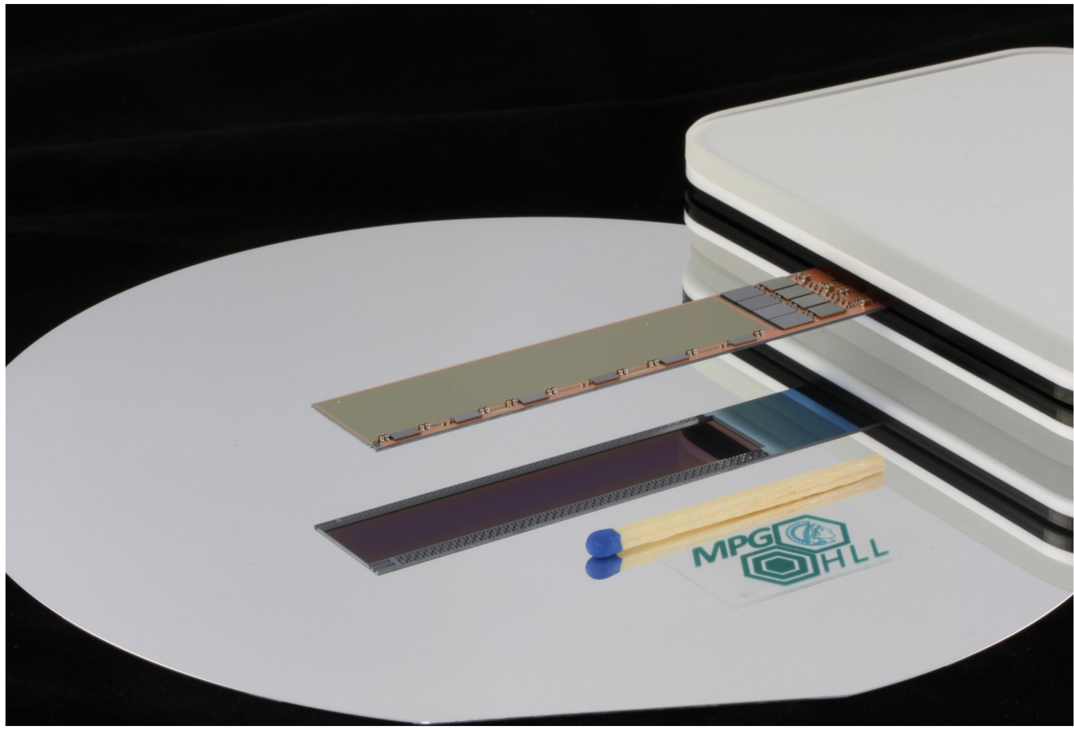
Are we still competitive?

Strengths:

Integrated detector concept (all-silicon ladder)

In-house production → in our hands

Proven technology (after PXD)



Weaknesses:

Read-out speed (rolling shutter)

In-house production → inaccessible

Complexity (can we make DEPFET more user-friendly?)

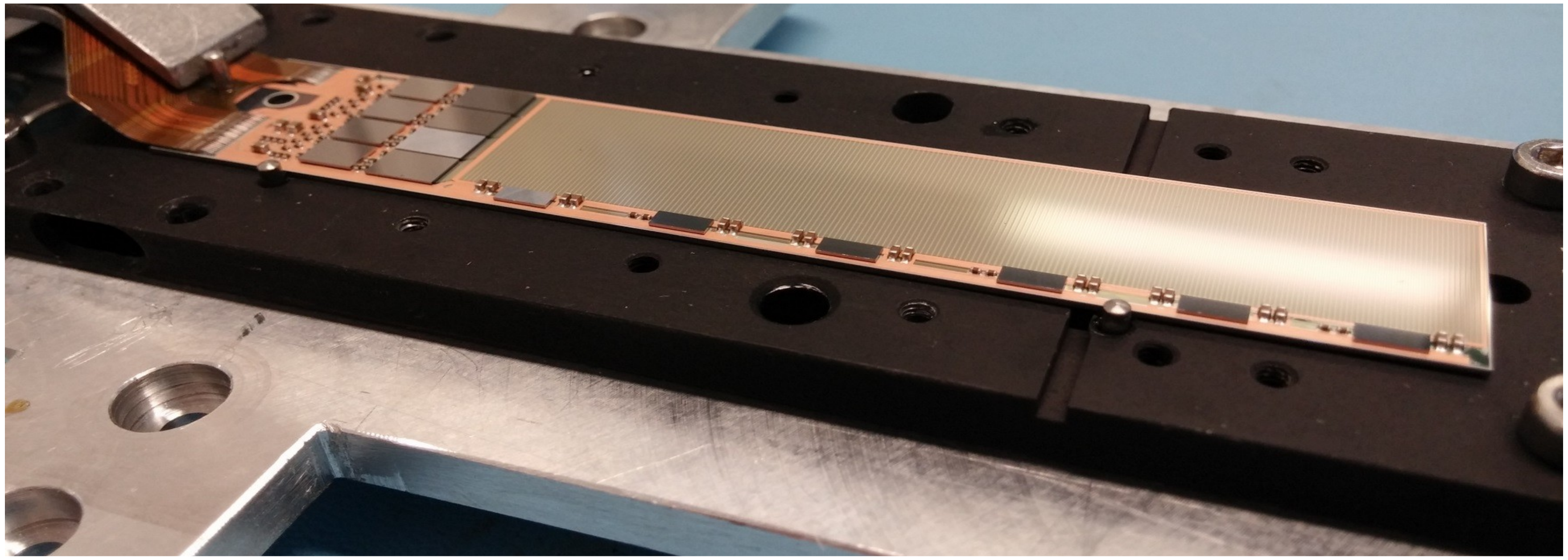
Power consumption?

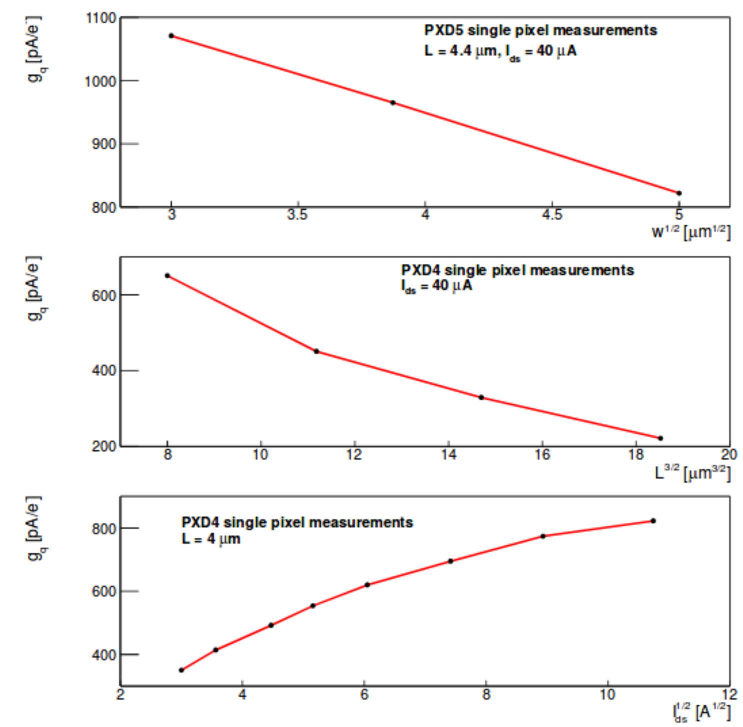
Return to the drawing board, using the lessons learnt in PXD production

DEPFET v2.0

Belle II PXD meets most requirements. And we know we can meet the others...

Can DEPFET improve further?



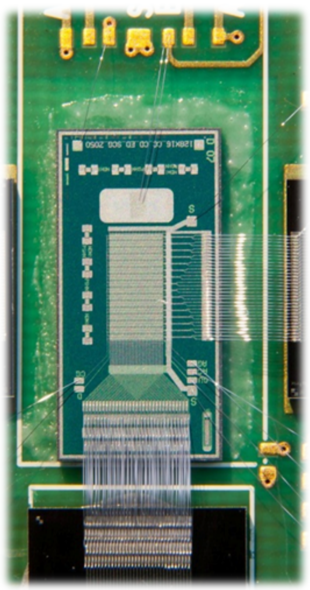


- smaller gate length (upgrade lithography) ---> higher g_q, less DCD power
- read-out speed (+//, +metal, faster sampling) ---> crucial
- forward coverage ---> adapt ladder to disk geometry
  ---> reduce end-of-ladder area/material
- advanced cooling (MCC) ---> especially in DC machines

Marcel.Vos@ific.uv.es

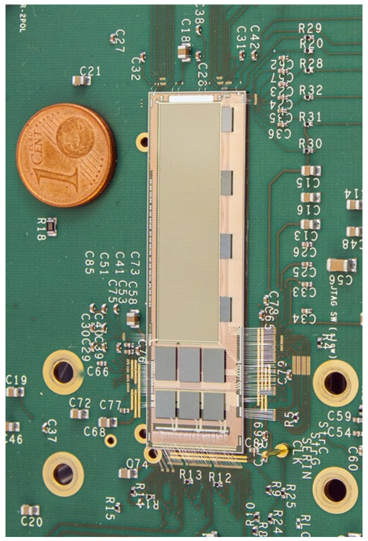
DEPFET time-line

"Early days"



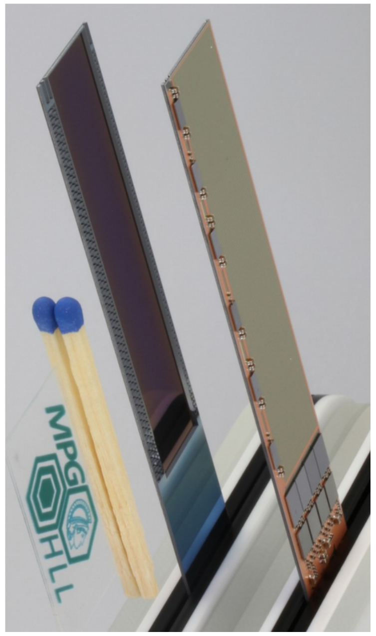
2007-2011 prototypes with $O(10^3$-$10^4)$ pixels

"The most complex piece of silicon in the world", ECFA review



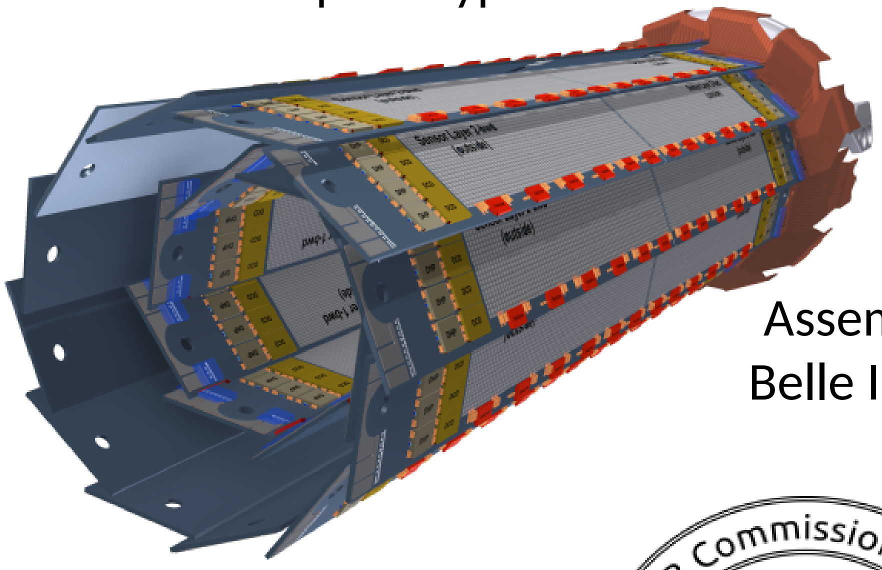
January 2014, first large-scale, multi-ASIC ladder at DESY TB

"The real thing!"



October 2015, first complete & operational Belle II ladder

The Belle II VXD
"a 30% ILC prototype"



Assembly Belle II VXD

SuperKEKB Commissioning Detector BEAST II 獣 Belle II Collaboration

Belle II upgrade

Proof-of-principle | Complete demonstrator | A real detector | Physics

2002.... | 2007.... | 2013 | 2014 | 2015 | 2016 | 2018

a vertex detector for TESLA

LC-specific detector R&D

ILC design & R&D

Small-pixel prototype with 1.5 µm resolution

DEPFET for ILC, IEEE TNS 60, 2, 2

ECFA review: http://ific.uv.es/~vos/ECFA_DEPFET.pdf

DEPFET

ILC candidacy benefits from developments for Belle-II

Wrap-up

The ILC remains a viable option for the future of HEP in the post-LHC era

Staged (descoped) project "Japanese Higgs factory" has received support of JAHEP and ICFA

Decision before the European strategy update

DEPFET remains a viable candidate for the vertex detector and forward tracking disks

The competition has made progress, we have to improve too

Must renew R&D process and detailed design effort to revitalize the DEPFET candidacy