Module Testing Summary - Status Update Göttingen

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Overview

1. Mass Testing at Göttingen
2. Comparison: wafer level tests and mass testing
3. Module Optimization Statistics

Mass testing progress

- situation:
  - two setups running in parallel ✓
  - module transport organisation: ok ✓
  - waiting for new modules
  - doing "ring" studies with extended source measurements
- accomplished so far:
  - 16 modules tested (2 IB, 7 OF, 7 OB)
  - 12 grade A, 3 grade B
    1 grade A but not understood noise pattern in DCD3

Comparison: wafer level tests and mass testing

Wafer level tests: nomenclature

polyline short

- short between poly1 (gate) and poly2 (clear-gate) nets
- position of short assessable within limits

→ affacted gate shows normal pedestals but no hit sensitivity starting at the short (constant clearing)

Wafer level tests: nomenclature II

(drain) open

- open in drain line
- position of open not assessable, contacting at row 1 and row 768

→ affected drain shows pedestal ADU 0 starting at the open

(drain) short

- drain line shorted to another drain line
- position of short not assessable, do etching repair step if present, but no re-evaluation

→ drain line with high/low ADU, high/low occupancy, noise?

Module characterization: nomenclature

0-pixel, 0-drain, 0-gate

- pedestal of 0 ADU
- outside of dynamic range, or no current input

$\leftrightarrow$ **open drain line**, not connected gate

255-pixel, 255-drain, 255-gate

- pedestal of 255 ADU
- outside of dynamic range, or high current input

$\leftrightarrow$ **shorted drain**, shorted gate

Module characterization: nomenclature II

noisy

- pedestal fluctuation of > 3 ADU

dead

- no hit sensitivity in source measurement, i.e. occupancy of 0

$\leftrightarrow$ **polyline short**

$\rightarrow$ basis for grading

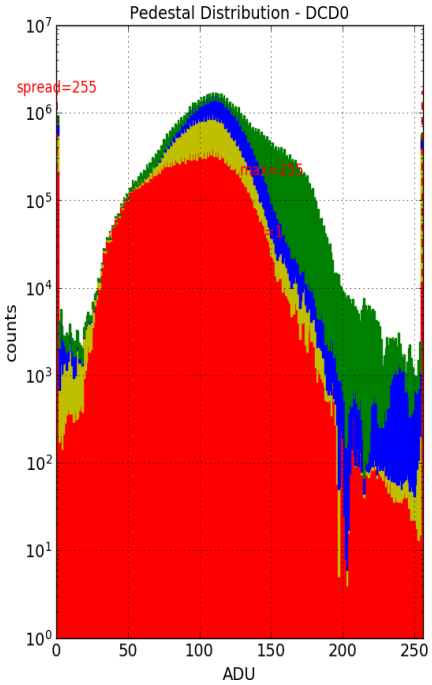
hot

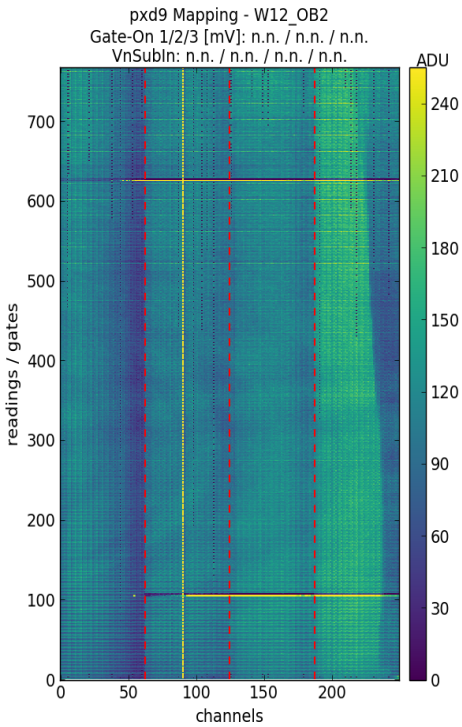
- high occupancy in source measurement $> 10^{-3} - 10^{-6}$

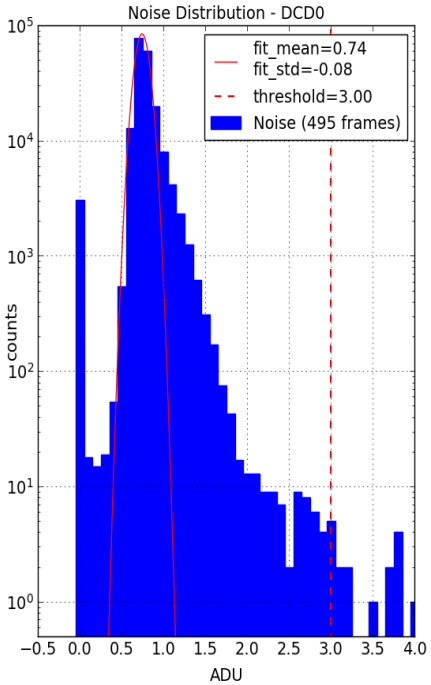
Comparison example: W12_OB2 - Wafer level tests

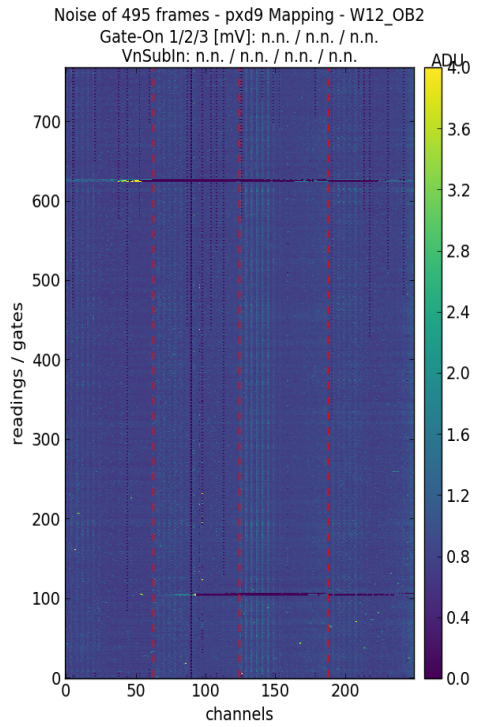
- polyline shorts: 2
  - → expect 2 (semi-)dead gates
- drain opens: 0
  - → expect no open drain lines
- drain shorts: 2
  - → expect up to 4 problematic drains (255-drains, dead drains, hot drains)

Comparison example: W12_OB2 - Pedestals



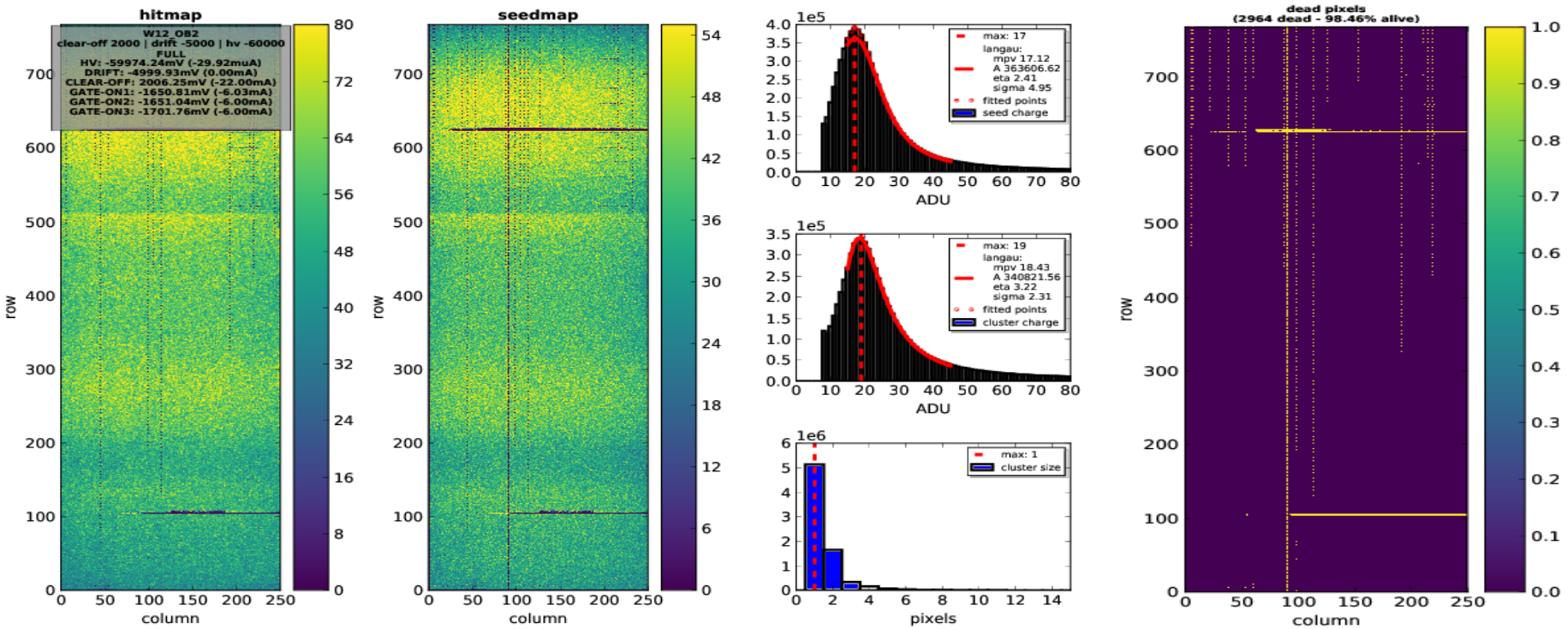






- **23 0-drains!**
- 2 255-drains
- 4 0-rows (pairs of 2)
- 3 255-rows next to 0-rows (due to DCD input fluctuation?)

Comparison example: W12_OB2 - Hitmaps



- 25 dead drains (23 + 2)
- 6 dead rows (gate 26, 156)
- 6 hot rows (gate 26, 156)
  - polyline short??

→ still 98.46% alive (grade B)

Comparison: modules tested in GOE

preliminary

module	#dead	% alive	poly short	dead gates	hot gates	drain opens	dead drains	drain shorts	hot drains
W03_OB1	2453	98.72	1	1-2	1-2	0	1	0	0
W05_OB1	1530	99.20	2	0	0	0	1-2	0	1-3
W06_OB1	2510	98.69	2	1-2	0-1	0	1-6	0	1-4
W08_OB2	697	99.64	1-2	0	0	0	**13**	0	0
W09_OB2	918	99.52	1-2	6-8	0	0	5	0	0
W12_OB2	2964	98.46	2	2	1-2	0	**25**	2	(**0**)
W46_OB1	209	99.89	1-2	0	0	0	1	0	0
W11_OF2	3277	98.29	2	1-2	0	0	**27-28**	1	(**0**)

Conclusion

- major discrepancy: open drain lines
  - wafer level test limited or drain lines damaged afterwards?
    - etching repair for drain shorts
  - most modules still perfectly fine, module performance ok
- impact of drain shorts not fully clear
- have to understand influence of analog common mode correction, etc.

Module Optimization Statistics

Module Optimization Statistics

procedure

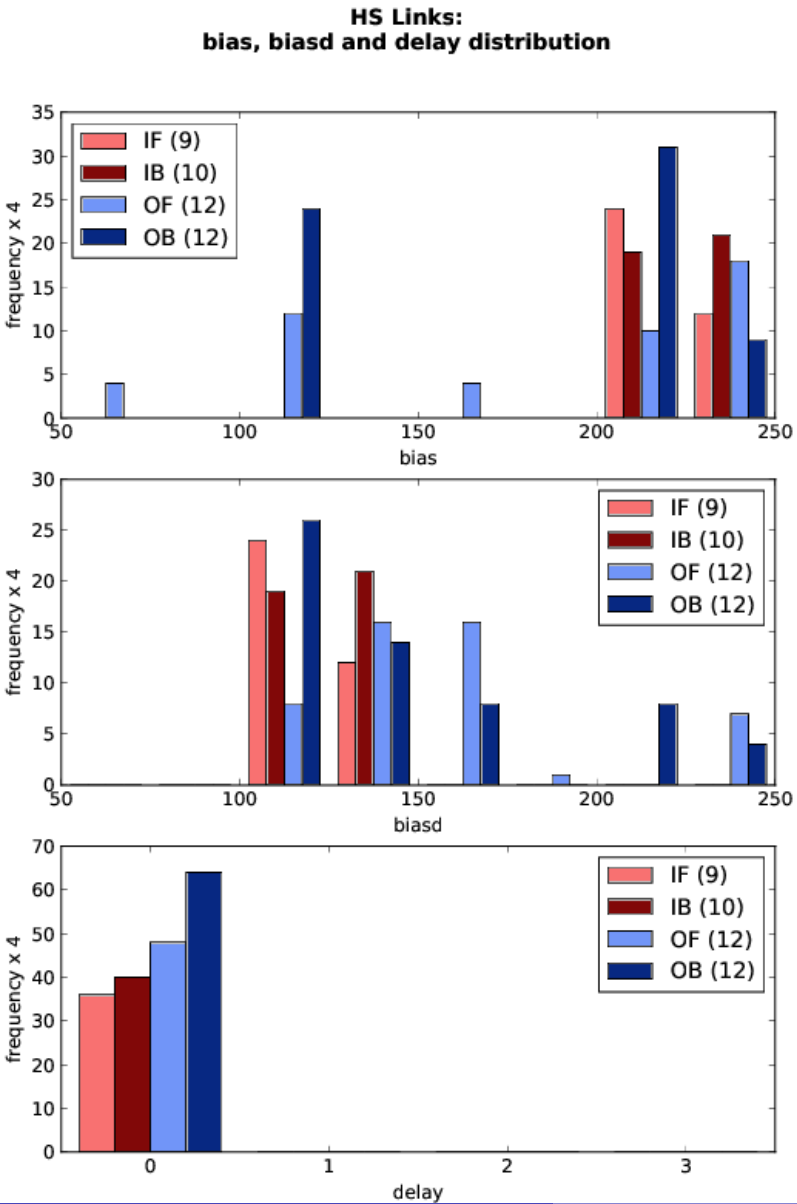
- get list of tested module names, cross-checked with elog
- read configDB file for each module
- retrieve latest commit in *trunk* branch and read PV values

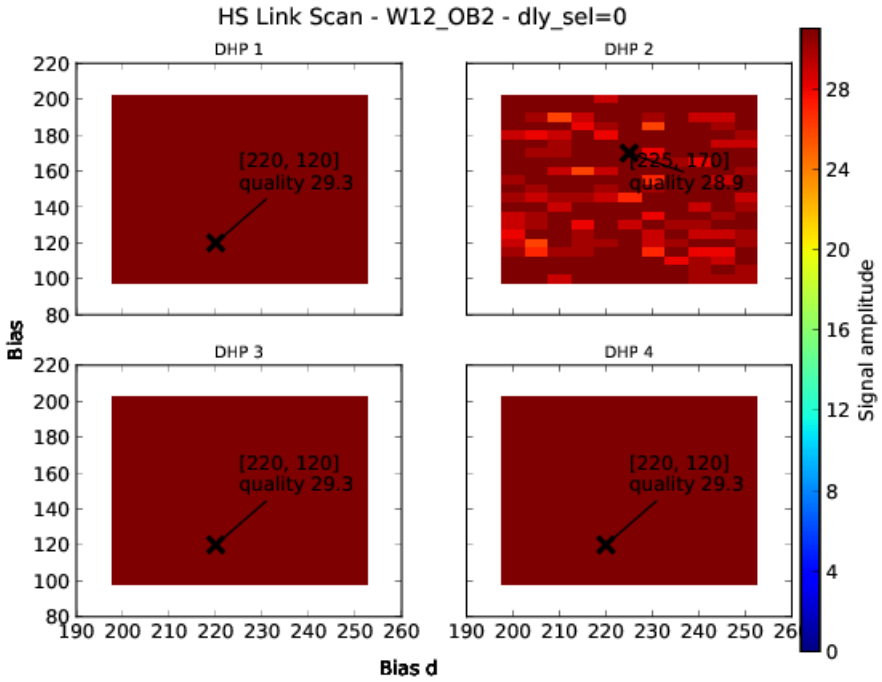
issues

- multiple DHE nodes $\rightarrow$ which holds optmized values?
- no guaranty that latest *trunk* commit holds all optimized values
- optimization procedure changed/improved over time

$\rightarrow$ L1 module results biased

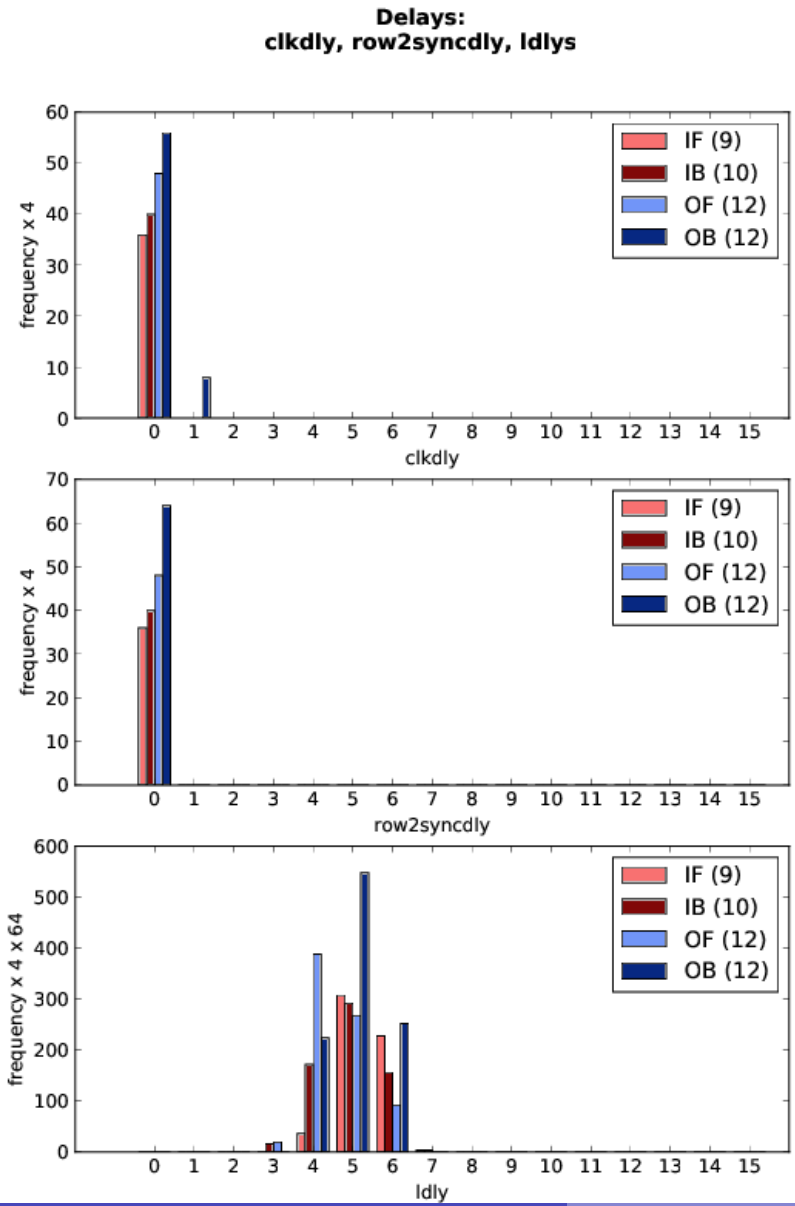
Module Optimization Statistics - HS link parameters





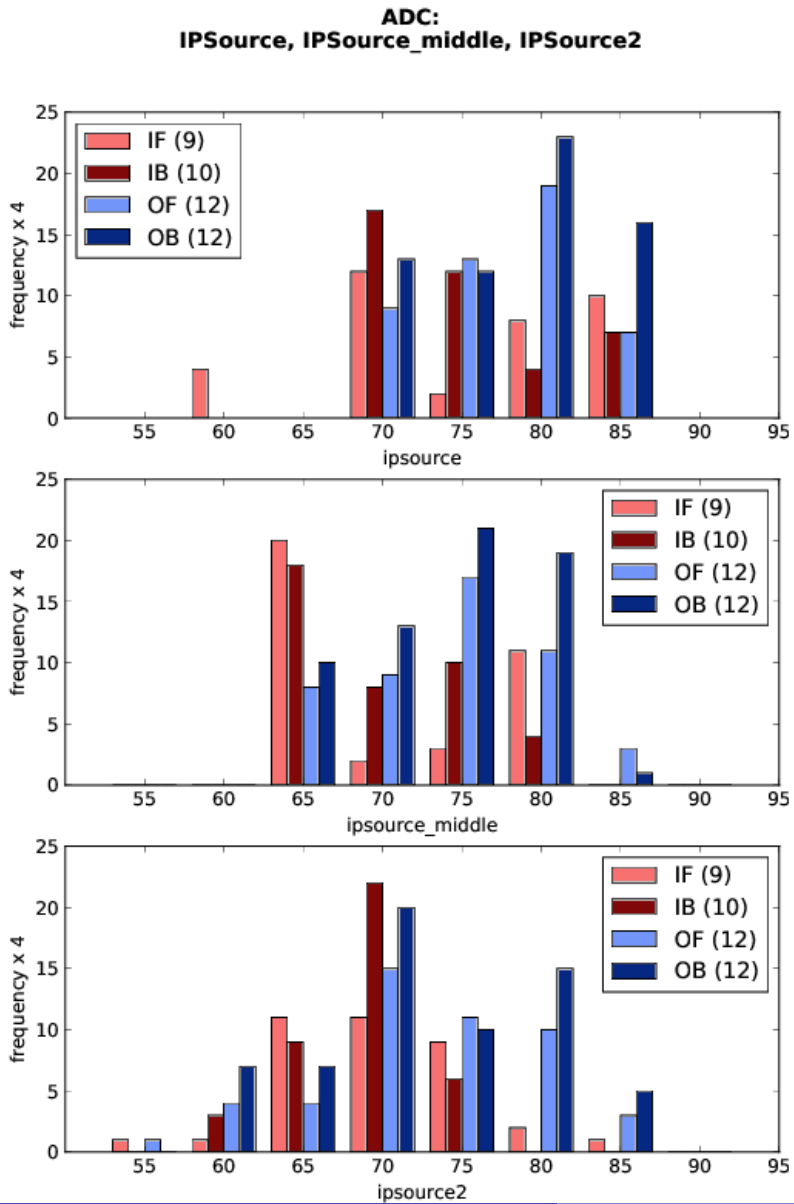
- delay 0 fixed
- no particular sweet spot

Module Optimization Statistics - DCD-DHP data delays



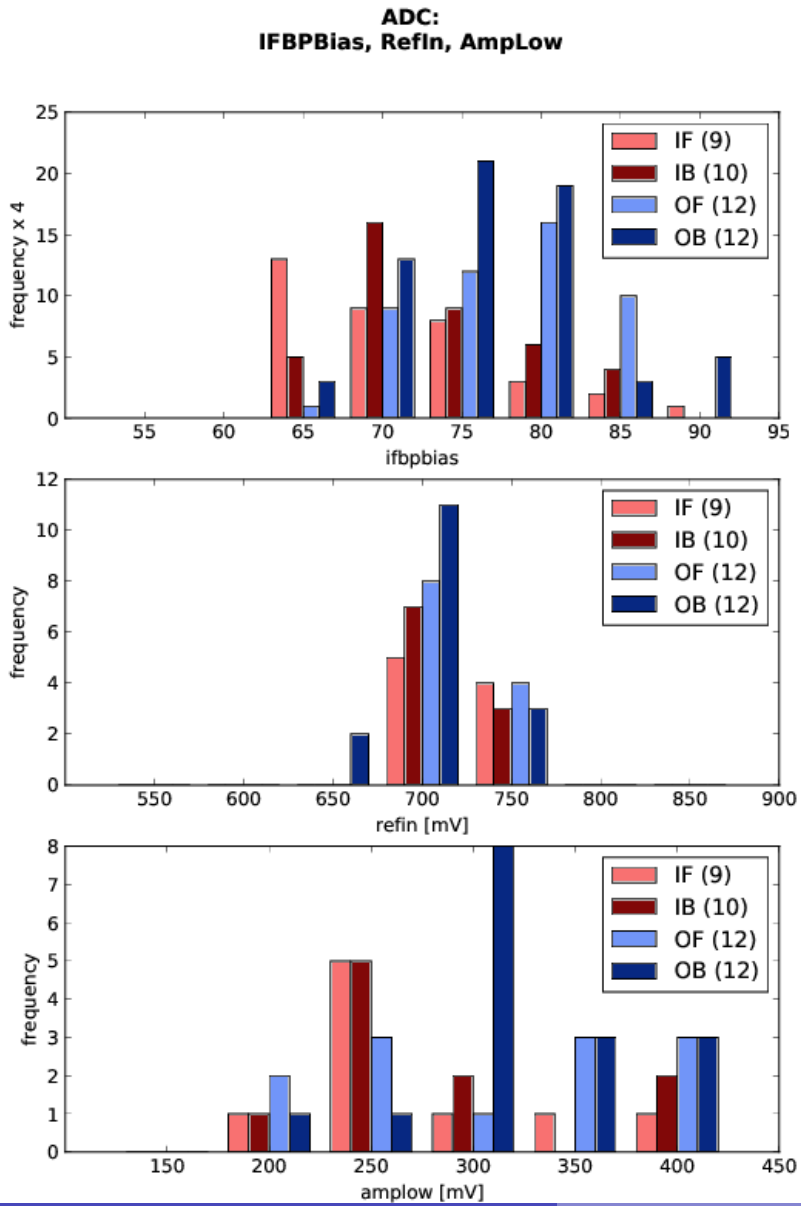
- global delays
  (clkdly + row2syncdly)
  usually fixed to 0
- local delays optimal around 5

Module Optimization Statistics - DCD parameters



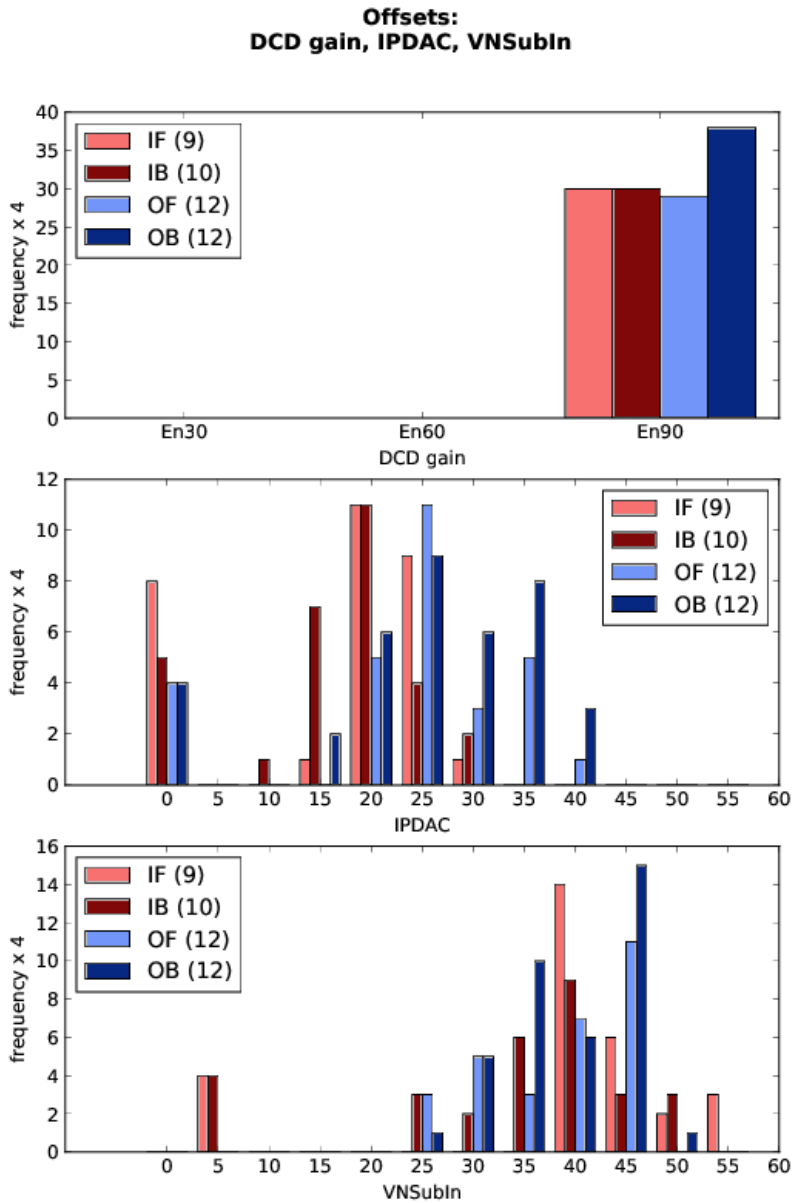
- scan ranges re-defined over time
- working (local) optimum always found
- current scan ranges
  - IPSource 60-85
  - IPSourceMiddle 70-84
  - IPSource2 60-85

Module Optimization Statistics - DCD parameters II



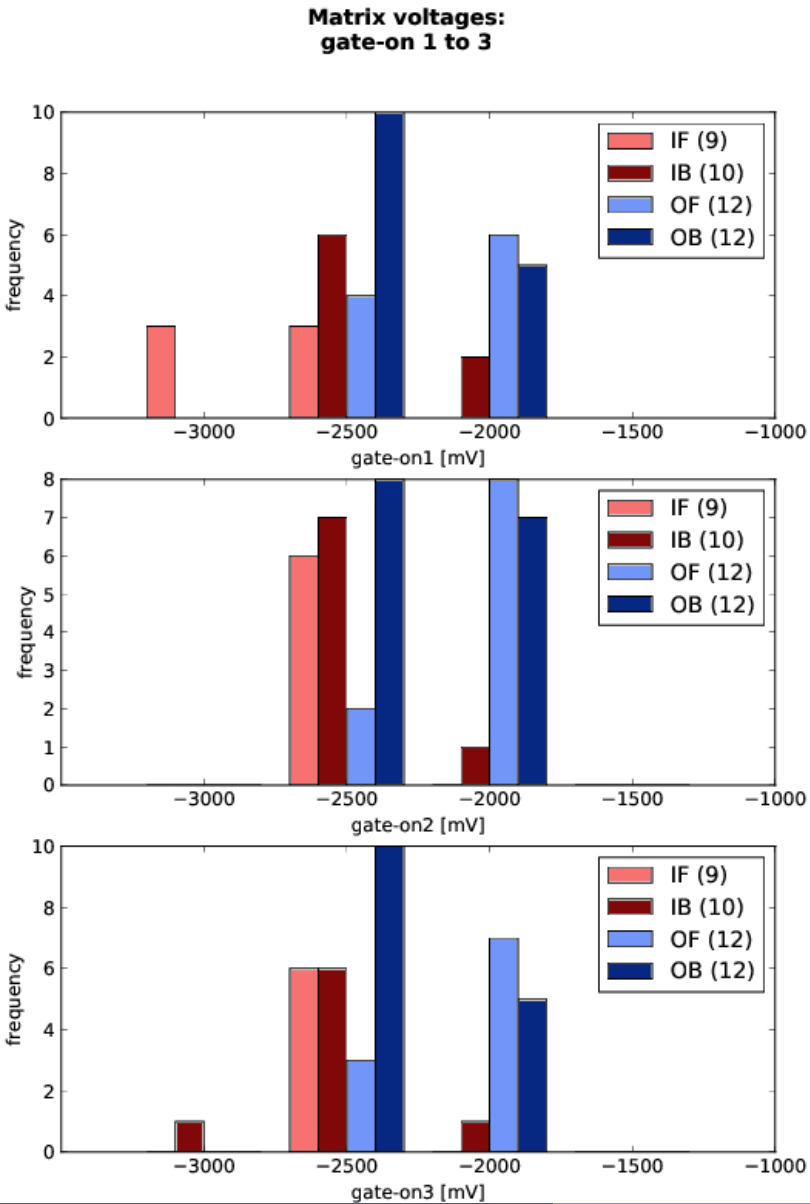
- scan ranges re-defined over time
- working (local) optimum always found
- current scan ranges
  - IFBPBias 60-90
  - Refin 650-750
  - AmpLow 250-450

Module Optimization Statistics - Gain/Offsets



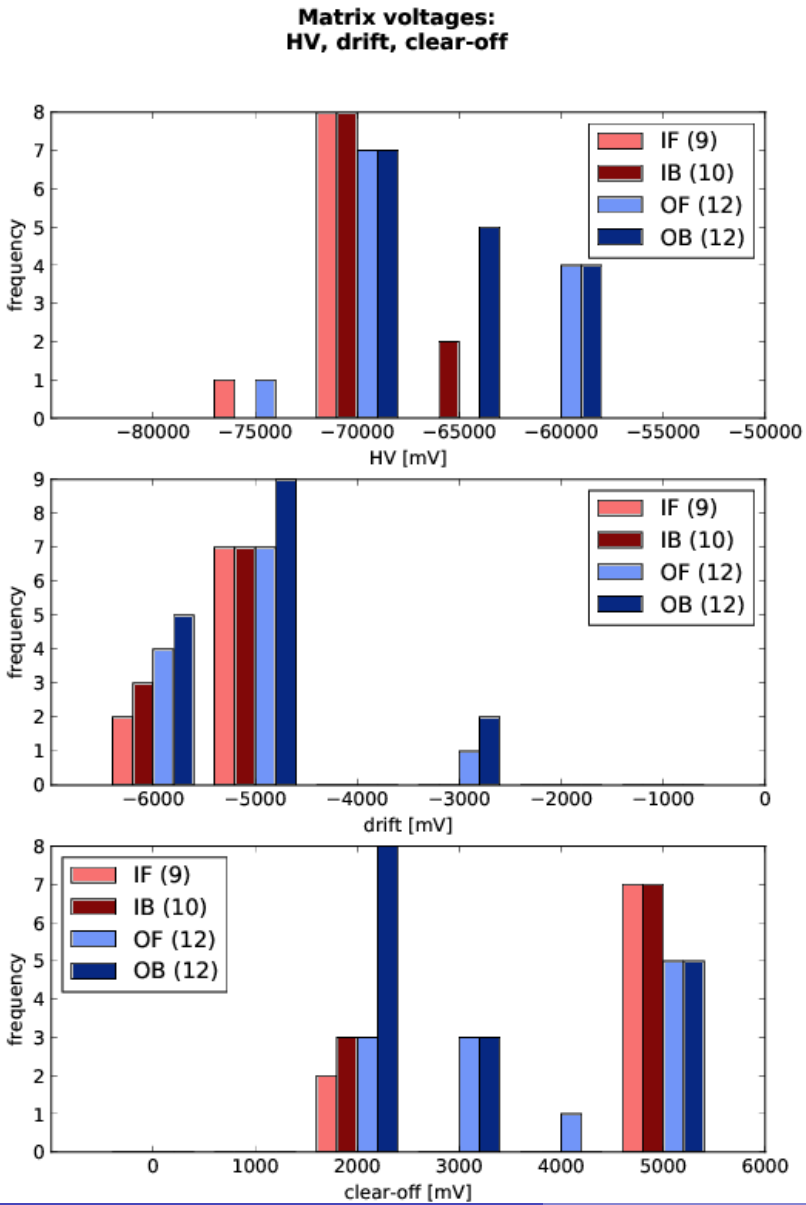
- gain En90 as target
  - *preliminary: needs to be checked!*
- some modules without offset calibration? (IPDAC 0)
- some modules not fully optimized? (VNSubIn 5)

Module Optimization Statistics - Matrix biasing



- gate-on usually limited by pedestal spread (radiation damage and offset calibration capability)

Module Optimization Statistics - Matrix biasing II



- no well-defined, automated optimization procedure available

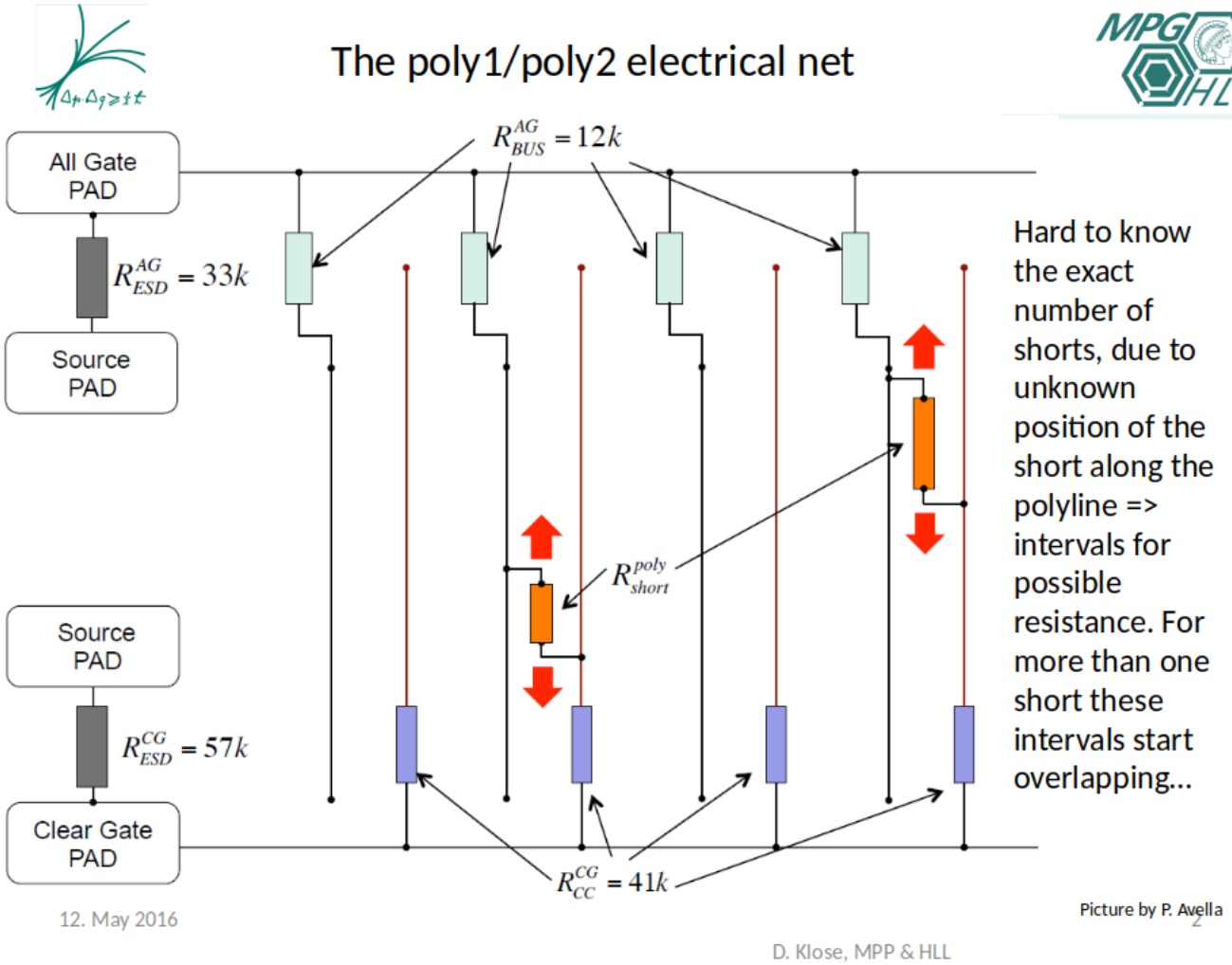
Conclusion

- optimization and characterization procedure successfull on all modules ✓
  - grade B module due to open drain lines, hot and dead gates, ...
- optimal matrix biasing not yet clear

→ need to make sure we collect all optimized settings!

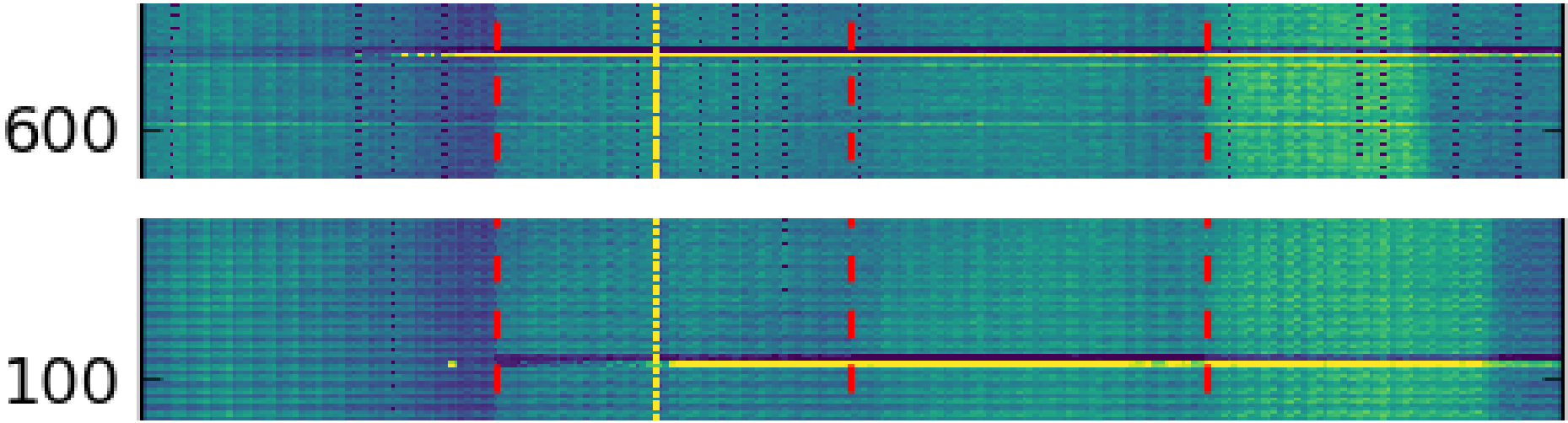
Backup

Wafer level tests - polyline shorts



by Daniel Klose

W12_OB2 gates 26+156 in detail



- both gates show
  - two rows with pedestal close to 0 ADU for DCD2-4
  - pedestal close to 255 ADU for two neighbouring rows
  - within **same** gate

  → polyline short scenario?

ring studies