DHP Test Chip Design Status

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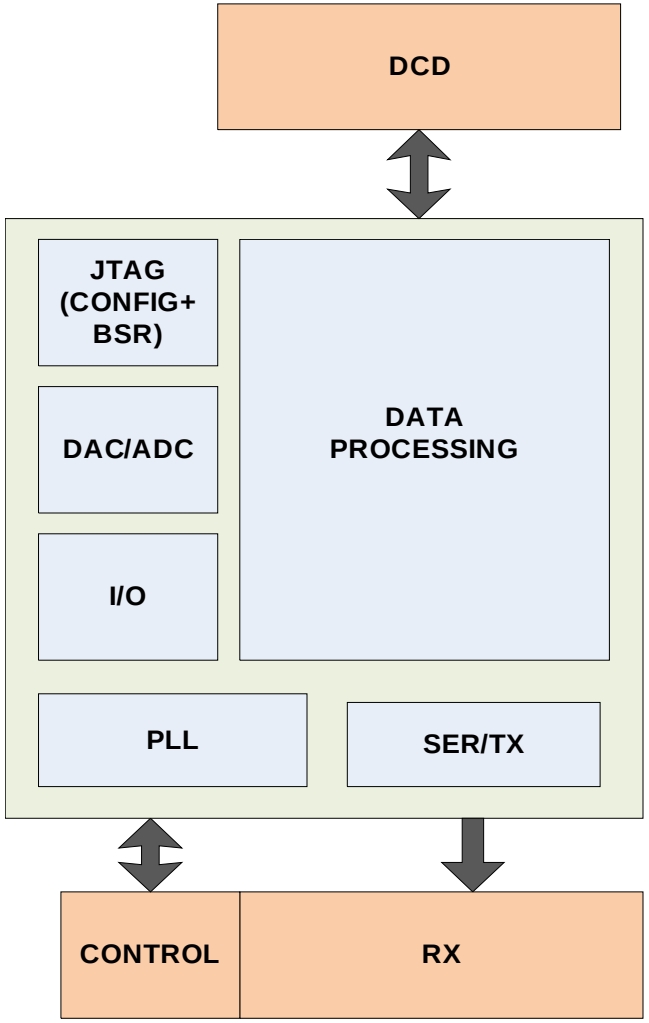
Functionalities

- Record 4x1024 (4 frames) rows of raw data
- Trigger ID – 8bit, Frame ID - 8bit
- Latency up to 1024 rows
- Configuration through JTAG
- Boundary scan
- Temperature measurement (not yet in test chip design)
- On chip clock management PLL (not yet in test chip design)
- Single bit error protected memories + triple redundant registers
- High speed CML output (Aurora protocol)
- 5 operating modes
  - AQUSITION
  - AQUSITION TO MEMORY
  - SEND MEMORY
  - TEST

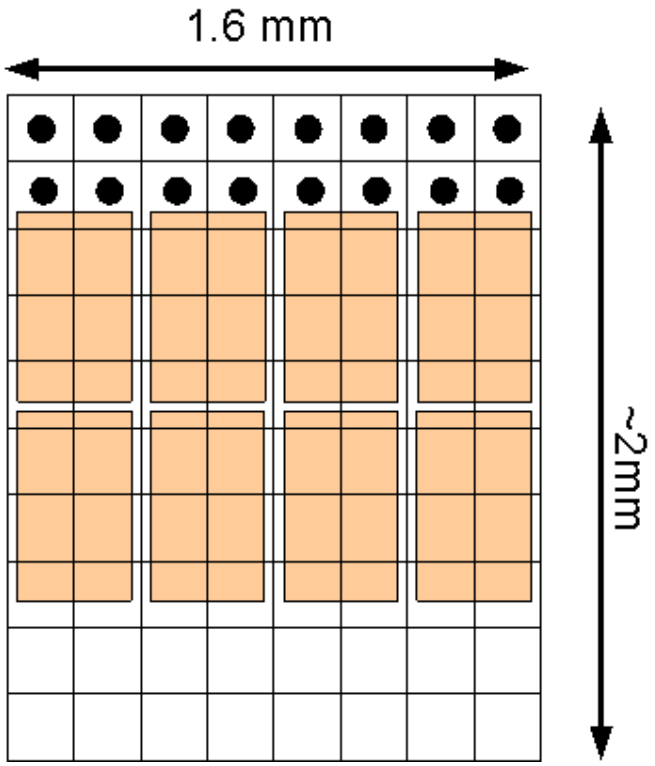
DHP Concept



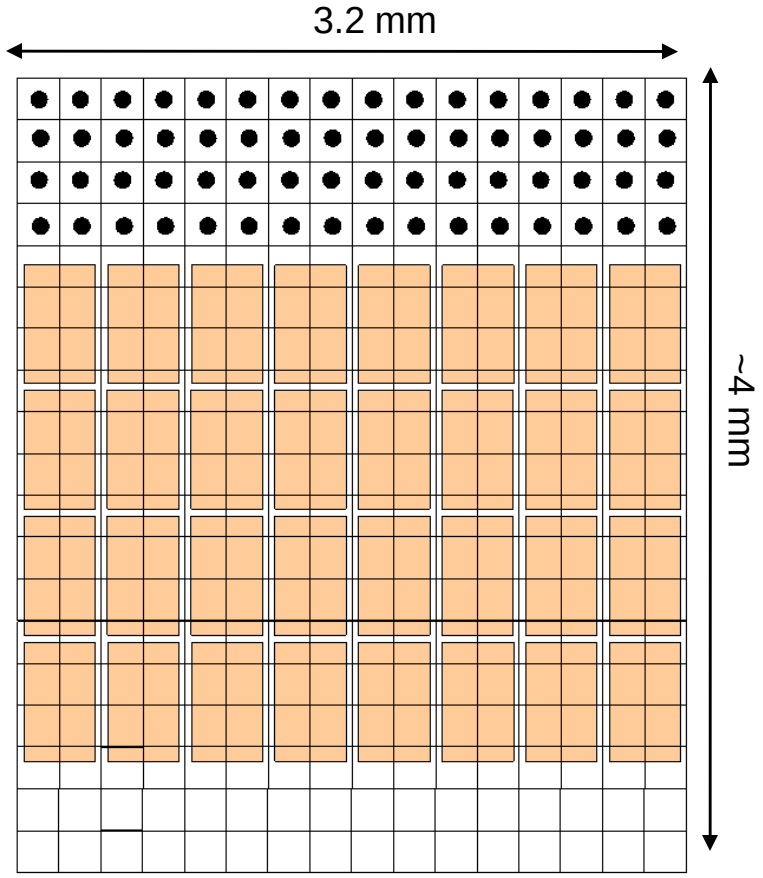
- Main clock 100MHz
- DCD clock 400MHz
- Output clock 0.4-1GHz

Floor Plan

Test Chip (16 inputs)



Final chip (64 or 32 inputs)



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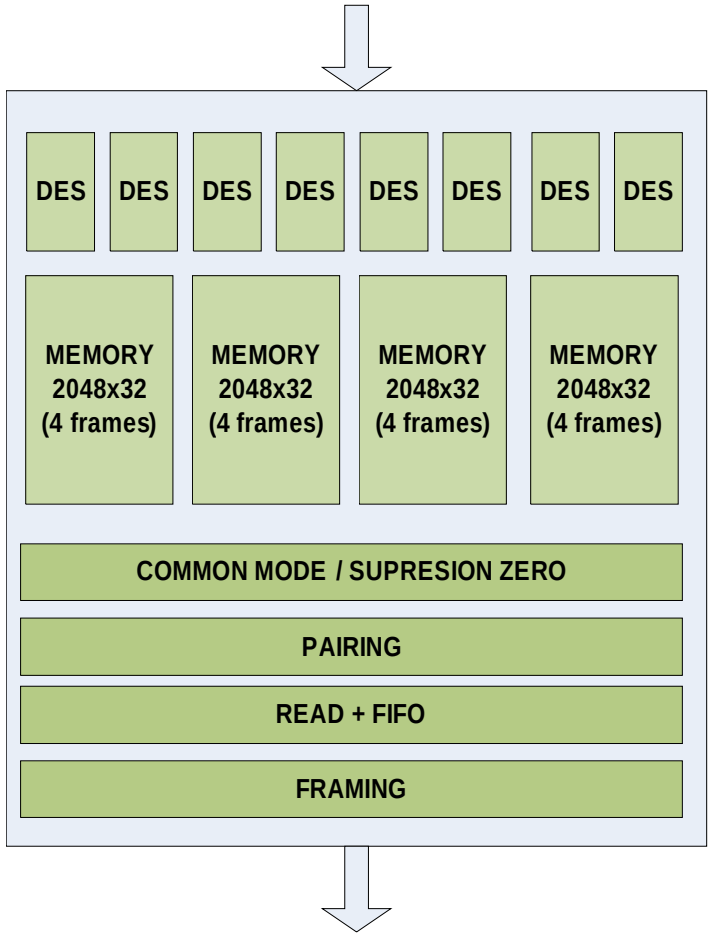
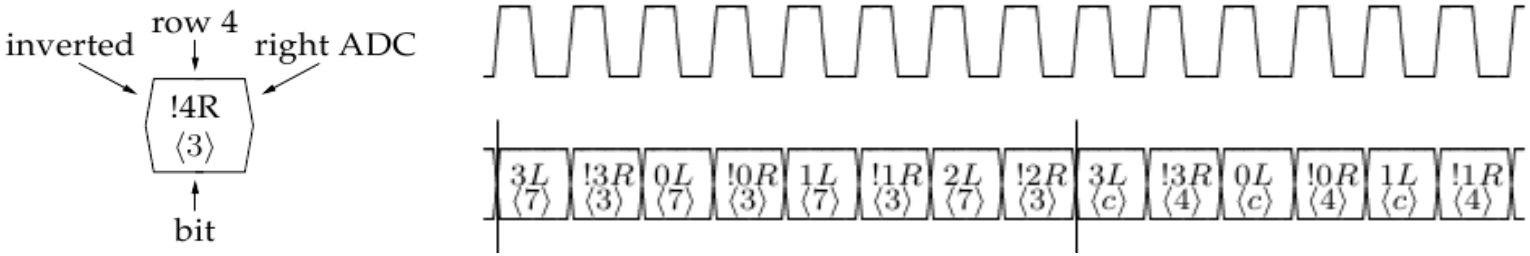
Processing



- 2 de-serializers/inputs share one memory
- Buffering for latency
- Pedestal correction
- Common mode correction
- Hit Pairing
- Readout
- Output framing

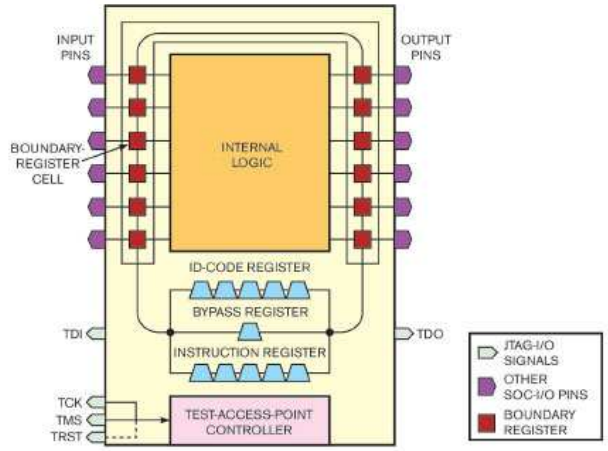
DCD comunication

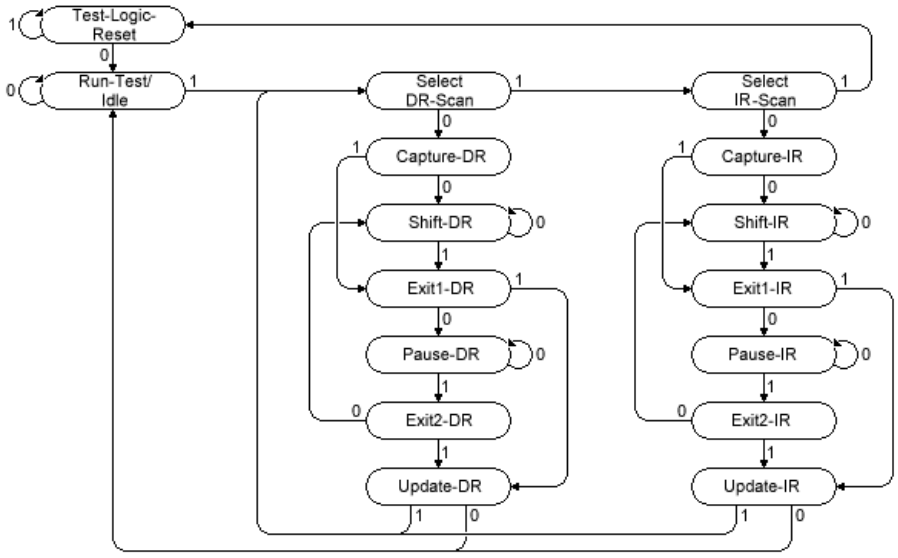


- DHP → DCD signalization
  - clock (400 MHz)
  - row2_sync (~6 MHz)
  - frame_sync ?
- DCD → DHP protocol
  - current code adapted DCD2 output format
  - need to be defined urgently!

Configuration / Control

- **Control signals:**
  - clock (100MHz)
  - frame sync
  - trigger
  - reset
- **JTAG signals (+BSR):**
  - TCK
  - TDI
  - TDO
  - TMS
  - TRST





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Output protocol (proposal)

- Header Data Field (32bit)

field	bits
trigger id	8
frame id	8
chip id	8
flags	8

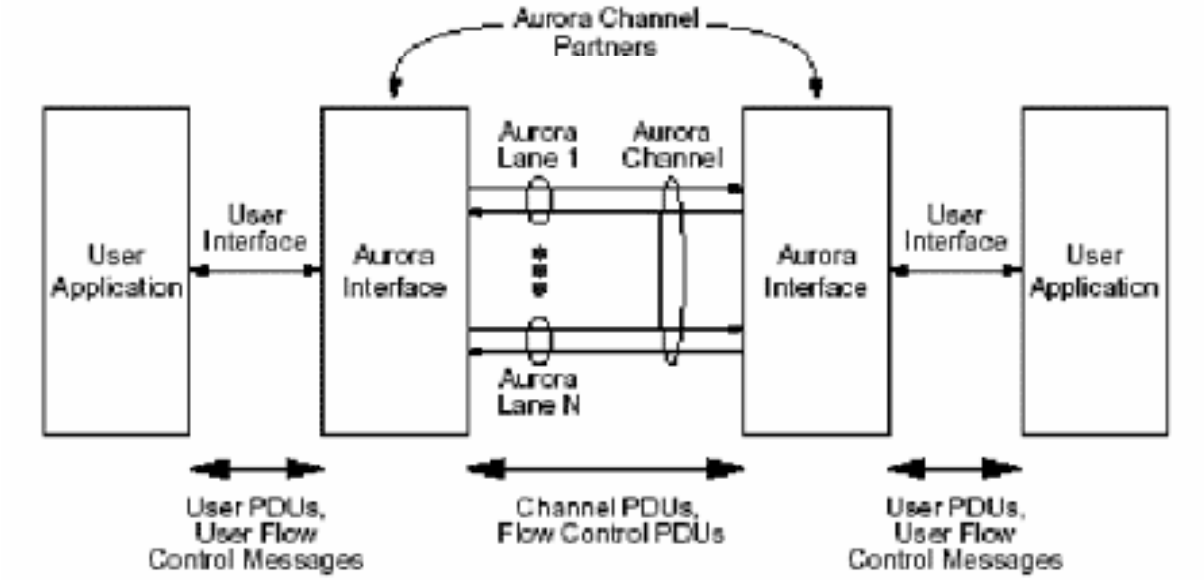
- Hit data fiels (32bit)

field	bits
column	6
row	9
orientation	1
val 1	8
val 2	8

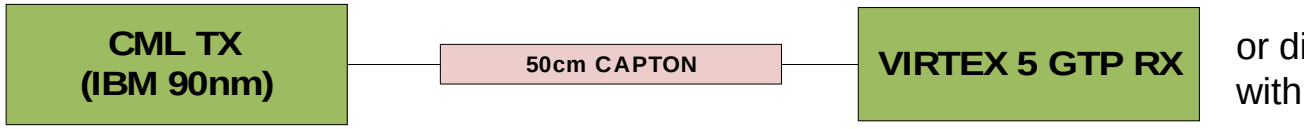
Send after start of frame every 512 rows

Output comunication

- Basted on Xilinx Aurora Protocol
- Tested with Xilinx IP
- Plans for up to 2Gb/s link

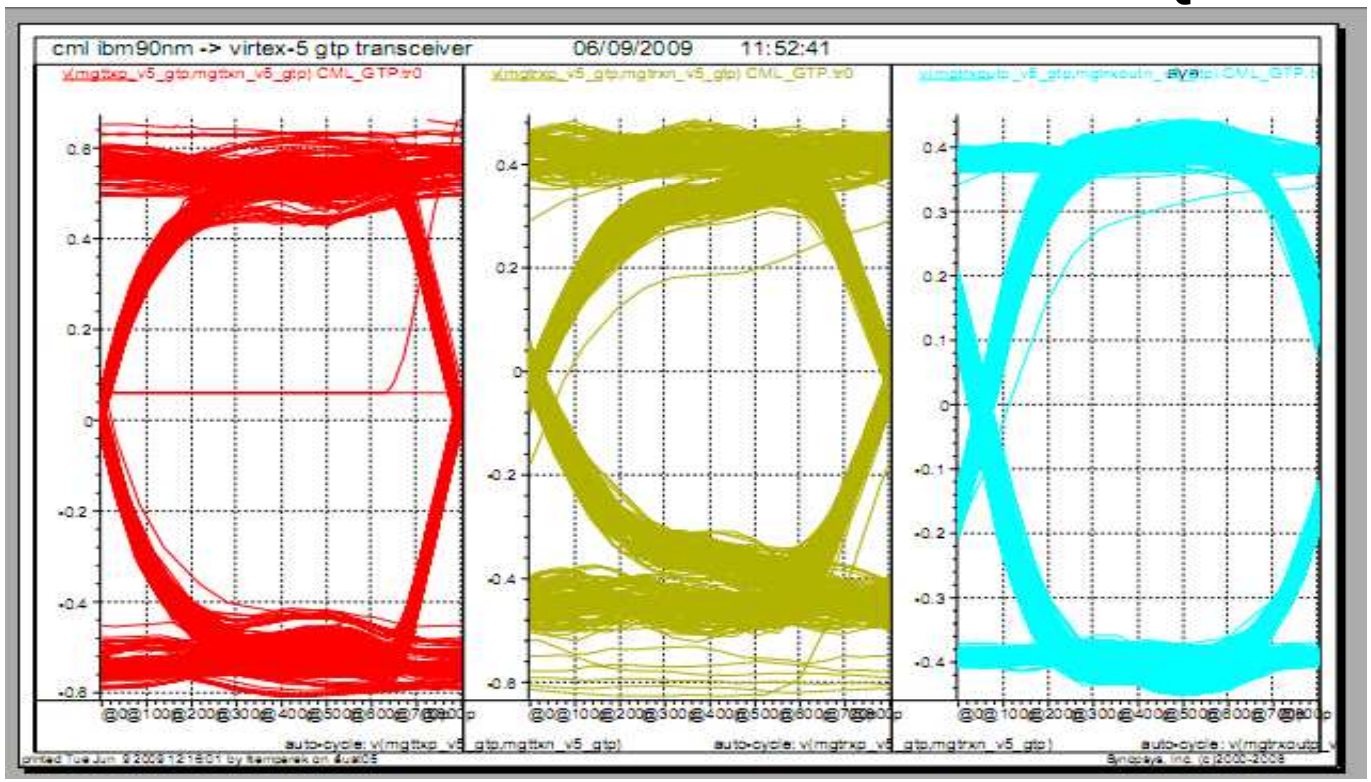


Transmision test (preliminary)



or diff. repeater
with equalizer

TX **RX** **RX EQ**



HSPICE
1.2 Gb/s

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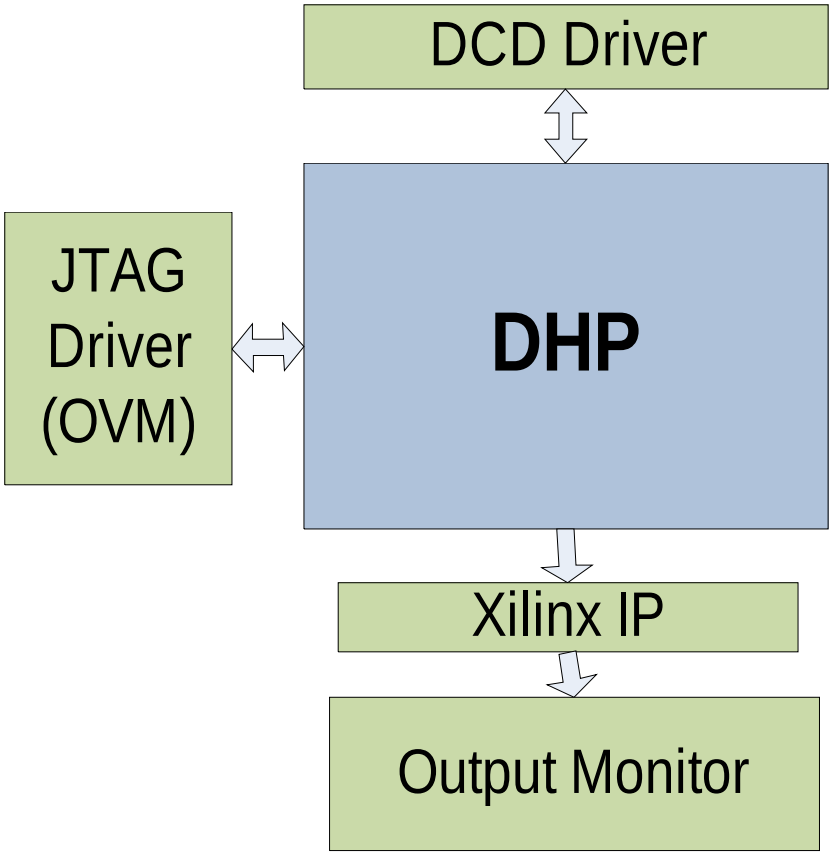
Functional Verification



- OVM verification enviroment (for final design)
- Use of real Xilinx IP for data receiver

Design Status For Test DHP Chip

Block	Status
Digital Core	- RTL almost finished - verified basic main functionalities (need resources :-) - first synthesis and formal verification OK ! Need final spec for DCD communication
Framing & serializer	- RTL done - verified (with Xilinx AURORA IP)
LVDS_TX/LVDS_RX	- Schematic implementation and simulation ongoing
Low Swing Receiver	- Schematic & simulation done
CML_TX	- Schematic & simulation done, layout in progress
PLL	- Pending (may come too late for this submission)
DAC/ADC	-

Submission 26.10.2009

First power estimation (digital core only)

- 16 DHP input (64 DCD inputs)
- Done after synthesizes (DC) with wire load modeling

```
Cell Internal Power  =  44.2962 mW   (84%)
Net Switching Power  =   8.7248 mW   (16%)
                         ---------
Total Dynamic Power     =  53.0210 mW  (100%)

Cell Leakage Power      =  70.2054 uW
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More precise results in 2 weeks