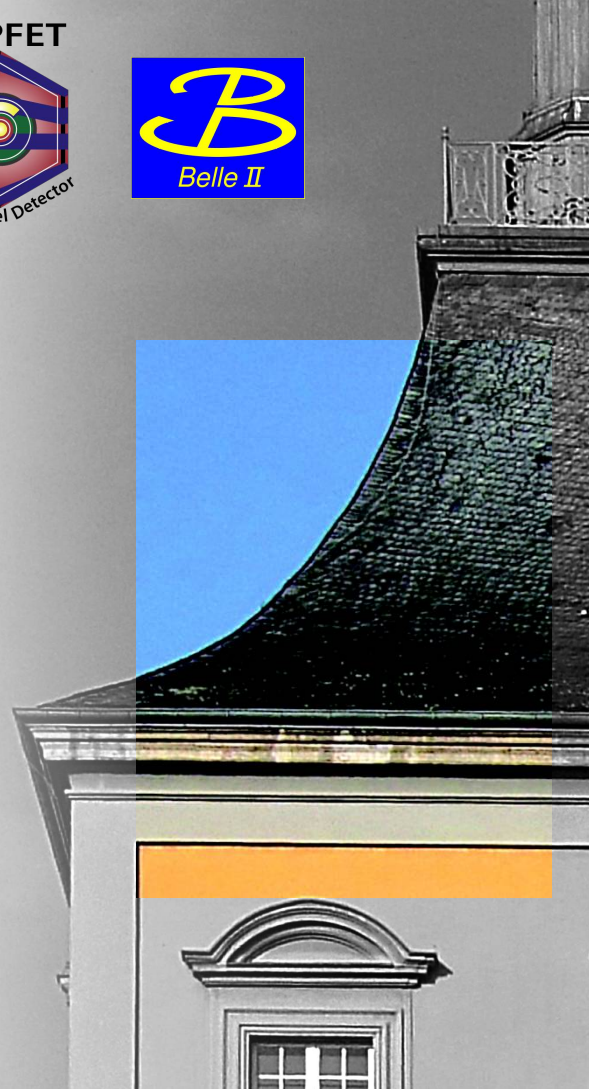
UNIVERSITÄT BONN

SI LAB Silizium Labor Bonn

bmb+f - Förderschwerpunkt Elementarteilchenphysik Großgeräte der physikalischen Grundlagenforschung

DEPFET Active Pixel Detector

Belle II



BOTHO PASCHEN FOR BELLE II PXD

OVERVIEW OF PXD MODULE SOFTWARE

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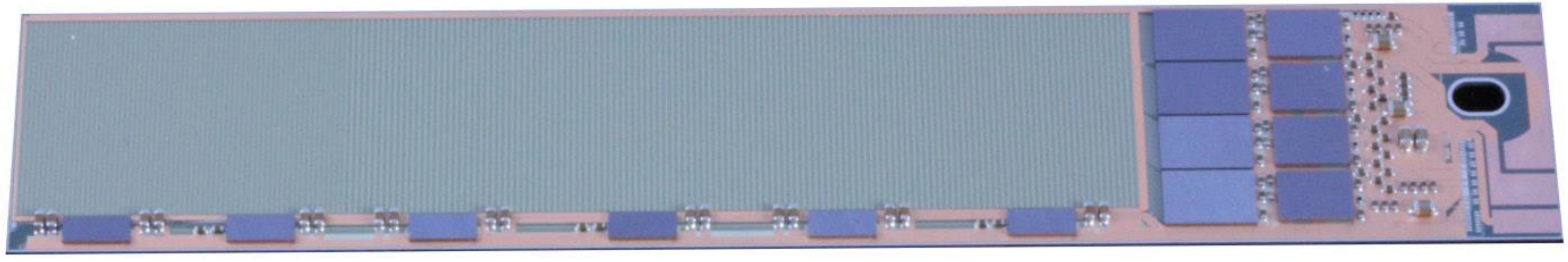
SCOPE OF THE MEETING

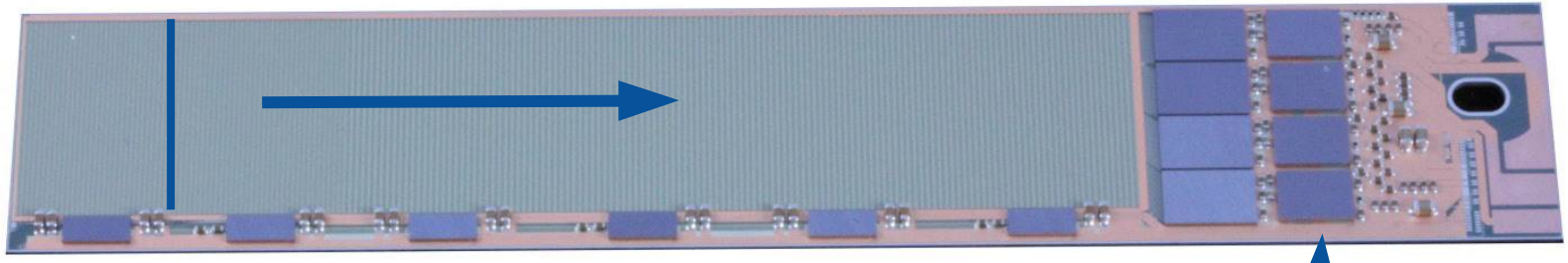
- Overview of the system and all software components
- Current status and development
- Hands-on session and discussion at the DESY setup



PXD MODULE

Drain Current Digitizer (DCD)
4 ASICs, 256 ADCs each

DEPFET matrix
768 x 250 pixels



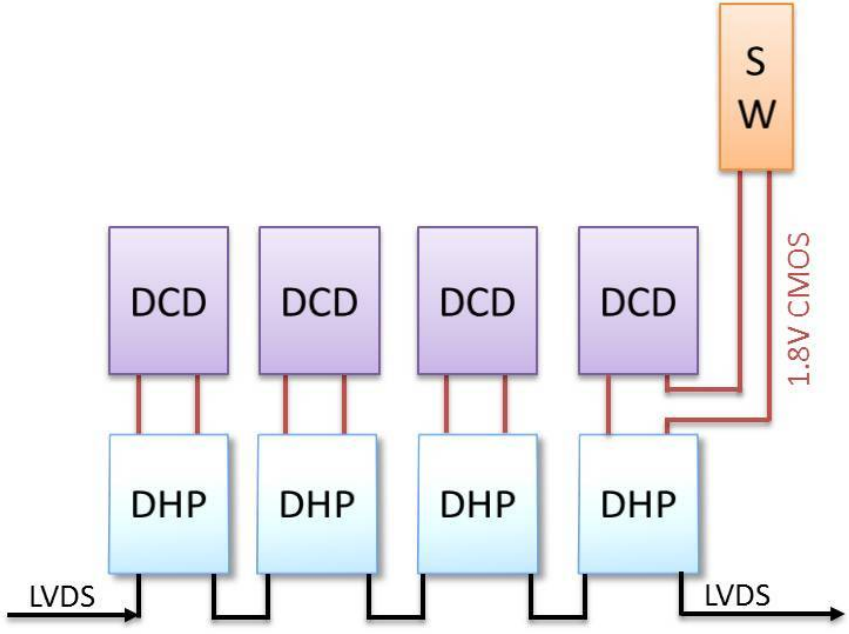
6 Switcher ASICs
- control readout cycle

Rolling shutter readout
- 4 pixel rows at a time
  aka. “gate”/”electrical row”

→ 1 full frame = 192 gates (20 us)

Data Handling Processor (DHP)
4 ASICs, 1:1 corr. with DCDs
- zero suppression
- data output

ASICS: JTAG



- Chain configurable in DHPs

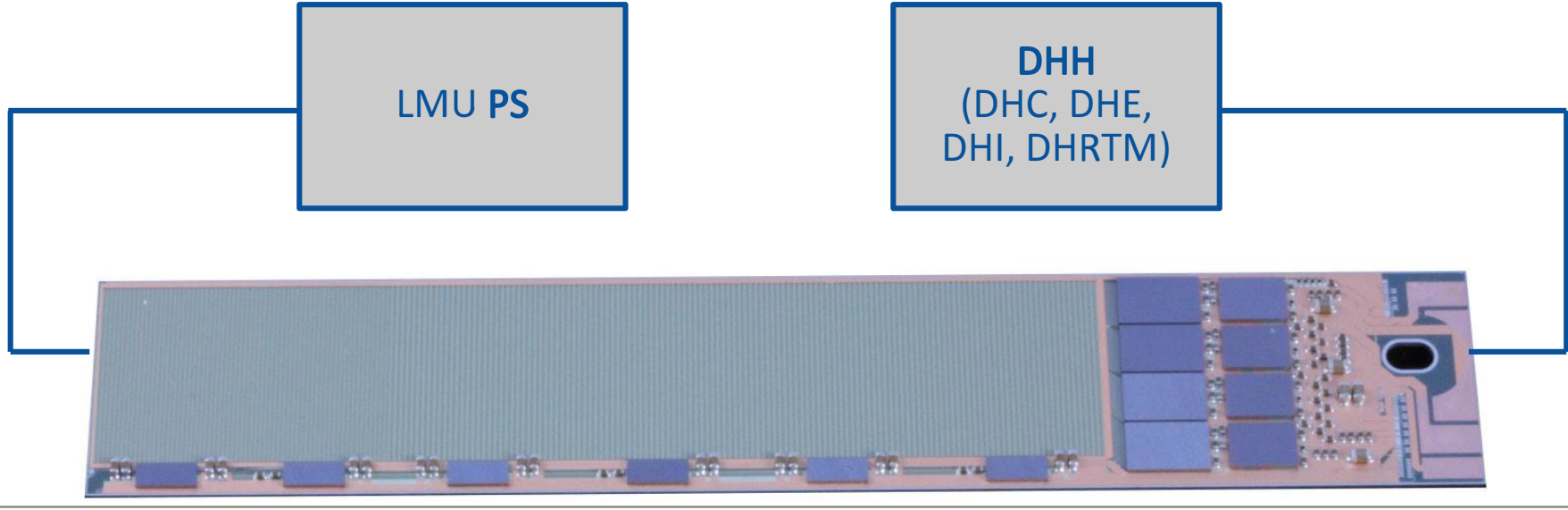
dcd_jtag_en_out

- **JTAG** for slow control (writing registers)
- Switcher JTAG: unimportant
- DCD registers
  - ADC and current tuning
  - Enable/Disable analog part
- DHP registers
  -

Memory	raw-data	pedestal	offset	switcher
Size [kB]	128	128	32	16

SERVICES OF THE SYSTEM

- Power and matrix bias: LMU Power Supply (PS)
- Readout and ASIC control: Data Handling Hub (DHH)



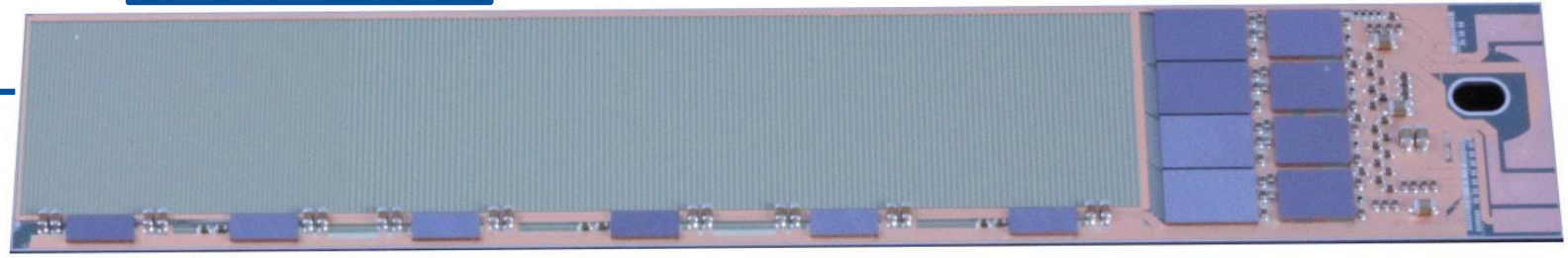
LMU POWER SUPPLY

- Supplies 23 different voltages to the module
  - ASIC power: 9 voltages
  - DEPFET Matrix: 14 voltages

	min.	Set Current	max.	min.	Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
sw-sub	0 mA	50 mA	50 mA	-7100 mV	-7000 mV	0 mV		-7067 mV	-7002 mV	-9 mA	sw-sub
sw-dvdd	0 mA	30 mA	30 mA	0 mV	1800 mV	2000 mV		2963 mV	1801 mV	19 mA	sw-dvdd
sw-refin	0 mA	30 mA	30 mA	-7100 mV	-5200 mV	0 mV		-5241 mV	-5202 mV	0 mA	sw-refin
dcd-amplow	0 mA	1300 mA	1400 mA	0 mV	250 mV	500 mV		993 mV	249 mV	-686 mA	dcd-amplow
dcd-avdd	0 mA	3000 mA	3000 mA	0 mV	1800 mV	2000 mV		5098 mV	1801 mV	2728 mA	dcd-avdd
dcd-dvdd	0 mA	940 mA	1000 mA	0 mV	1800 mV	2000 mV		3587 mV	1800 mV	834 mA	dcd-dvdd
dcd-refin	0 mA	1000 mA	1000 mA	0 mV	700 mV	1300 mV		2440 mV	700 mV	203 mA	dcd-refin
dhp-core	0 mA	730 mA	800 mA	0 mV	1200 mV	1640 mV		2968 mV	1199 mV	663 mA	dhp-core
dhp-io	0 mA	550 mA	550 mA	0 mV	1800 mV	2000 mV		3338 mV	1800 mV	276 mA	dhp-io

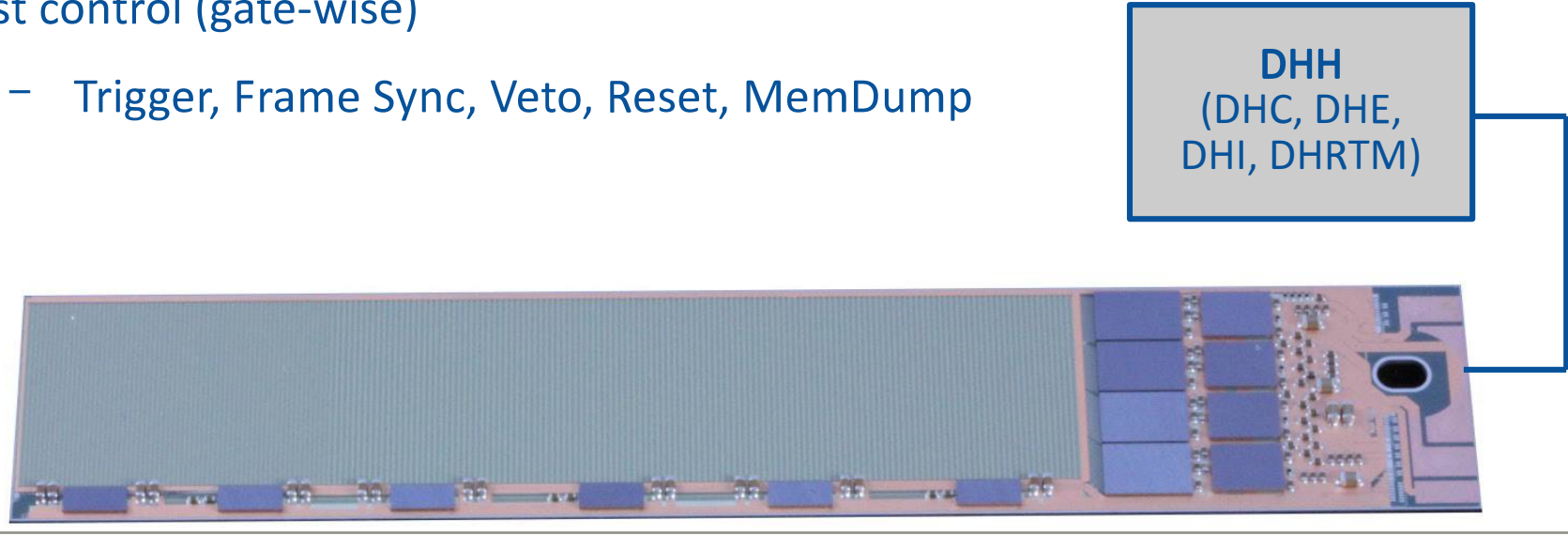
bulk	0 mA	10 mA	10 mA	0 mV	10000 mV	10000 mV		9997 mV	10000 mV	0 mA	bulk
clear-on	0 mA	40 mA	70 mA	0 mV	19000 mV	22000 mV		19096 mV	19004 mV	27 mA	clear-on
clear-off	0 mA	30 mA	40 mA	0 mV	3000 mV	20000 mV		2856 mV	3010 mV	-21 mA	clear-off
gate-on1	0 mA	15 mA	30 mA	-4000 mV	-2000 mV	5000 mV		-2077 mV	-1997 mV	-7 mA	gate-on1
gate-on2	0 mA	15 mA	30 mA	-4000 mV	-2000 mV	5000 mV		-2072 mV	-2008 mV	-6 mA	gate-on2
gate-on3	0 mA	15 mA	30 mA	-4000 mV	-2000 mV	5000 mV		-2079 mV	-1996 mV	-6 mA	gate-on3
gate-off	0 mA	30 mA	30 mA	0 mV	5000 mV	6000 mV		5102 mV	4996 mV	26 mA	gate-off
source	0 mA	120 mA	150 mA	0 mV	6000 mV	7000 mV		7425 mV	5999 mV	69 mA	source
ccg1	0 mA	10 mA	10 mA	-5000 mV	0 mV	0 mV		-2 mV	2 mV	0 mA	ccg1
ccg2	0 mA	10 mA	10 mA	-5000 mV	0 mV	0 mV		0 mV	5 mV	0 mA	ccg2
ccg3	0 mA	10 mA	10 mA	-5000 mV	0 mV	0 mV		-3 mV	-1 mV	0 mA	ccg3
hv	0 uA	1000 uA	10000 uA	-80000 mV	-58000 mV	0 mV		-57913 mV	-58027 mV	-5 uA	hv
drift	0 mA	10 mA	10 mA	-7000 mV	-7000 mV	0 mV		-7010 mV	-7011 mV	0 mA	drift
polycover	0 mA	0 mA	10 mA	0 mV	0 mV	0 mV		10 mV	12 mV	0 mA	polycover
guard	0 mA	10 mA	30 mA	-6000 mV	-5000 mV	0 mV		-4999 mV	-5004 mV	0 mA	guard

LMU **PS**



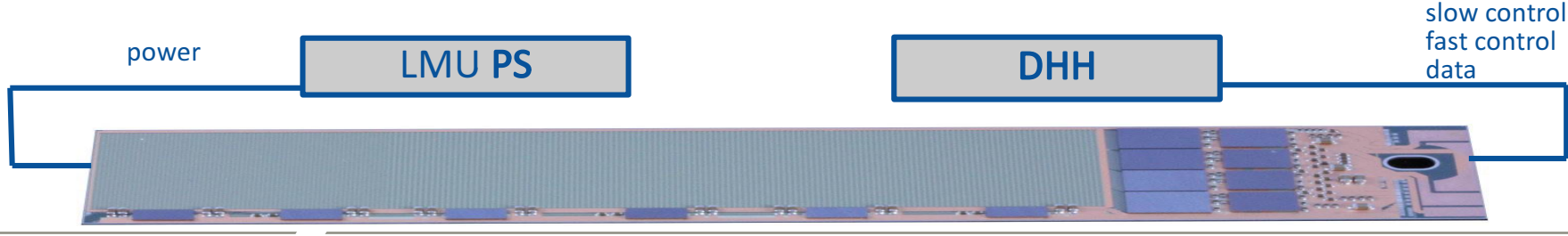
DATA HANDLING HUB (DHH)

- Data readout DHE → DHC → PC
- Slow control (DHI): JTAG communication with ASICs
- Fast control (gate-wise)
  - Trigger, Frame Sync, Veto, Reset, MemDump



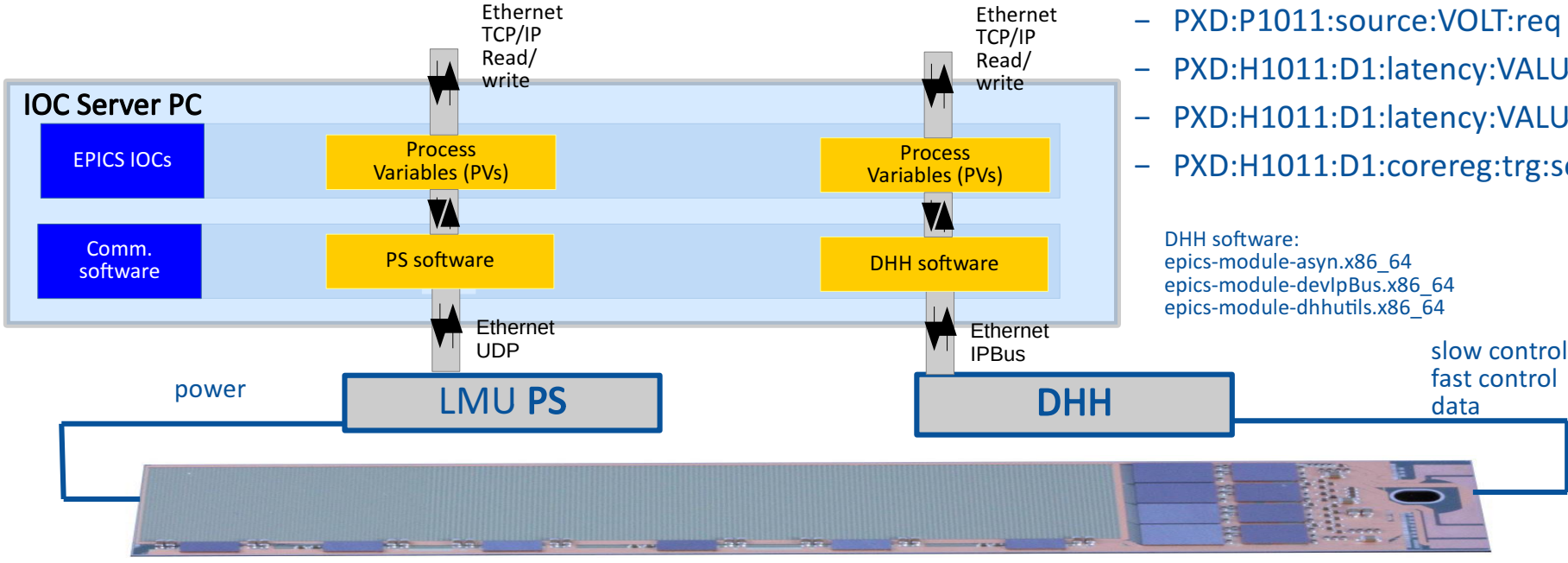
EPICS
HARDWARE REPRESENTATION IN SOFTWARE

- All ASIC/FPGA registers represented as EPICS Process Variables (PVs):



EPICS
HARDWARE REPRESENTATION IN SOFTWARE

- All ASIC/FPGA registers represented as EPICS Process Variables (PVs):
  - PXD:H1011:trg_len:VALUES:set
  - PXD:P1011:source:VOLT:req
  - PXD:H1011:D1:latency:VALUE:set
  - PXD:H1011:D1:latency:VALUE:cur
  - PXD:H1011:D1:corereg:trg:set

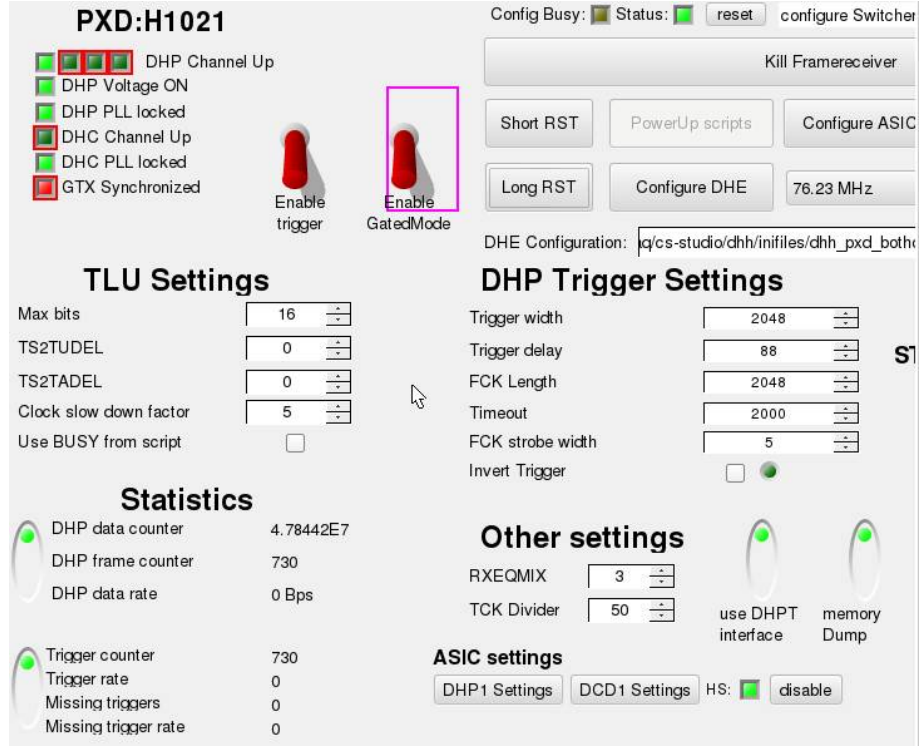


DHH software:
epics-module-asyn.x86_64
epics-module-devIpBus.x86_64
epics-module-dhhutils.x86_64

USING EPICS PVS

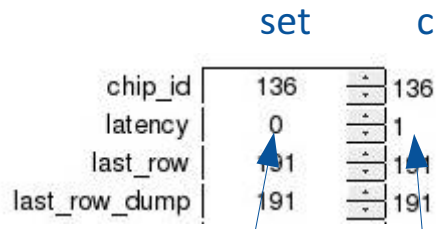
- CS-Studio
- Python scripts

```
from epics_utils import get_pv

# enable triggering
trigger_enable = get_pv("PXD:H1021:trg_en:VALUE:set")
trigger_enable.put(1)

# check link status
link_status_pv = get_pv("PXD:H1021:dhp1_channel_up:S:cur")
link_ok = link_status_pv.get()

if not link_ok:
      print("DHP link 1 is down")

# set DHP CML bias value
# and write to DHP JTAG register
get_pv(DHP, "idac_tx_bias:VALUE:set").put(130)
get_pv(DHP, "globalreg:trg:set").put(1)
```



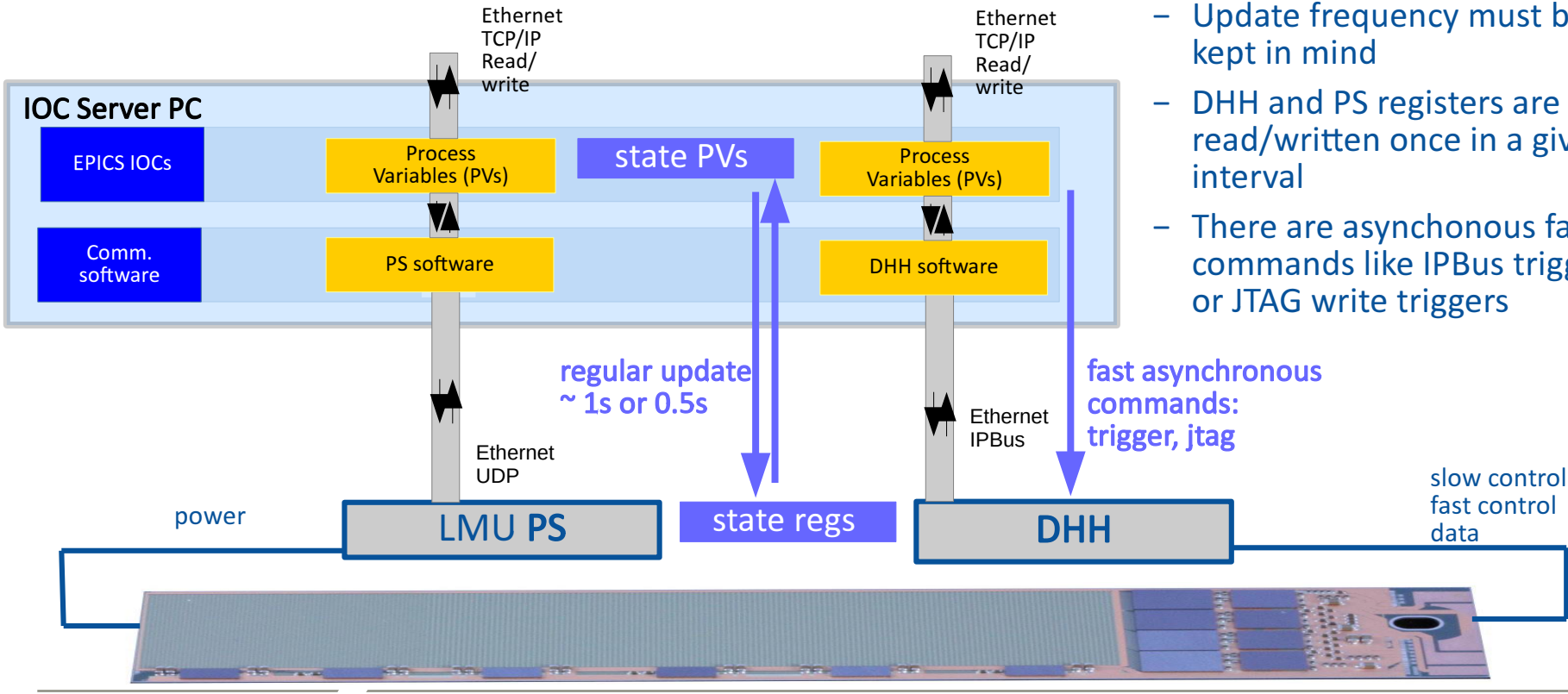
COMMUNICATION WITH ASICS

- ASIC register:
  - „set“ and „cur“ values
  - Values are written to ASIC registers only when JTAG dispatch is triggered



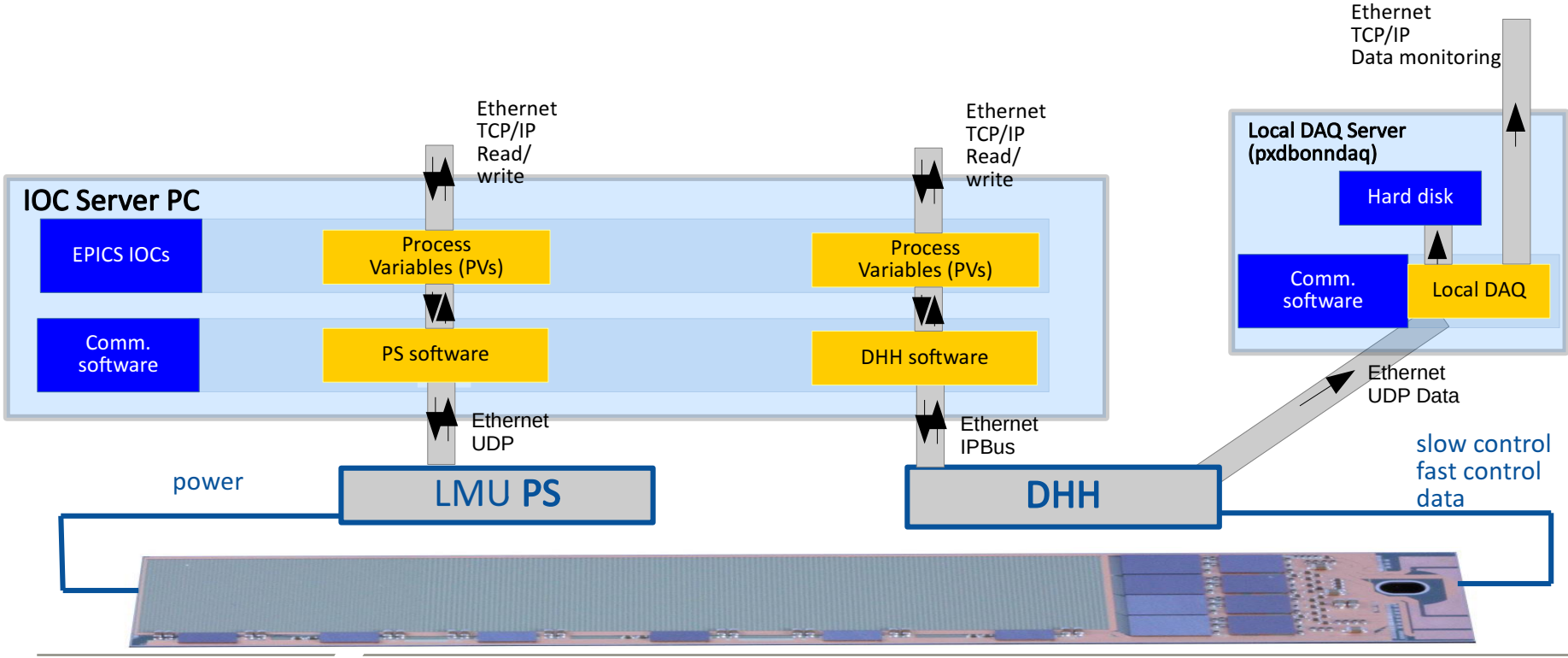
caput PXD:H1011:D1:latency:VALUE:set 5	write set PV
caget PXD:H1011:D1:latency:VALUE:cur	read current value (cur PV)
1	result: 1
caput PXD:H1011:D1:corereg:trg:set 1	trigger DHP core JTAG register write
caget PXD:H1011:D1:latency:VALUE:cur	read current value (cur PV)
5	result: 5

COMMUNICATION



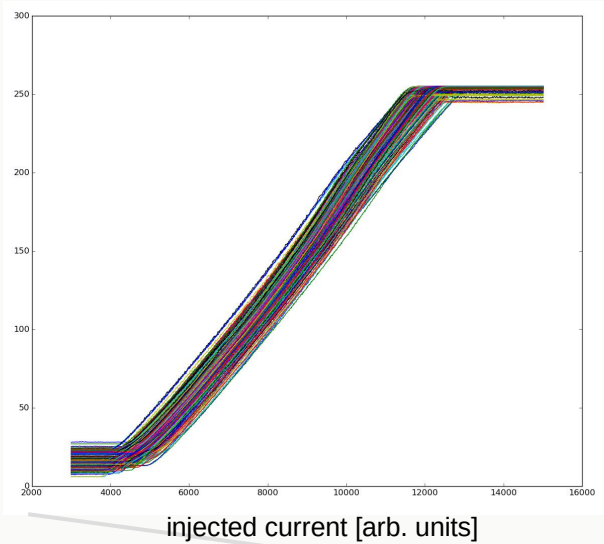
- Update frequency must be kept in mind
- DHH and PS registers are read/written once in a given interval
- There are asynchonous fast commands like IPBus trigger or JTAG write triggers

LOCAL DATA READOUT

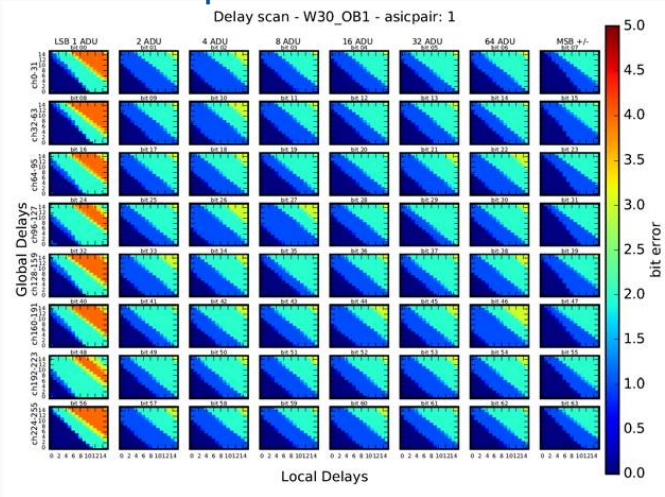


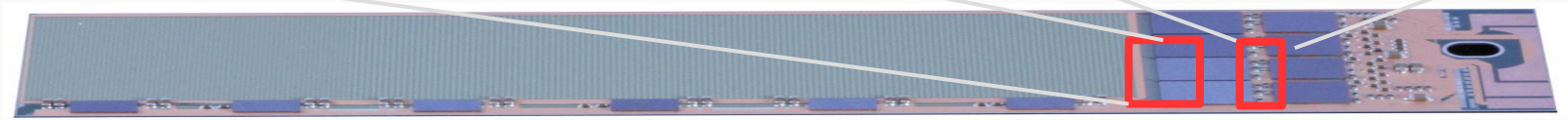
CHARACTERIZATION ROUTINES

256 analog channels per DCD
Transfer curves and parameter optimization



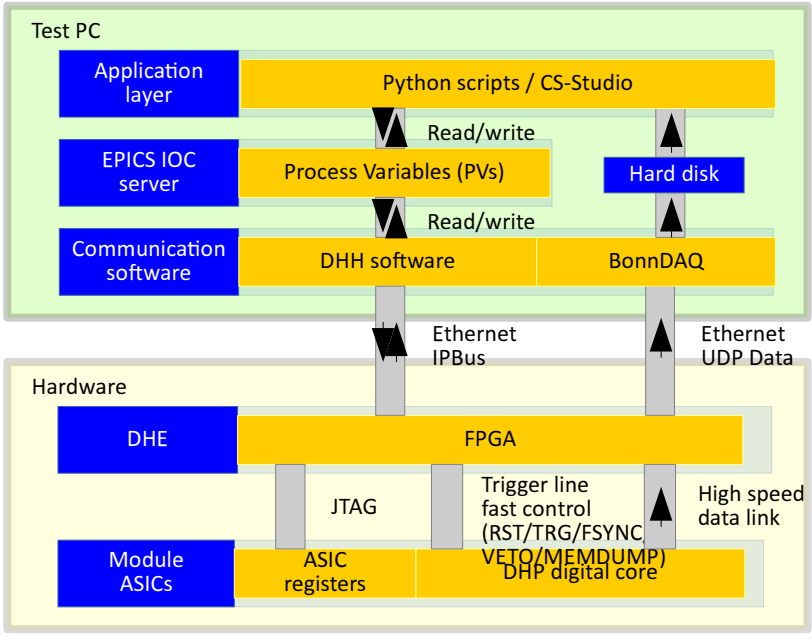
Timing of ASIC communication
Delay elements optimization with bit error tests



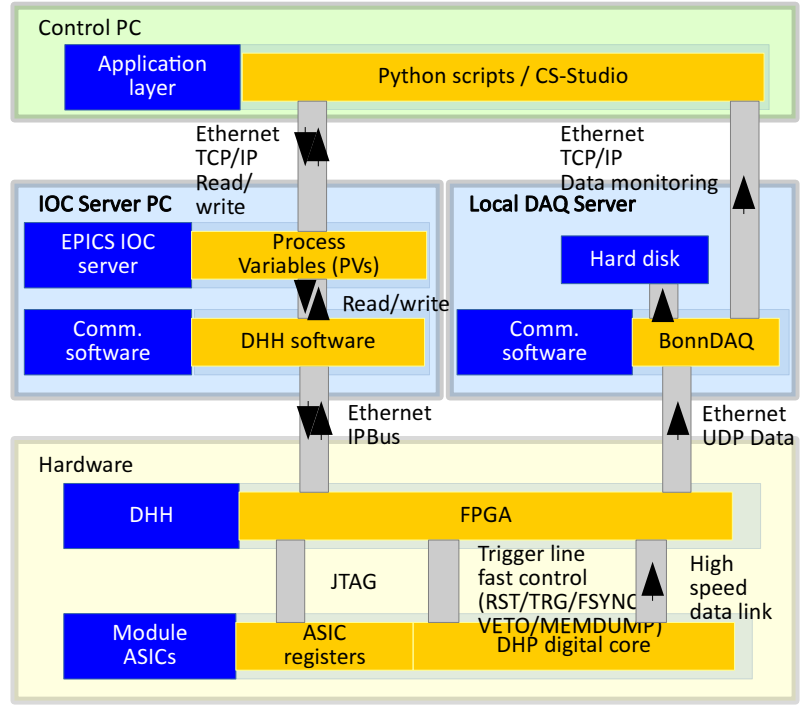


LAB VS FINAL SYSTEM

Laboratory



Belle II Experiment



→ The system used for laboratory testing already implements (almost) all the elements for the final Belle II experiment.

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LAB VS FINAL SYSTEM

- Laboratory DHH setup is much more simple
- Final DHH requires different triggering mechanism and different output format because of the DHC

- For final system, many „run control“ systems are available/being develop[illegible] bration IOC, utility IOC (temperature measurement) online monitor etc.

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Thanks