DHP Test Chip Design Status

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Functionalities

- Record 4x1024 rows of raw data (4 frames) . plus 1x pedestal?
- Trigger ID – 8bit (may be obsolete), Frame ID - 8bit
- Latency for up to 1024 rows before trigger
- Configuration through JTAG protocol standard (IEEE)
- Boundary scan test included through JTAG
- Temperature measurement
- Single bit error protected memories + triple redundant registers
- High speed CML output using Aurora protocol
- 5 operating modes
  - DO NOTHING
  - TEST
  - STORE DATA TO MEM
  - NORMAL AQUISITION (data, pedestals, subtration, clustering)
  - SEND MEM

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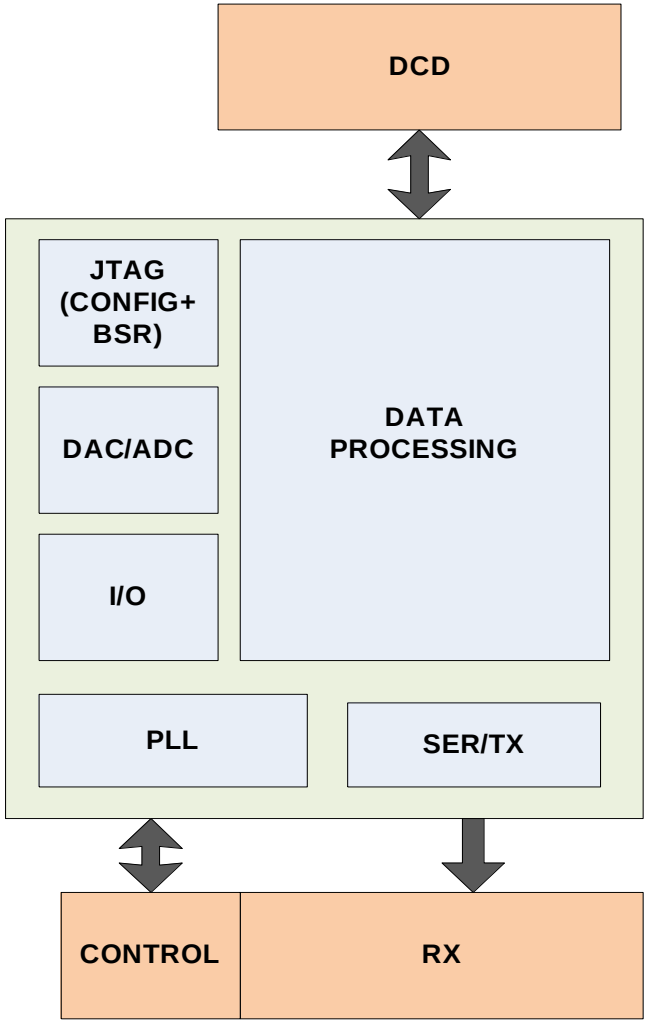
DHP Concept



- Main clock 100MHz (from erxtern, DHH)
- DCD clock 400MHz
- Output clock 0.4-1GHz

Status/Plans

- people

  Tomasz Hemperek (full time: memories, SER-Tx, processing)

  (Hans Krüger)

  Andre Kruth (I/O blocks and … perhaps PLL)

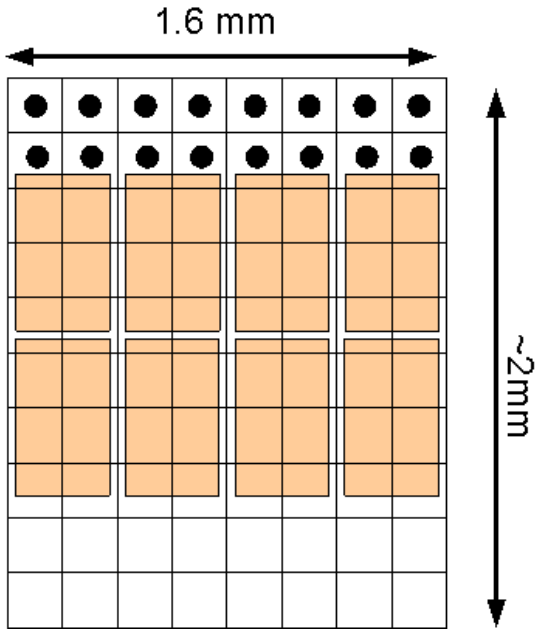
  Barcelona friends … next talk (DAC/ADC, biasing circuit)

- Testchip for the main blocks planned

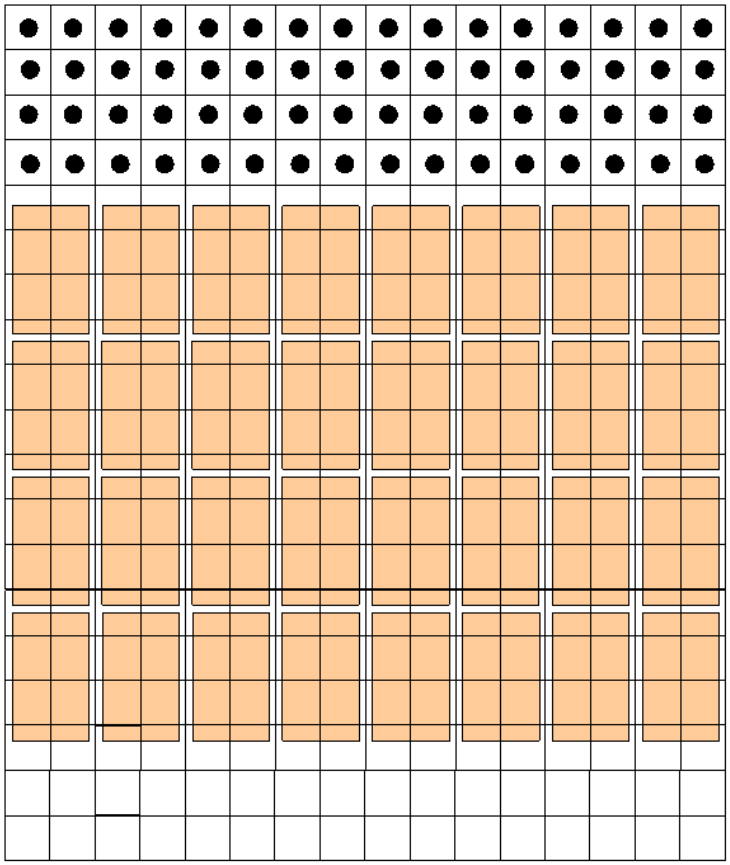
  - 90 nm IBM technology / 9 metals
  - submission date: 26/10/2009 (next one is 22/02/2010)
  - ~30 k$

Floor Plan

- Test Chip
  - ¼ of the memory
  - ¼ of I/Os
  - wire bonding ok



- Final chip ? wire bonding?



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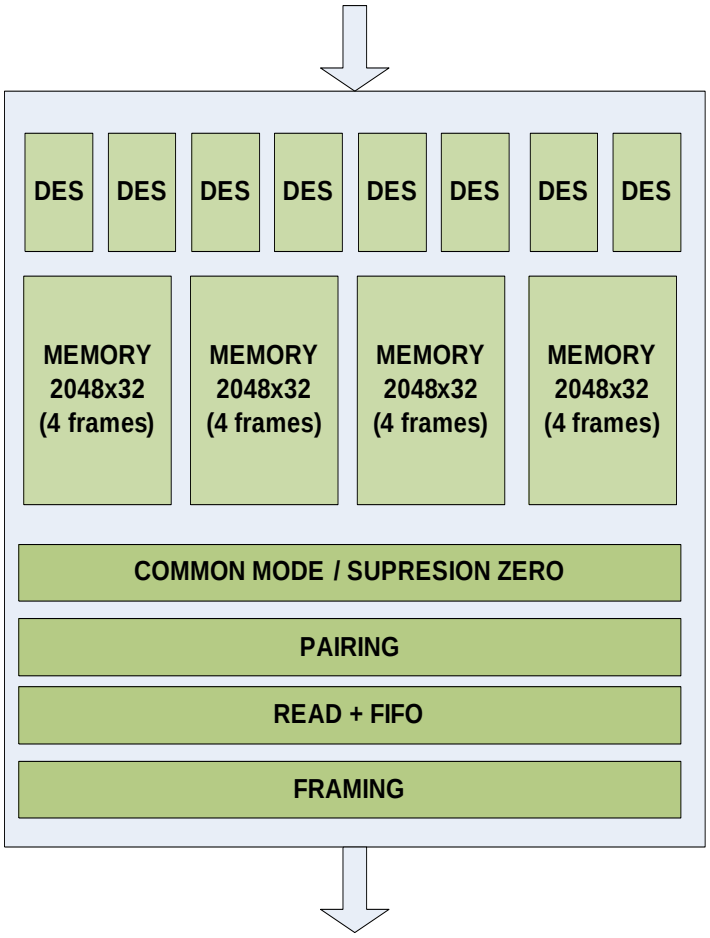
Processing



- 2 deserializers/inputs share one memory
- buffering for max. 1 frame
- pedestal correction
- common mode correction
- hit pairing
- readout
- output framing

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Summary

… with some luck we have a sizeable
testchip at the beginning of 2010
from which we can plan the full chip (not a big step)
… most important: irradiation tests

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