- **Workpackage issues**
- **Simulation studies in Valencia**

C. Lacasta, C. Mariñas, M. Vos

IFIC-Valencia

Outline

- Thermal parameters

- Cooling options

Contributions: P. Fischer, I. Peric, Ch. Kreidl, H.G. Moser, H. Krüger, Ch. Kiesling, C. Lacasta

- Thermal/mechanical studies in Valencia

- Summary

Power consumptions

➢ DCD

• In the PXD of Belle II, we have 250 columns; but because of we read 4 rows simultaneously, then we will need 1000 readout channels (4 DCDs needed in final design asuming the new geometry with 256 channels per chip).

• The DIGITAL power consumption of this chips is 768µA/channel. So, for 1000 channels, the current is 0.768A.

• The ANALOG power consumption is 2mA/channel. So, for 1000 channels, the current is 2A.

• Because of the voltage is 1.8V, the total DCD power consumption per half ladder is **5Watts** (Digital=1.4W, Analog=3.6W)

• For the PXD6 production, only 3 DCDs with 256 inputs are proposed; so he p.c. is **3.82W**.

➢ **SWITCHERs**

• Each Switcher uses **0.09W** (Digital=40mW, Analog=50mW)

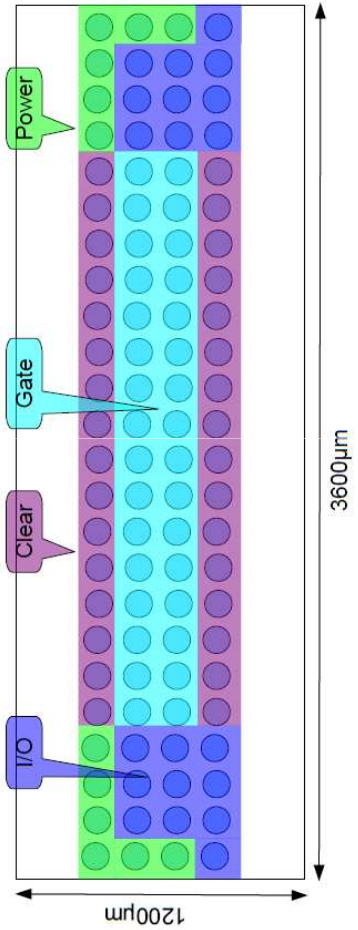
➢ **DHP**

• Still we have no reliable numbers for the DHP. Nevertheless, we will asume a power consumption of **2W** per half ladder for our simulations.

➢ **SENSOR**

• Assuming a drain current of 100µA and a Source-Drain voltage of 5V, we have 0.5mW per active pixel. There are 1000 pixels (250pixels x 4 rows) active in each module half → **0.5W**/half module

Switcher structure

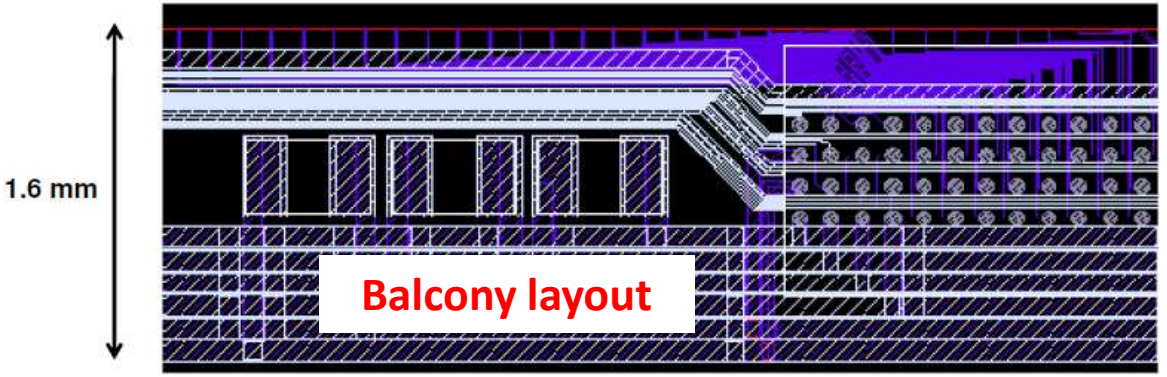


- Dimensions: 1.2x3.6 mm^2.

-Bumps: 32 for Gate, 32 for Clear, 32 for control (16 on the top and 16 on the bottom)

- Bump pitch array is 150x150µm^2.

- 1000 lines/(4 lines each time · 32 contacts)= 8 Switchers/ladder



Switcher bumps

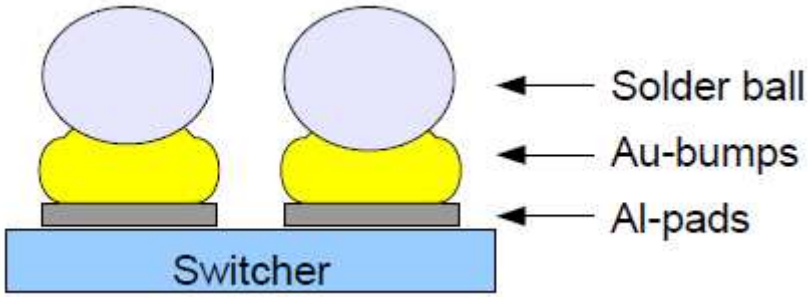
- Sizes and number of bumps are final for the Switcher.

- We will use a gold bump with a solder ball on top of it.

- The gold sphere (99.99% gold), which will be bumped to the Switcher and flattened, has a diameter ~35µm. They have a diameter of 60µm after coining.

- The Al-pads are round, and the diameter is 70µm

- The solder ball has diameter of ~100µm. It is an alloy: Sn-3Ag-0.5Cu. Solder Ball Type is Hitachi Metals SAC305.



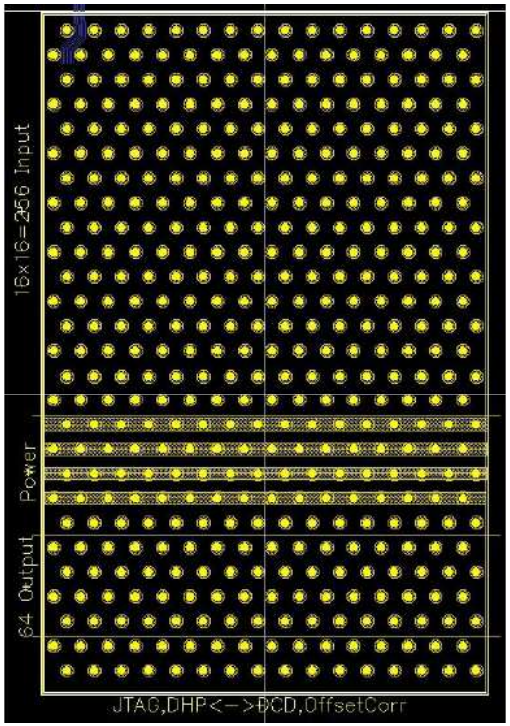
$$K_{Gold} = 317 \frac{W}{m \cdot K}$$

$$K_{Sn\text{-}3Ag\text{-}0.5Cu} = 57 \frac{W}{m \cdot K}$$

- Coined gold studs as underbump metallization

→ **Underfilling** material is not decided yet. Its thermal conductivity varies from 0.5 to 1.8 W/mK.

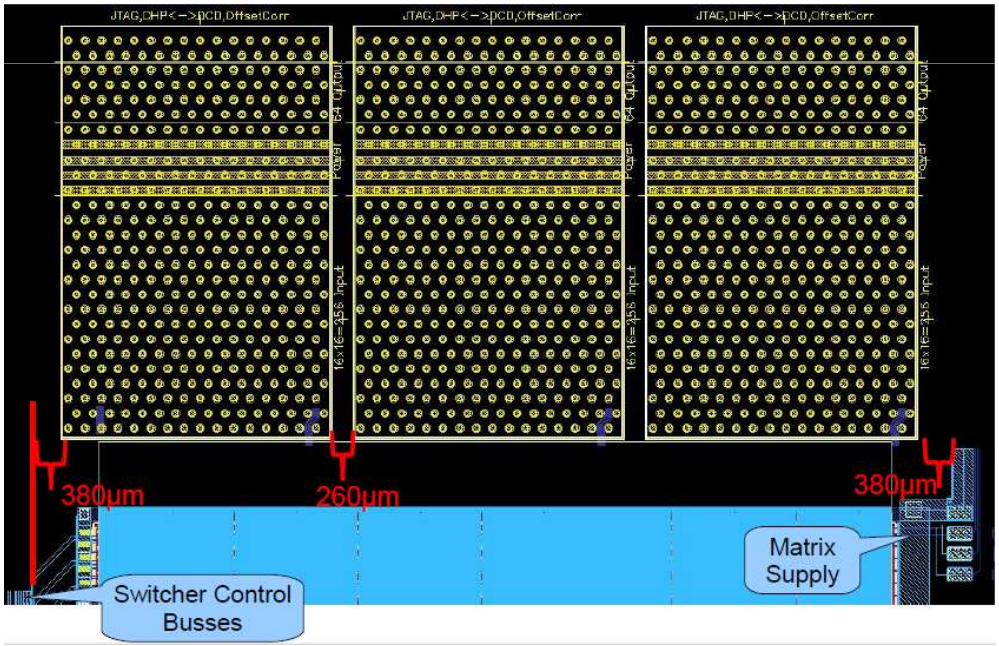
DCD Structure (proposal)



- Dimensions: 3280x5000 µm^2 + 130µm to both dimensions due to the fact that the die is not cut exactly to the designed size.

- Bumps: 432 bumps (256 inputs+80 power+64 output+32 JTAG)

- Bump pitch array is 200µm in X direction and 180µm in Y.



- 3 DCD used in PXD6 production
- 4 DCD in final production

proposed DCD at PXD6 Array

DCD bumps

- Sizes and number of bumps are not fixed yet for the DCDs.

- We also don't know how large the balls will be, nor which material.

- Several different options opened: Sn63/Pb37, Sn5/Pb95, and Sn/Ag/Cu, Sn/Ag.

- A rough number for the ball diameter is between 80-120µm.

$$K_{Sn63/Pb37} = 50 \frac{W}{m \cdot K}$$

$$K_{Sn5/Pb95} = 35.2 \frac{W}{m \cdot K}$$

$$K_{Sn/Ag} = 33 \frac{W}{m \cdot K}$$

$$K_{Sn/Ag/Cu} = 57 \frac{W}{m \cdot K}$$

- Let's assume a conductivity of 45 W/mK for this bumps, as a mean value of all of these numbers.
- And a bump diameter of 100µm

DHP (proposal)

- Dimensions: 3280x5000 μm^2

- Bumps: 432 bumps. Some of them are dummy bumps.

- Bump pitch array is 200µm.

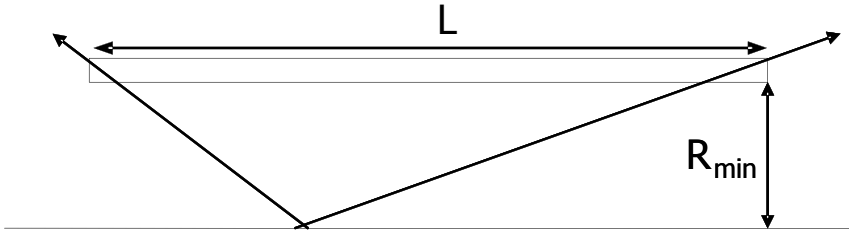
As a first approximation:

• The dimensions will be similar to the DCD. The combined width of the DHP chips will occupy the width of the active DEPFET pixel area: something between 11 and 13mm - neglecting the gaps between the chips.

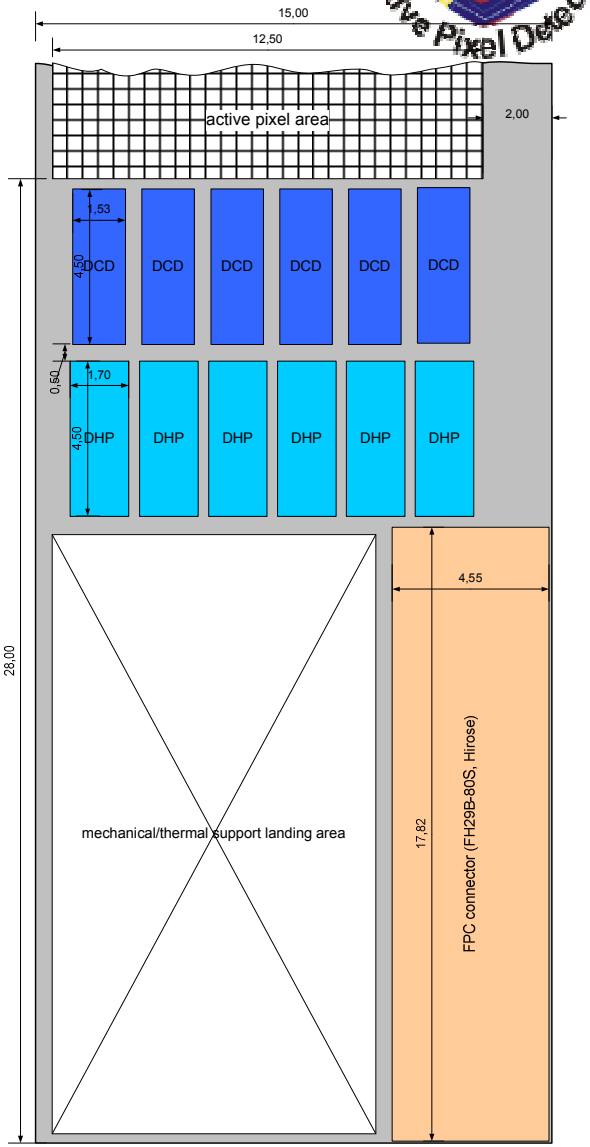
• The number of IOs will be less than the DCD but we will use dummy bump pads to have a regular bumping grid with 200µm pitch all over the chip

Ladder dimensions

- Monolithic inner layer
- Broken outer layer



	Layer 1	Layer 2
R_{min} (cm)	1.3	2.2
Sensitive Width (cm)	1.25	1.25
Balcony (cm)	0.2	0.2
Geometrical Width (cm)	1.5	1.5
Sensitive Length (cm)	7.5	11.7
Geometrical Length (cm)	8.06	12.26



- Sensitive $Length_{Inner}$=1000 lines · 75 microns=7.5cm
- Sensitive $Length_{Outer}$=1000 lines · 117microns=11.7cm
- Sensitive Width=250 columns · 50 microns=1.25cm

Setting limits

• The maximum temperatures allowed for the good performance of the detector in our simulations are:

T_{max} (Sensor)<30ºC

T_{max} (Chips)<60ºC

• We asume a total power dissipation of 9Watts distributed this way:

- ❖ 6W on the DCDs
- ❖ 0.5W on the sensor, uniformly distributed over the sensitive area
- ❖ 0.5W on the Switchers
- ❖ 2W on the DHP

$$K_{Diamond} = 2000 \frac{W}{m \cdot K}$$

$$K_{TPG} = 1600 \frac{W}{m \cdot K} \text{ and } 80 \frac{W}{m \cdot K}$$

Cooling options

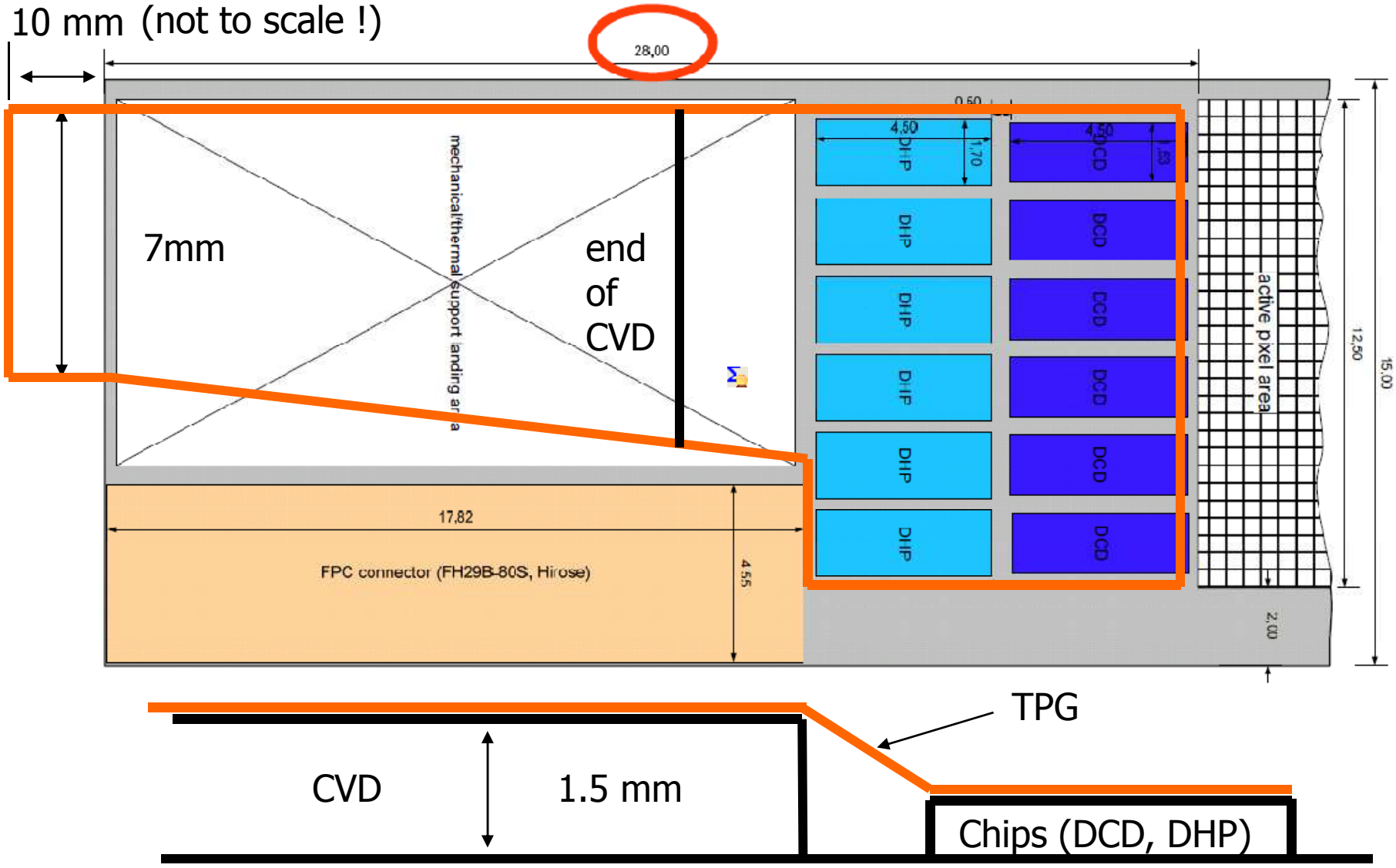
A couple of cooling options have arised:

- ‘Up’ cooling
  - TPG on the top of the chips and a diamond finger covering the free end’s area
  - Complicated design
  - TPG bridge ?
  - Sensor temperature ?

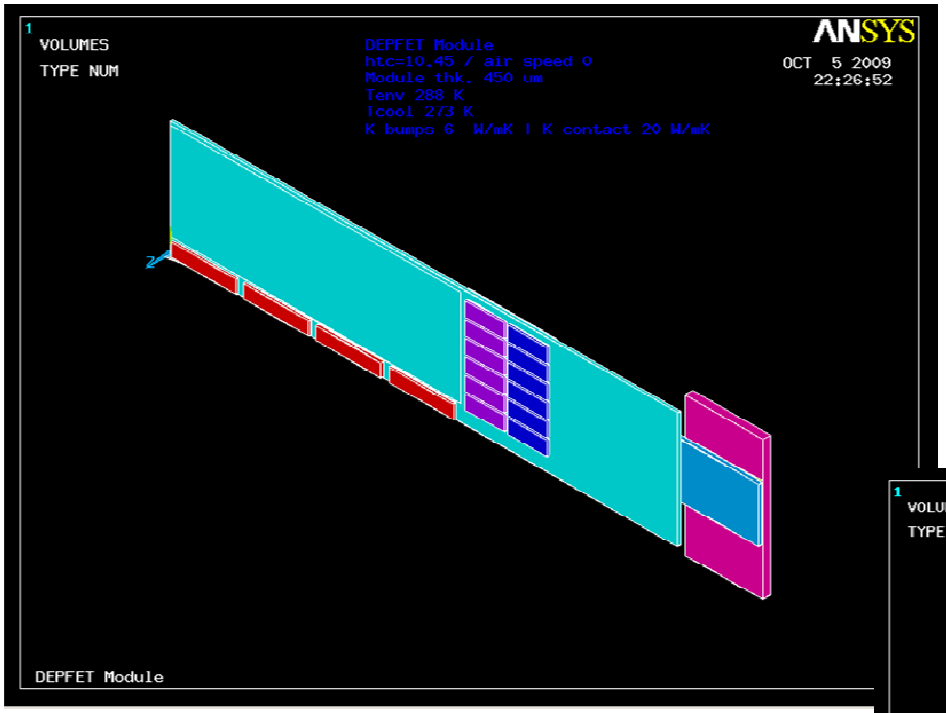
- ‘Down’ cooling
  - Diamond down the sensor, covering all the end’s lower area
  - Simply and clean design
  - Chips temperature (noise) ? → Noise ~ sqrt(kT). Increasing temperature from 0ºC to 80ºC gives only 14% more noise
  - Distance from IP (resolution) ?→ Physics impact in the detector placed 400 µm further away? What about background?

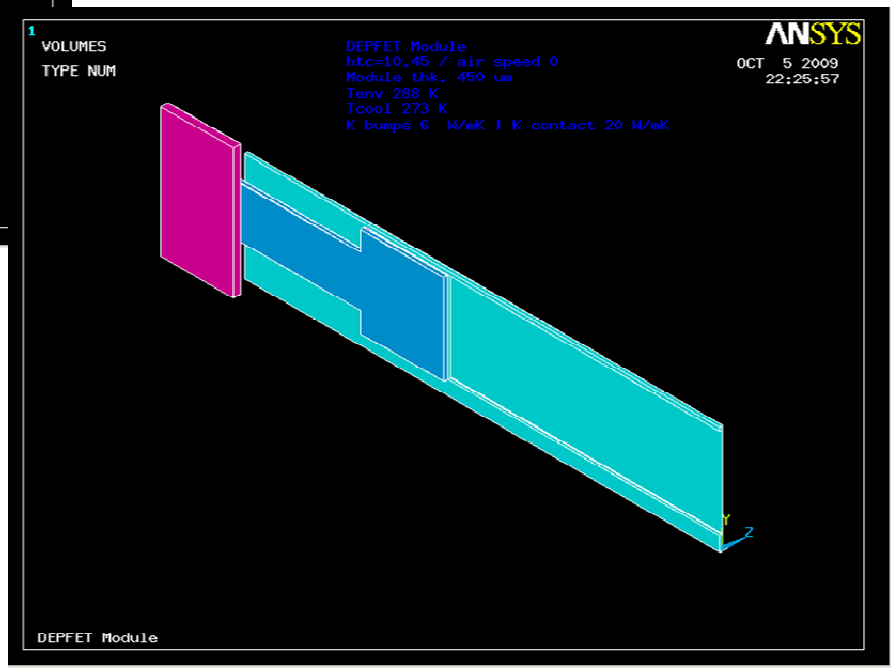
❖ We should choose the simpler working option

- 'Up' option


10 mm (not to scale !)
28,00
7mm
end of CVD
mechanical/thermal support landing area
active pixel area
DHP
DCD
4,50
1,70
1,53
0,50
12,50
15,00
2,00
17,82
FPC connector (FH29B-80S, Hirose)
4,55
TPG
CVD
1.5 mm
Chips (DCD, DHP)

- ‘Down’ option


1
VOLUMES
TYPE NUM
DEPFET Module
htc=10.45 / air speed 0
Module thk. 450 um
Tenv 288 K
Tcool 273 K
K bumps 6 W/mK I K contact 20 W/mK
ANSYS
OCT 5 2009
22:26:52
DEPFET Module


1
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ANSYS
OCT 5 2009
22:25:57
DEPFET Module

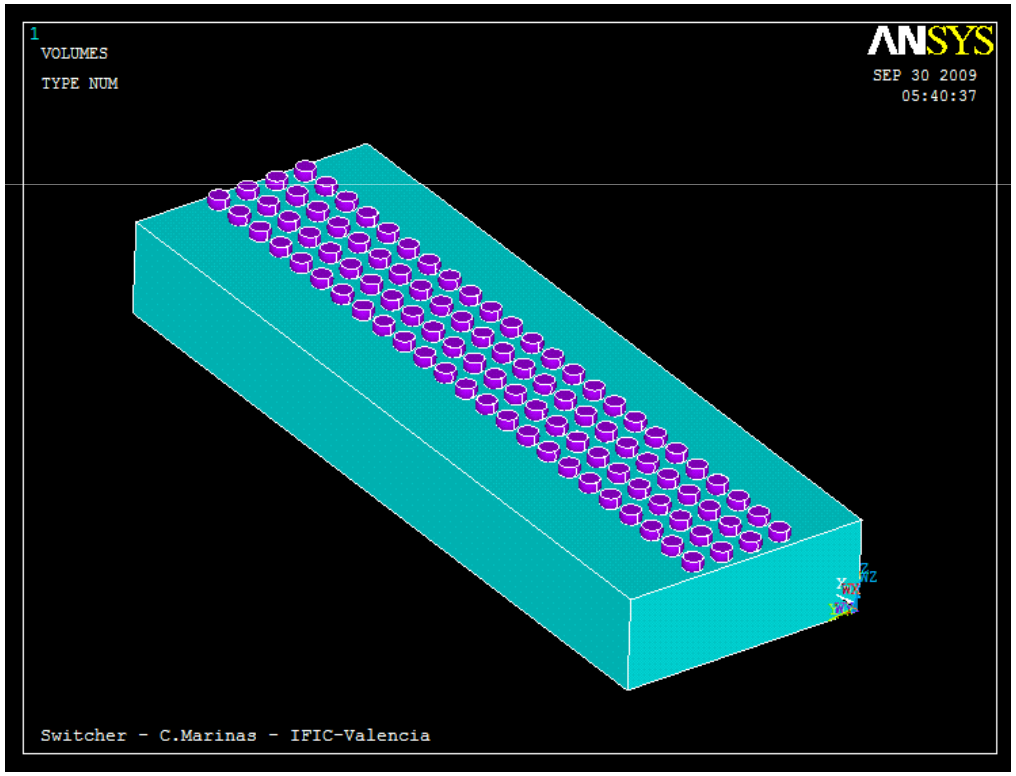
Studies needed

- Physics simulation
  - Background
  - Impact parameter resolution with distance to IP
- Thermal measurements and simulation
  - Heat conduction through the ball array
  - Chips/sensor temperature with the two cooling options
  - Cross-check with dummies
- Mechanical dummies
  - TPG bridge

Switcher in FE

Adressing the drawbacks…

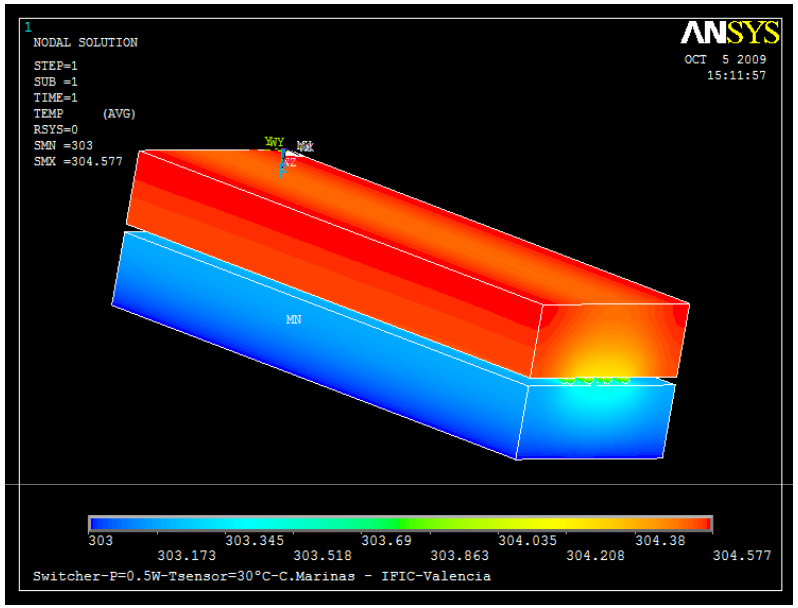
- Will the bumps be the bottleneck for the heat?
- What about the temperature of the chip?

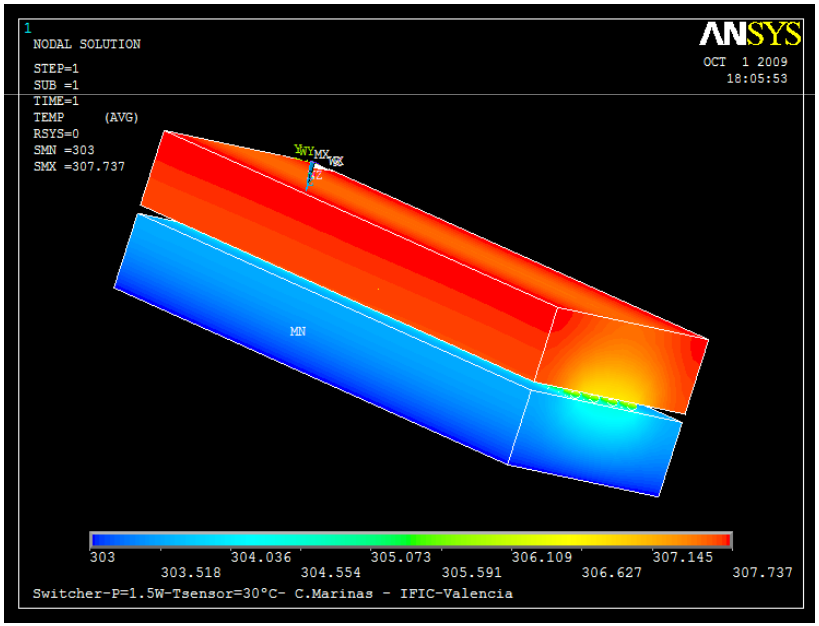


Switcher chip as defined in previous parameters

- 1.2x3.6 mm^2.
- 96 Bumps
- Bump pitch array 150x150μm^2.

Applying loads



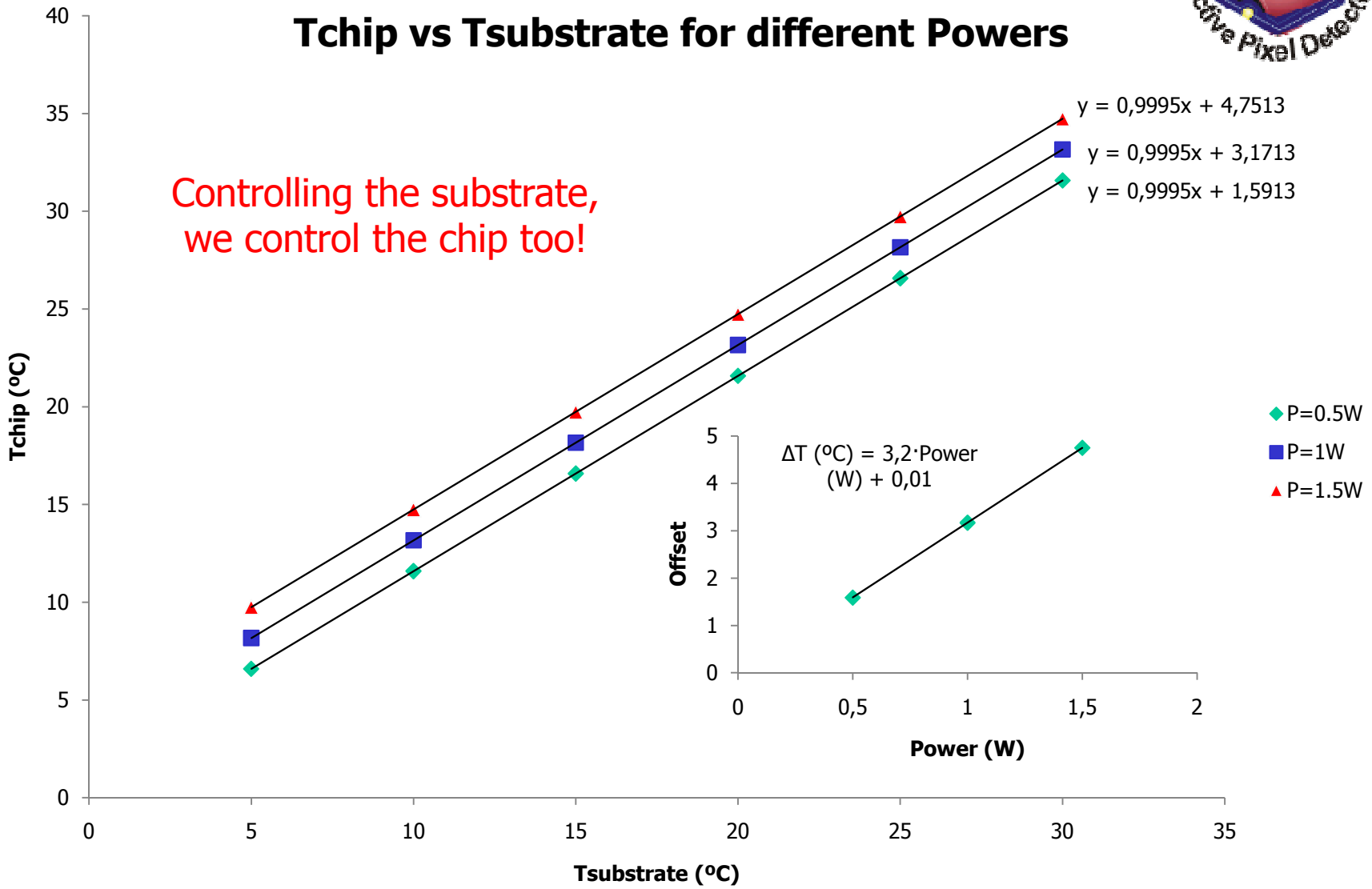


Apply loads:

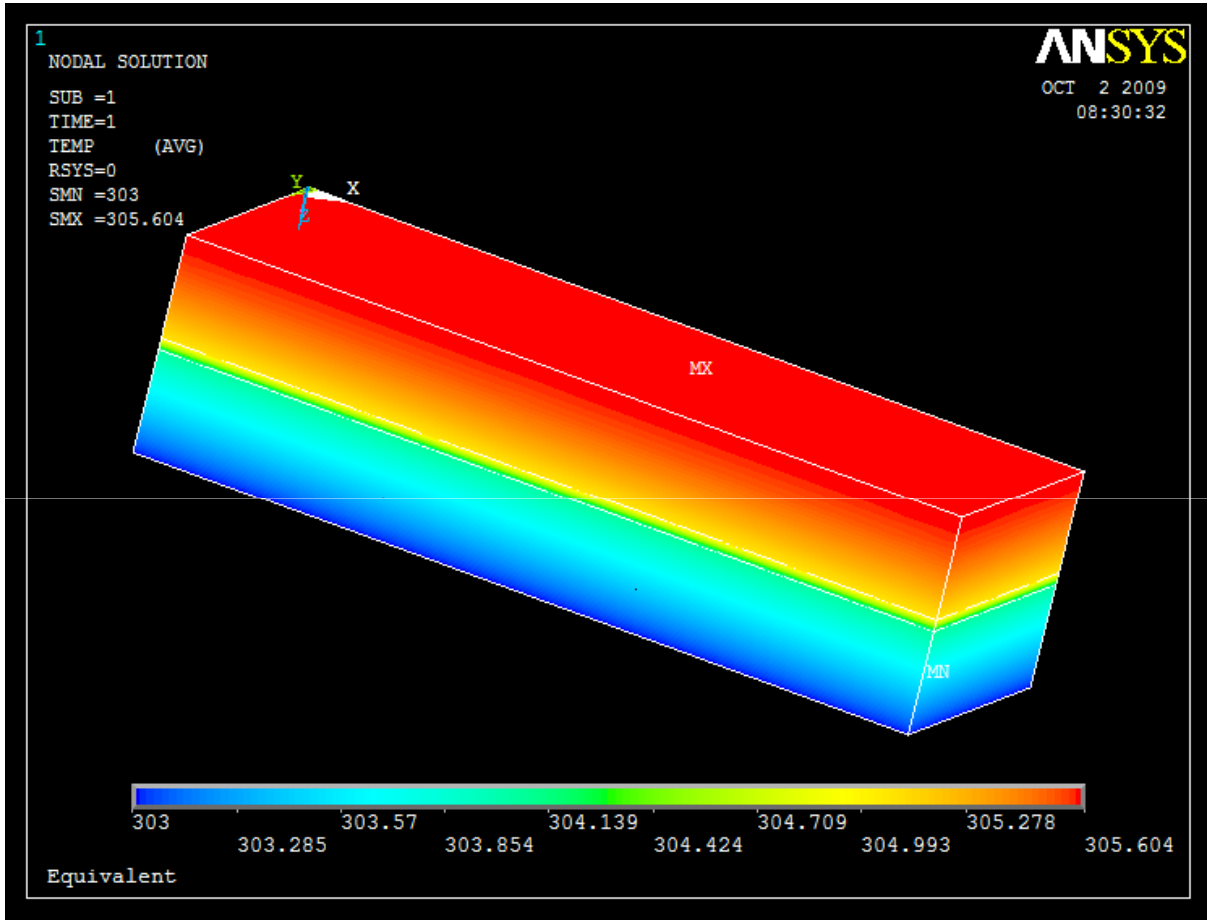
- Heat generation in the upper volume
- Cool the bottom of the sensitive block

→ See the temperature's evolution

Relation between T_{chip} and $T_{substrate}$



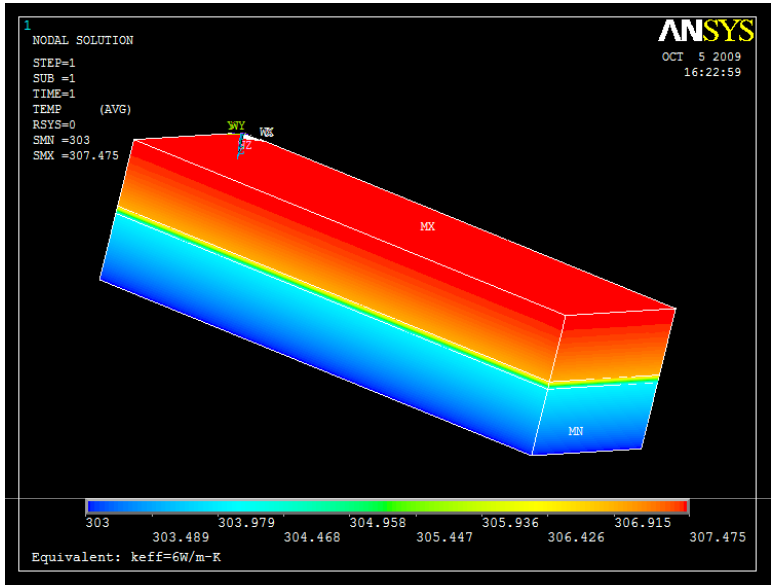
Equivalent model



Replace the array of bumps, by a block of thickness equal to the bump heigth, filling the total width and $\mathbf{k_{eff}}$

In order to implement the complete module keeping the computer time reasonable, lets look for an equivalent thermal coefficient of the bump matrix

‘Forced’ equivalent model



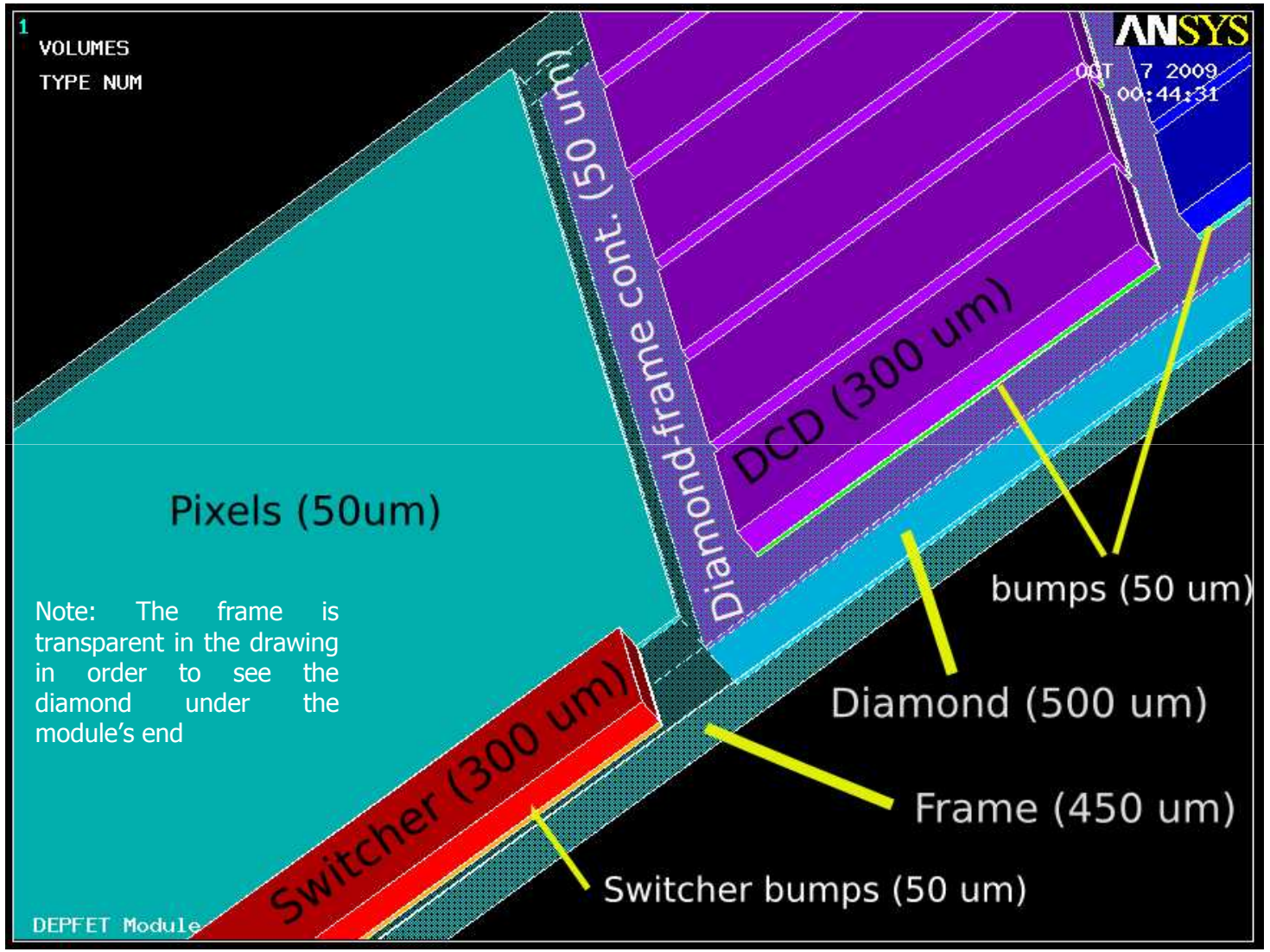
Let’s modify by hand the k_{eff} until reached the expected value…

→ k_{eff}=6W/m-K

Very good agreement ‘Full-Fast’ simulations

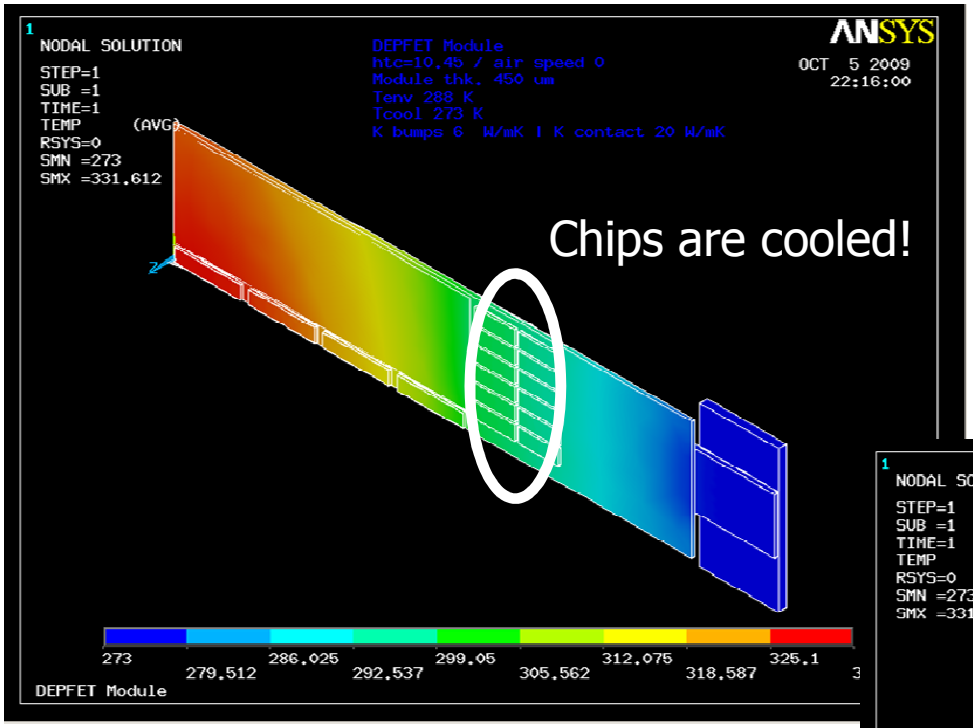
T substrate (K)	T chip (K); 0.5W; Full	T chip (K); 0.5W; Fast	T chip (K); 1W; Full	T chip (K); 1W; Fast	T chip (K); 1.5W; Full	T chip (K); 1.5W; Fast
278	279,59	279,5	281,17	281	282,75	282,5
283	284,59	284,5	286,17	286	287,75	287,5
288	289,58	289,5	291,16	291	292,74	292,5
293	294,58	294,5	296,16	296	297,74	297,5
298	299,58	299,5	301,16	301	302,74	302,5
303	304,58	304,5	306,16	306	307,74	307,47

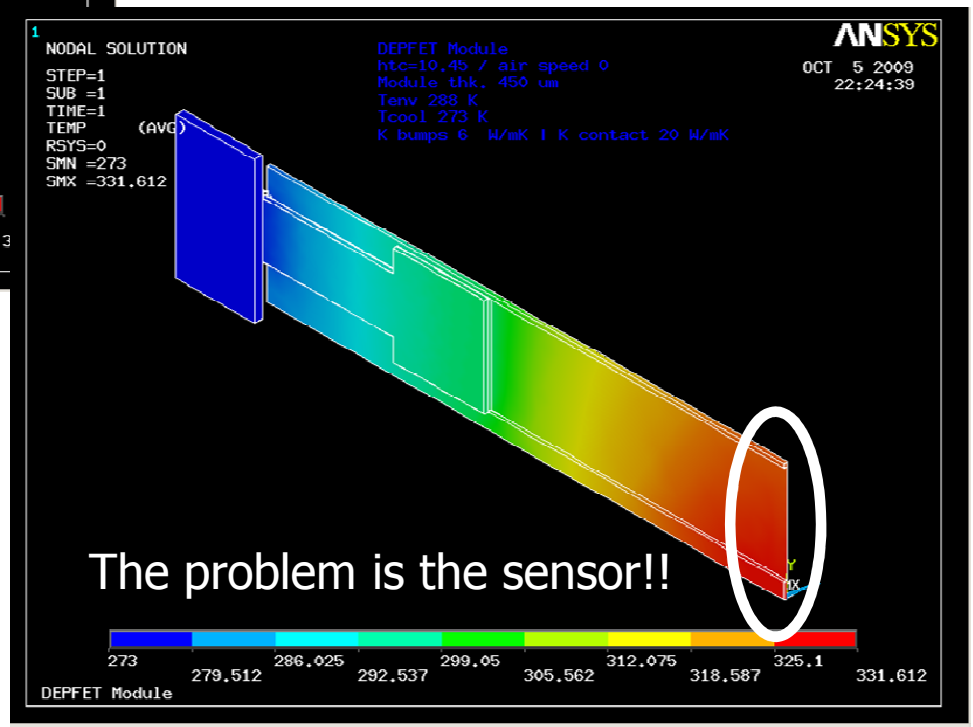
Full module geometry



Dimensions and arrangement according to the "Parameters list"

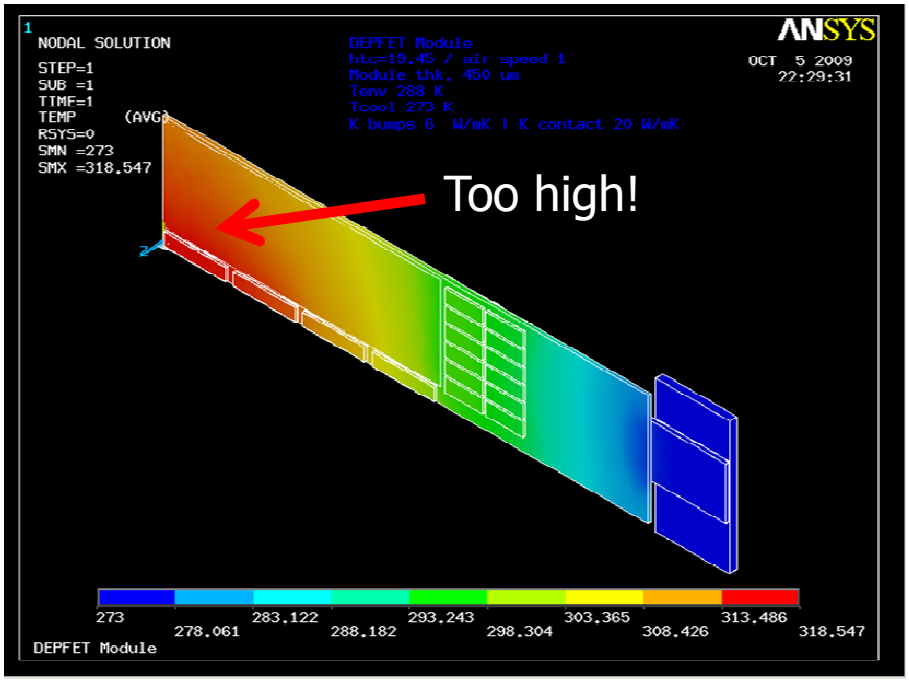
Full module



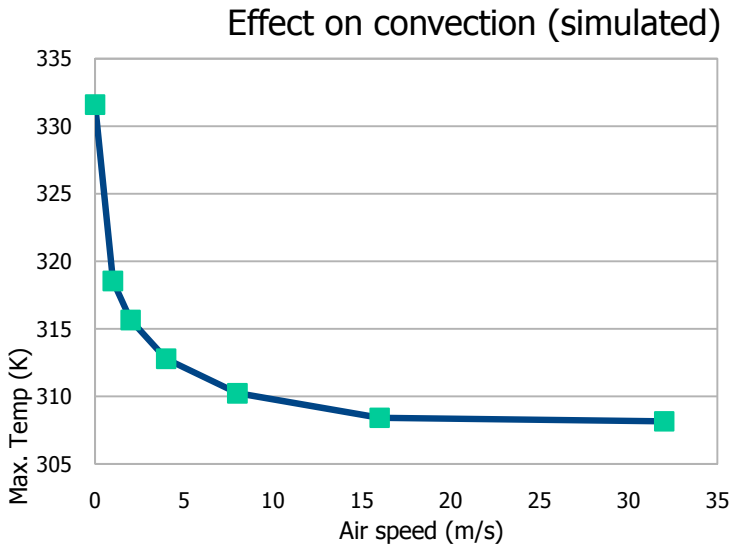


- $T_{CoolBlock}$=0ºC
- T_{sensor}=58ºC !! ← Too high!
- Free convection

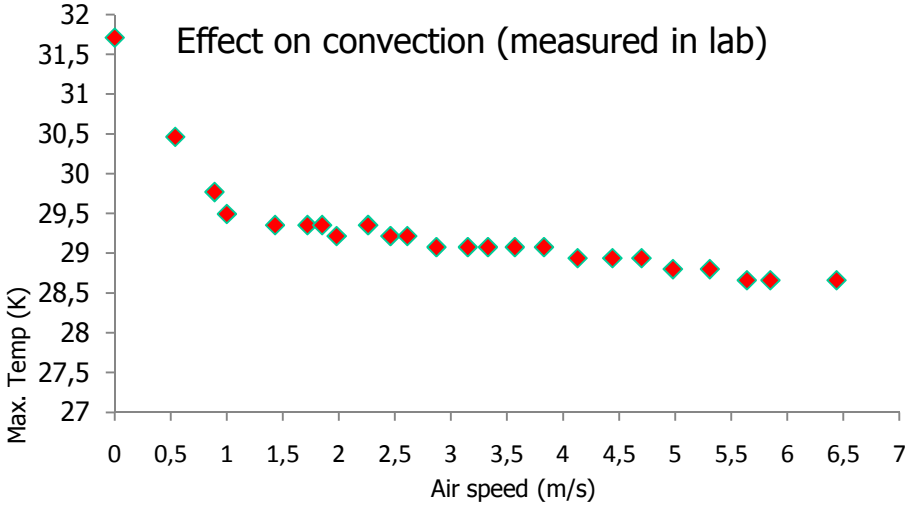
Introducing convection



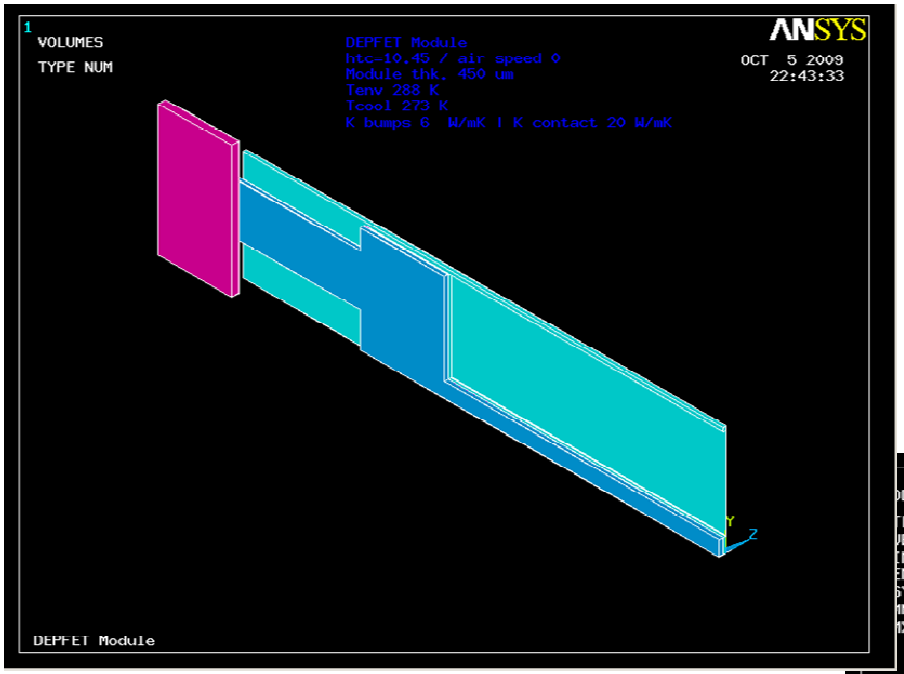
→ The problem is still there…

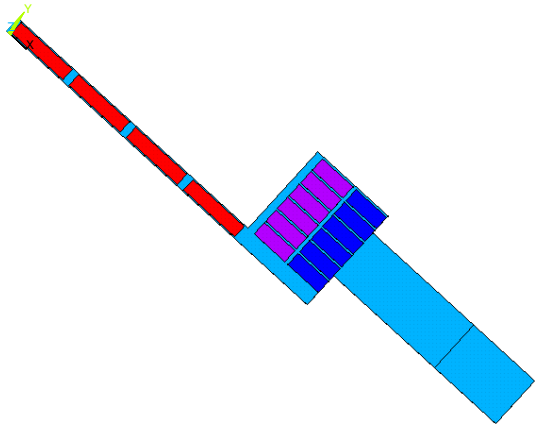


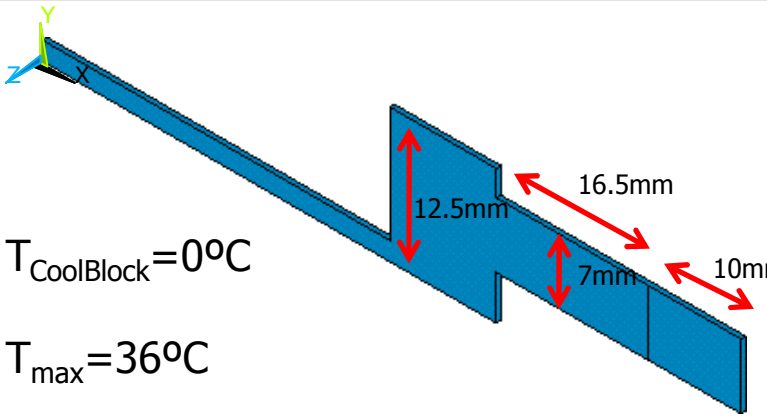
- $T_{CoolBlock}$=0ºC
- T_{max}=45ºC
- Air 1m/s, ambient T



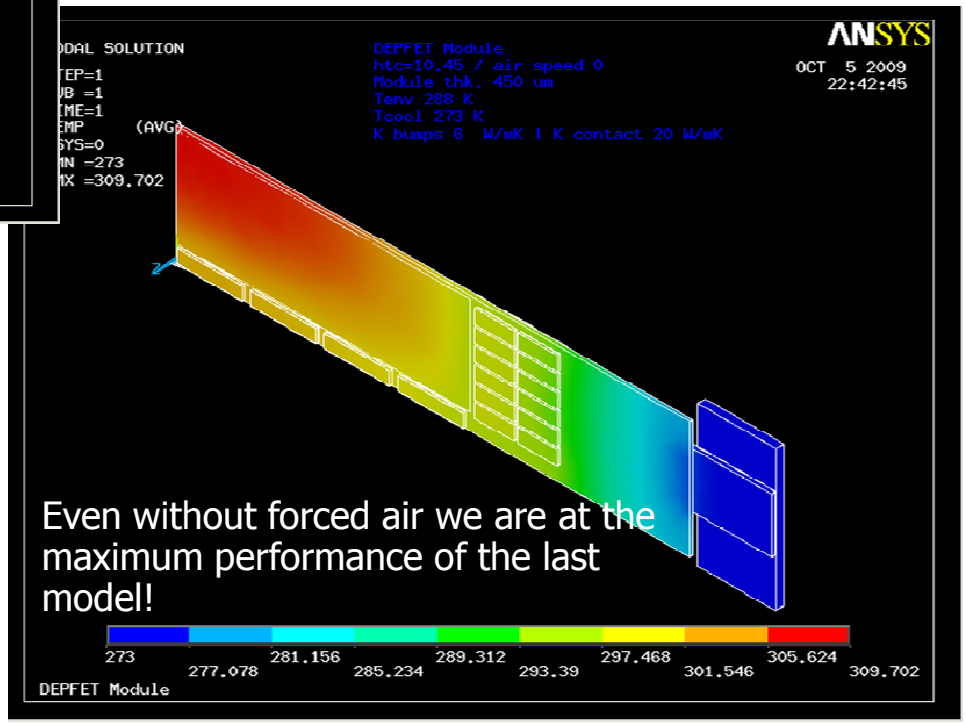
Extend diamond under the switchers





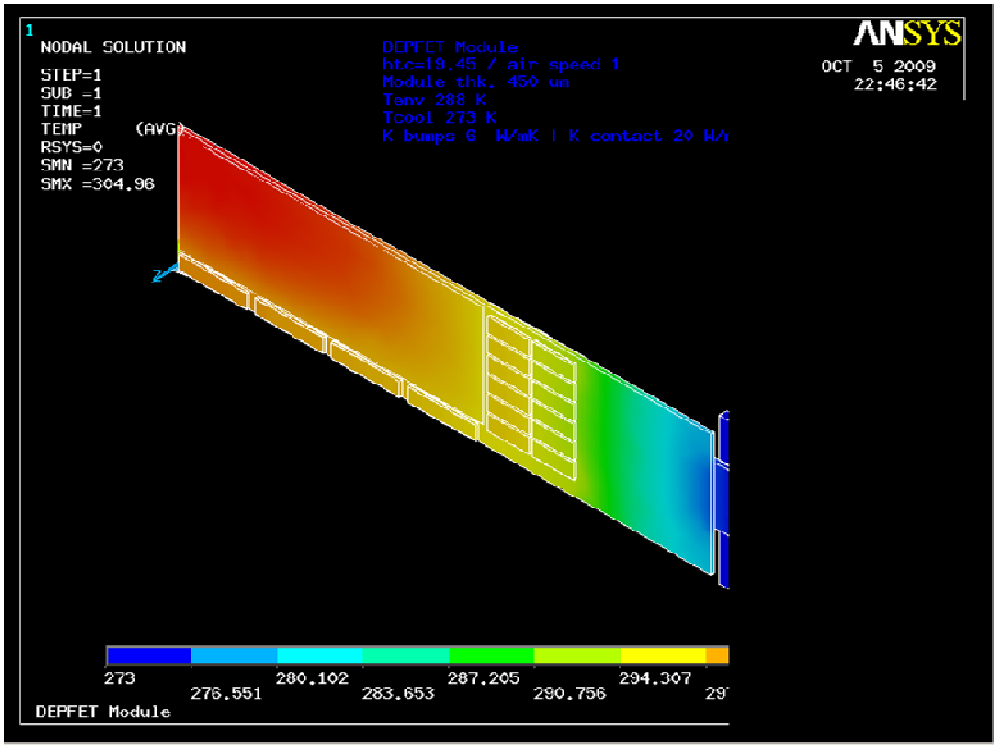


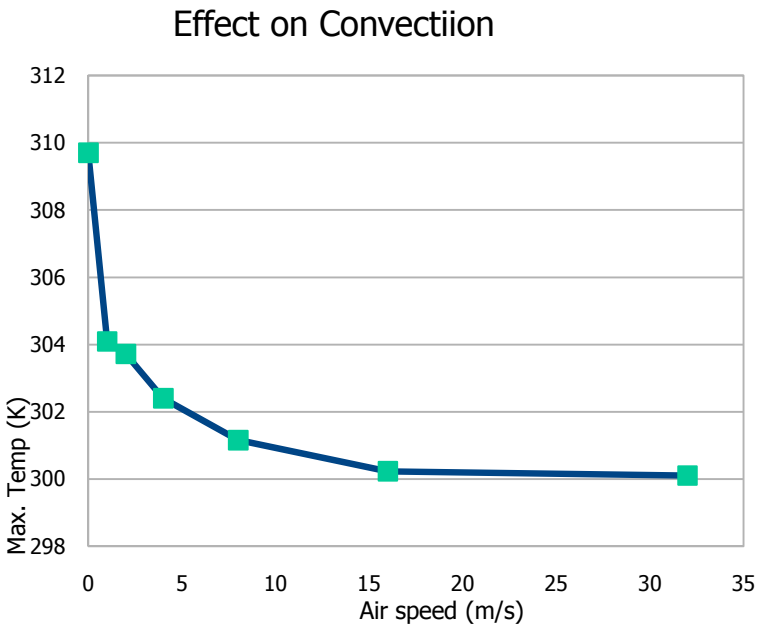
- $T_{CoolBlock}$=0ºC
- T_{max}=36ºC
- Free convection



Even without forced air we are at the maximum performance of the last model!

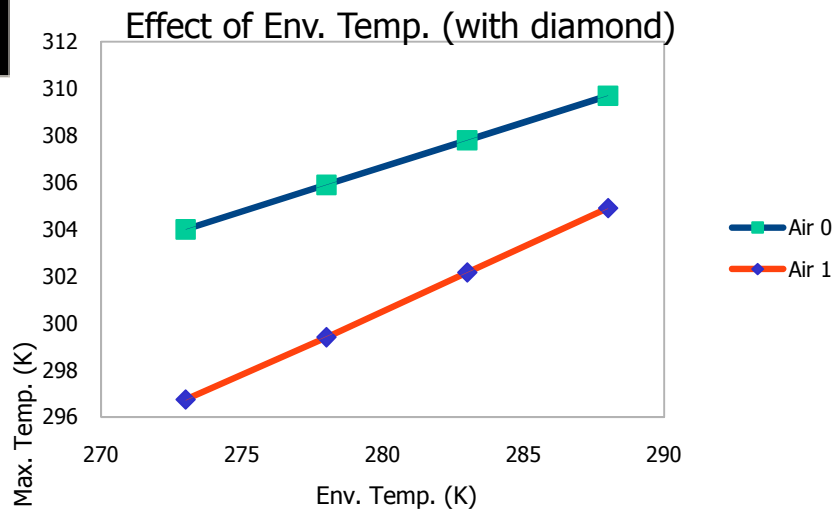
Introducing convection



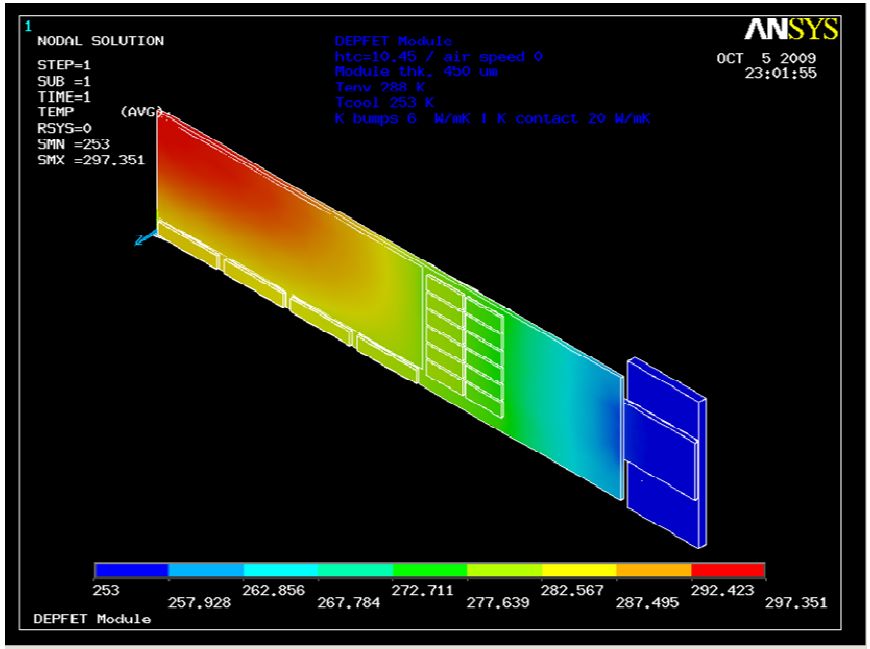


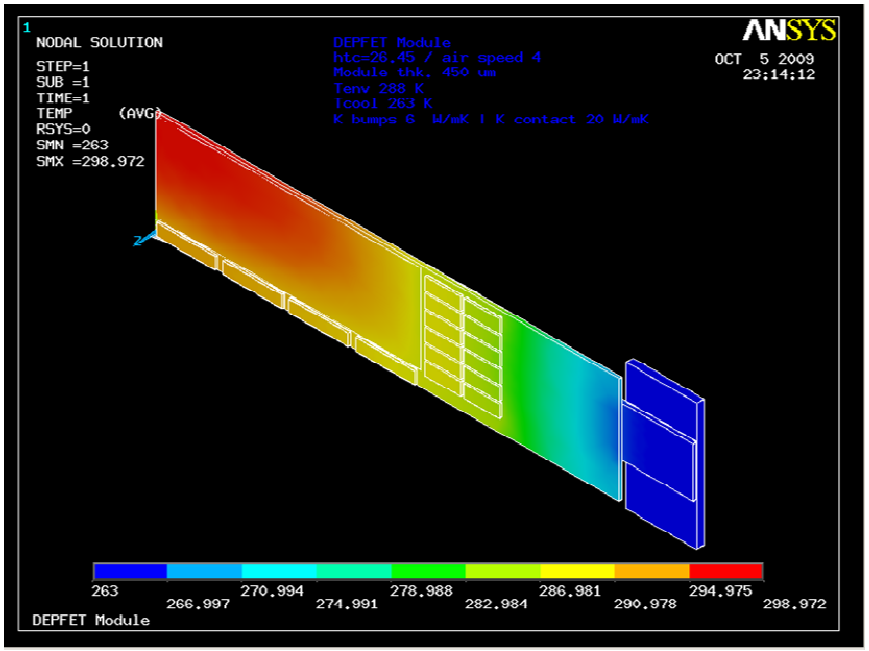
- $T_{CoolBlock}$=0ºC
- T_{max}=32ºC → Is this T low enough?
- Air 1m/s

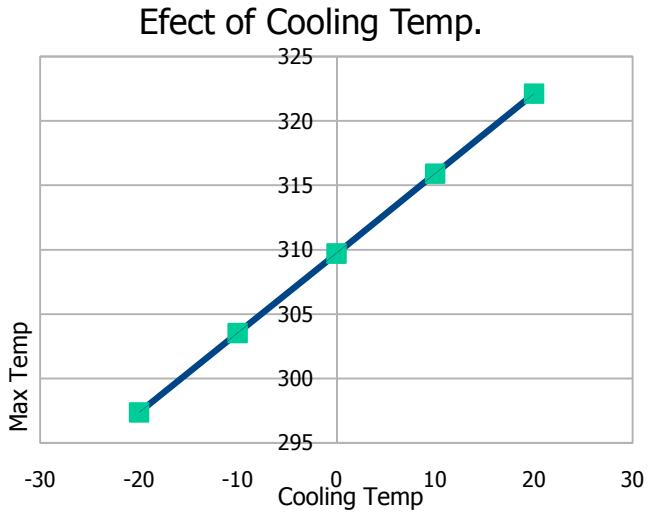
→ The situation is much favorable now…



Effect on cooling block's temperature



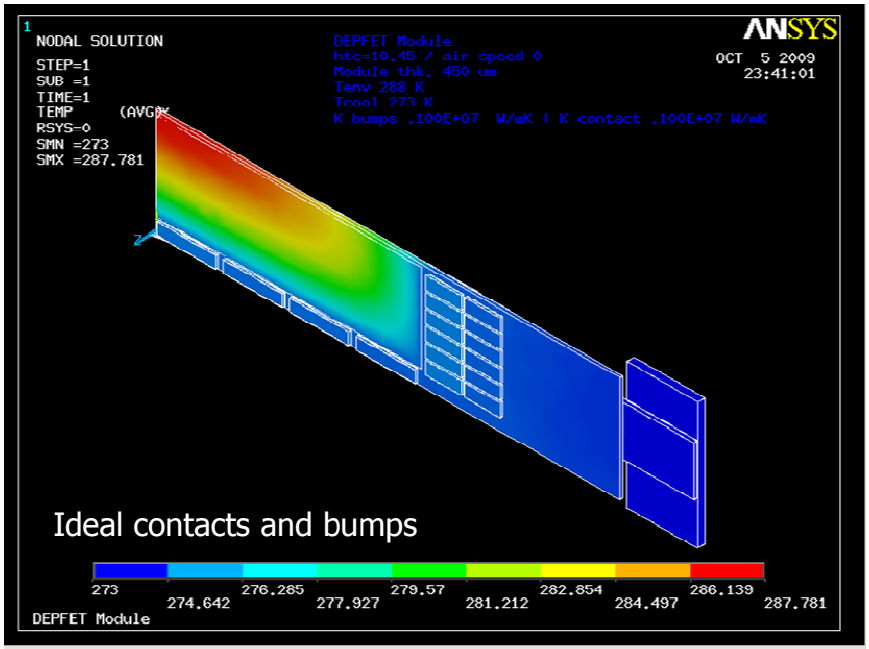


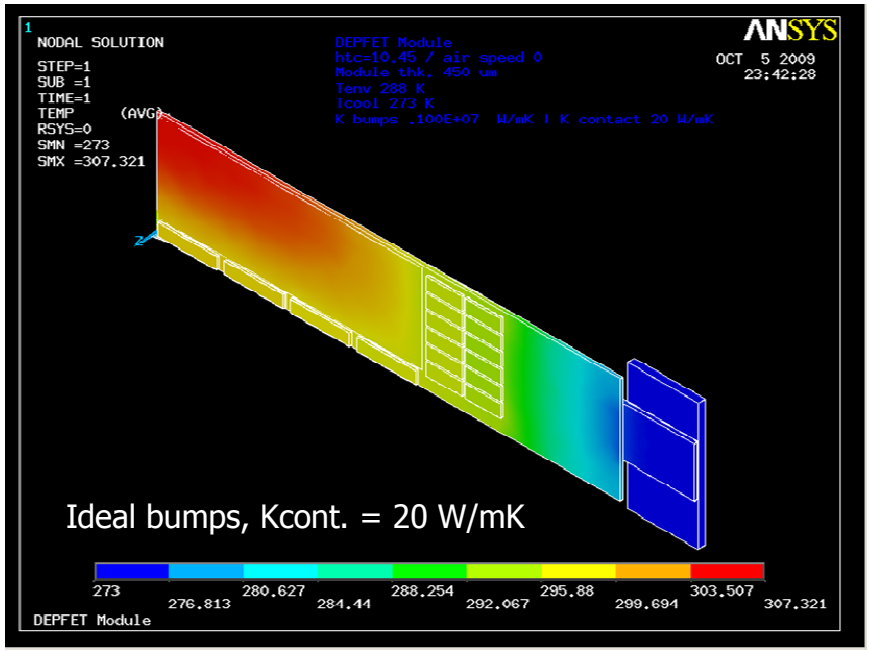


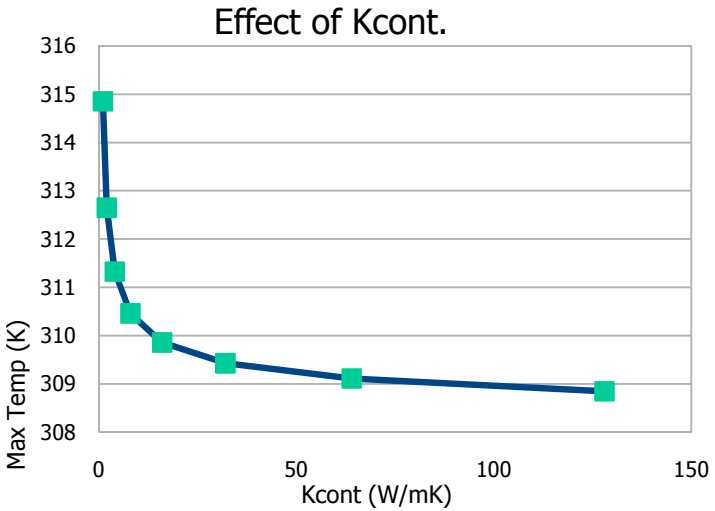
- We decrease 0.6 degrees for 1 degree less in the cooling block
- Efficiency quite low
- The sensor is still a problem
- Watch the T gradients in the 50µm foil of the sensor

→ Need to find another knob to play with max. T

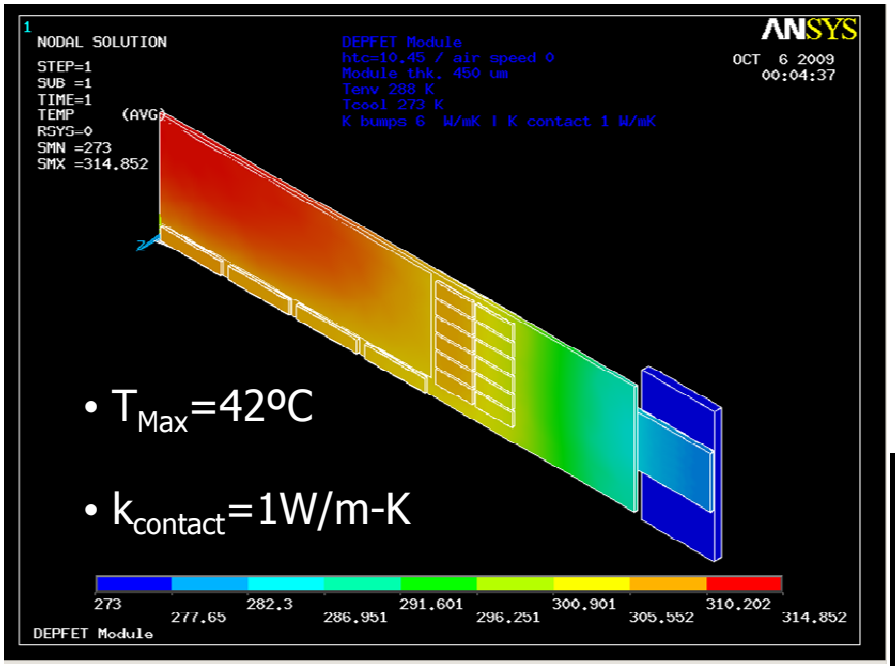
Effect on the $k_{Contact}$





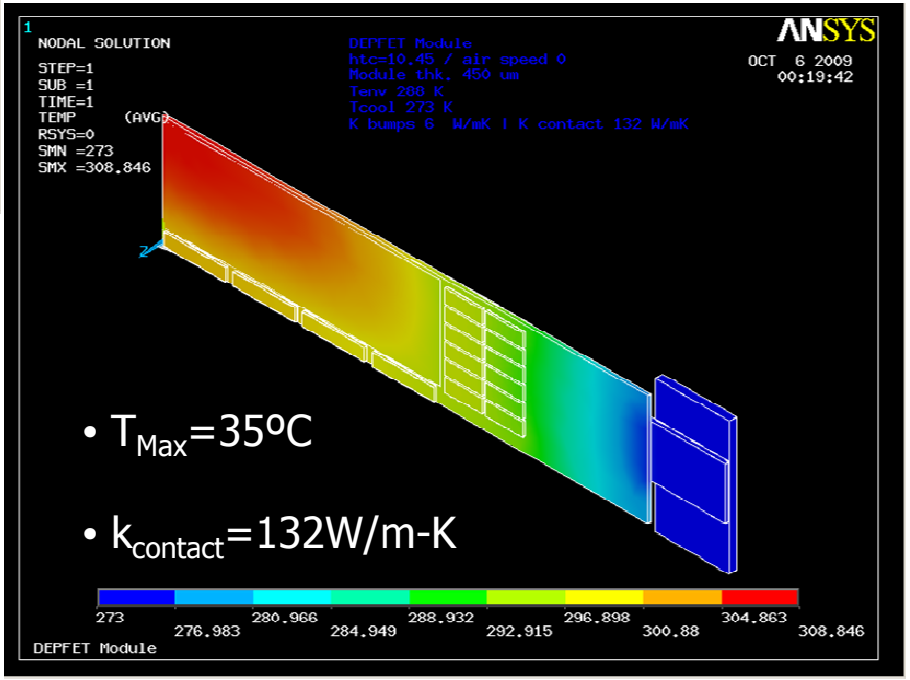


- Two contacts to be optimized:
  - Diamond-sensor
  - Diamond-cooling block



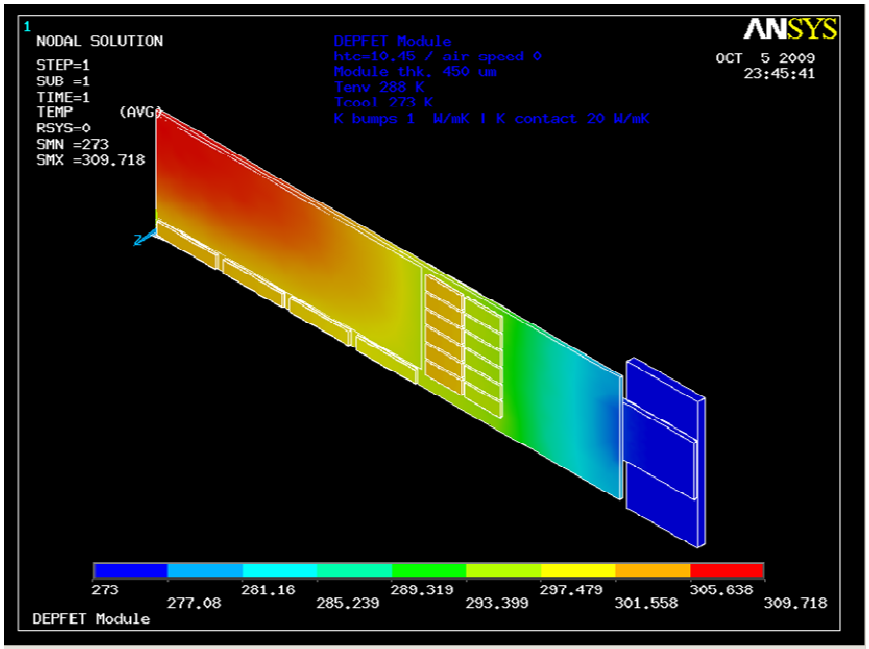
- T_{Max}=42ºC
- $k_{contact}$=1W/m-K

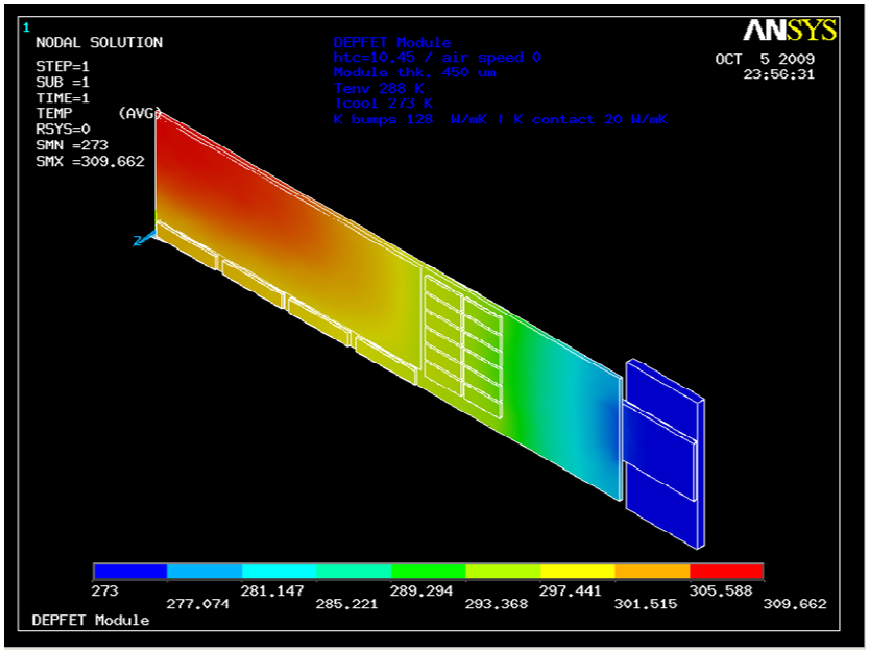
- $T_{CoolBlock}$=0ºC
- k_{bumps}=6W/m-K
- No air

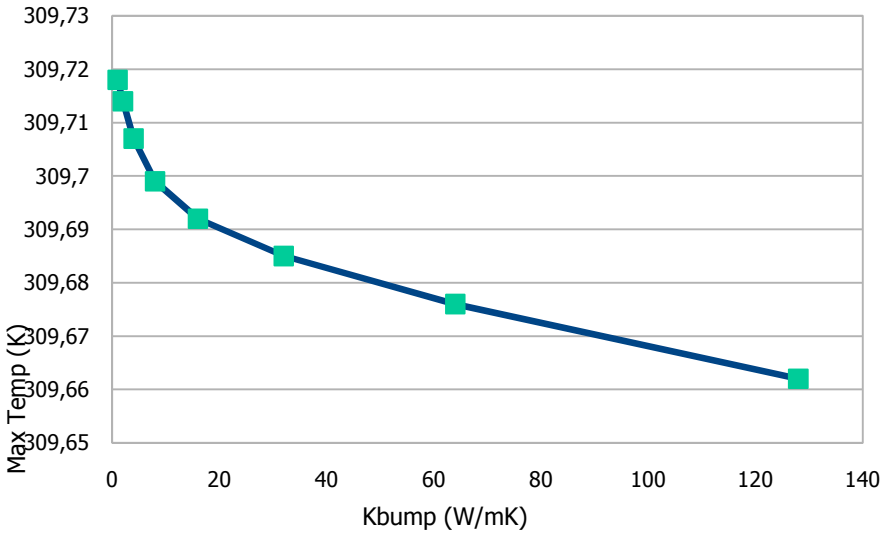


- T_{Max}=35ºC
- $k_{contact}$=132W/m-K

Effect on the k_{Bumps}

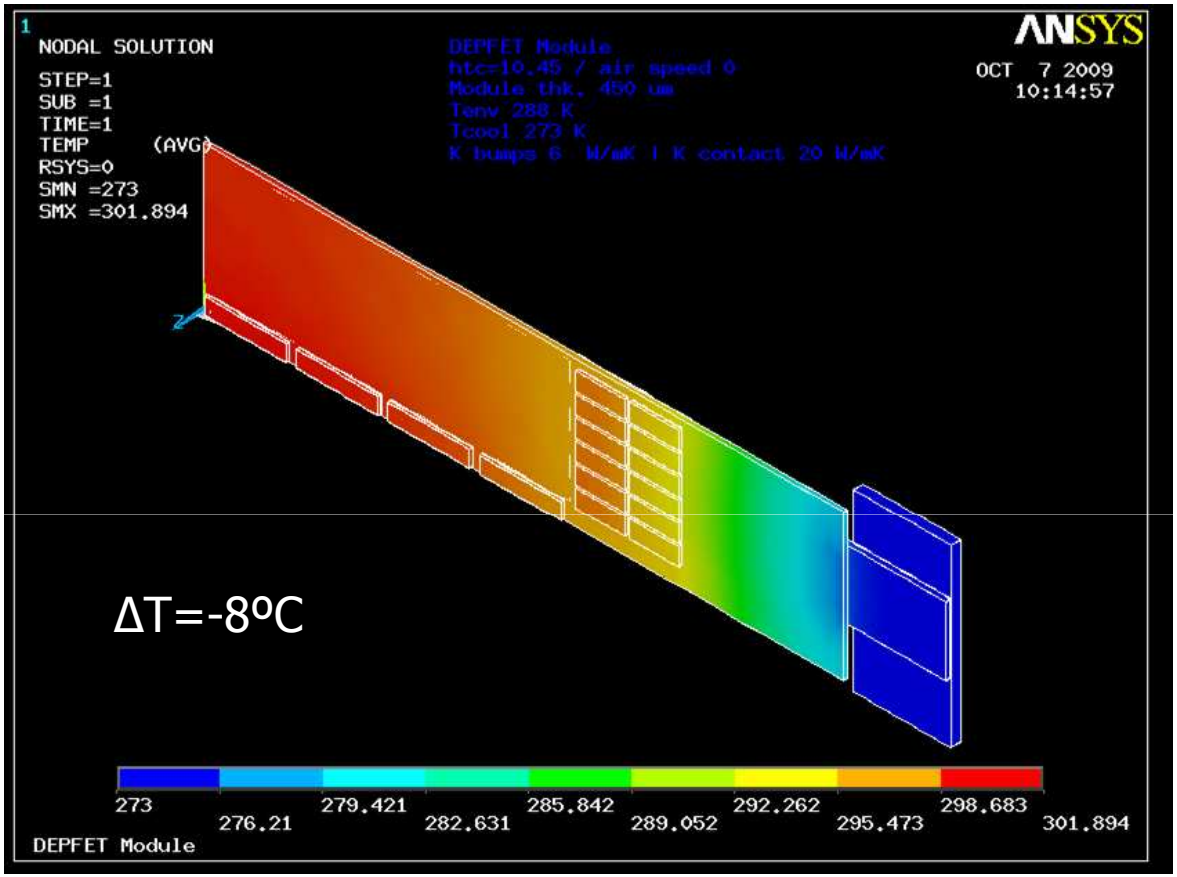


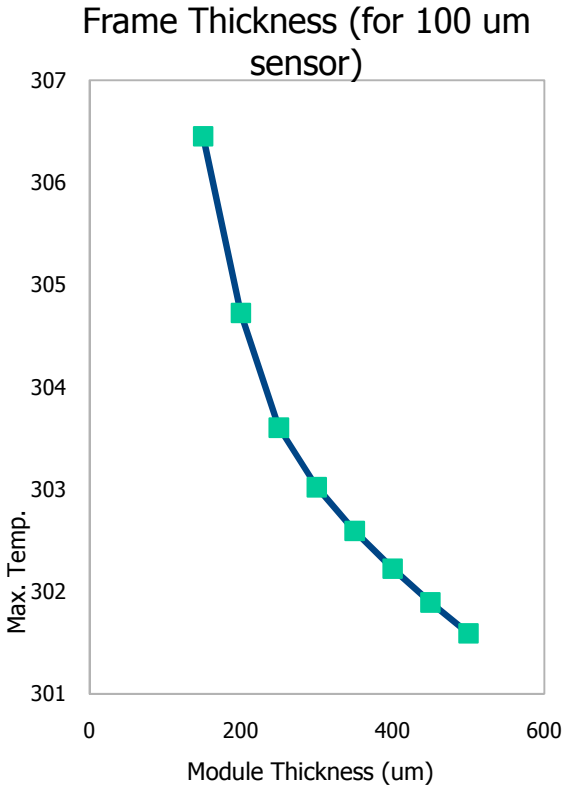




- Does not change the max. temperature.
- Chip temperature (DCD) varies a little from K=1 to 128 W/m-K

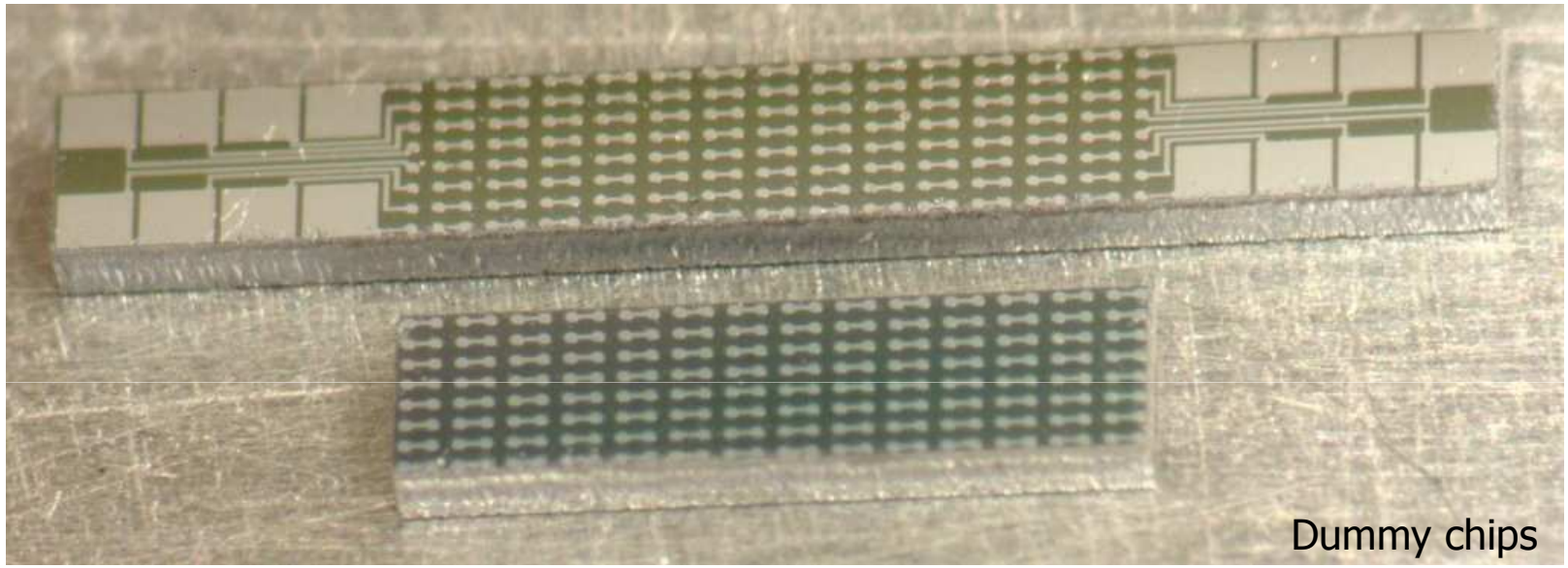
Thicker sensors?





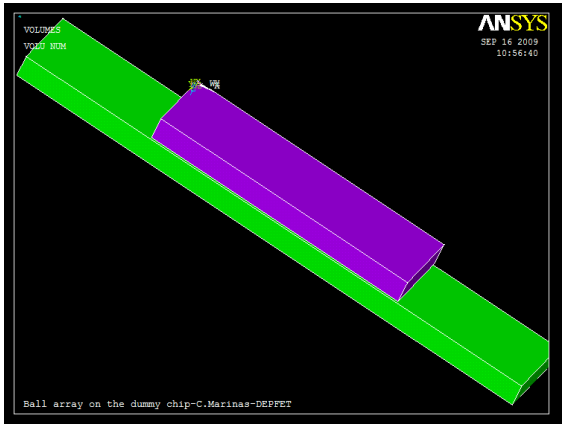
A 100 µm sensor helps cooling → 29ºC with free convection!

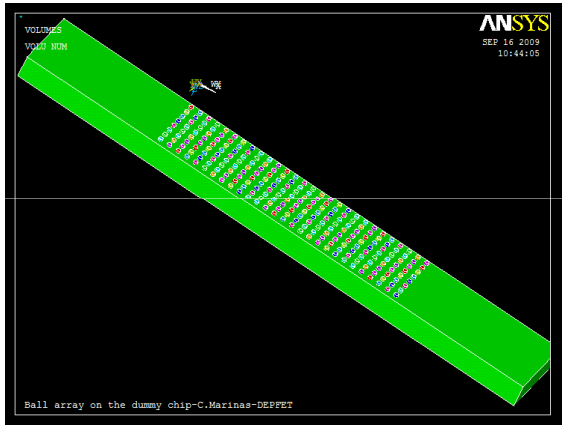
Flip-chip simulation

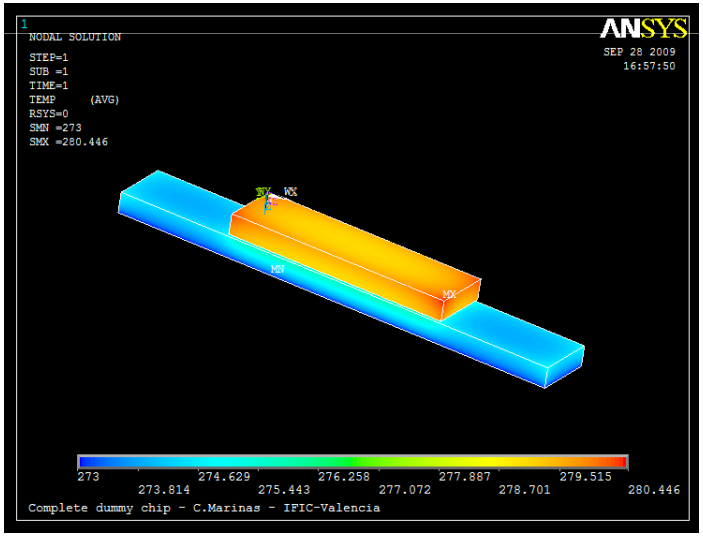


- Dummy chips created to test the electrical connections.
  - 450 µm thick dummy chip and substrate
  - Solder balls with and without gold underbump metallization availiable

FE dummy chip



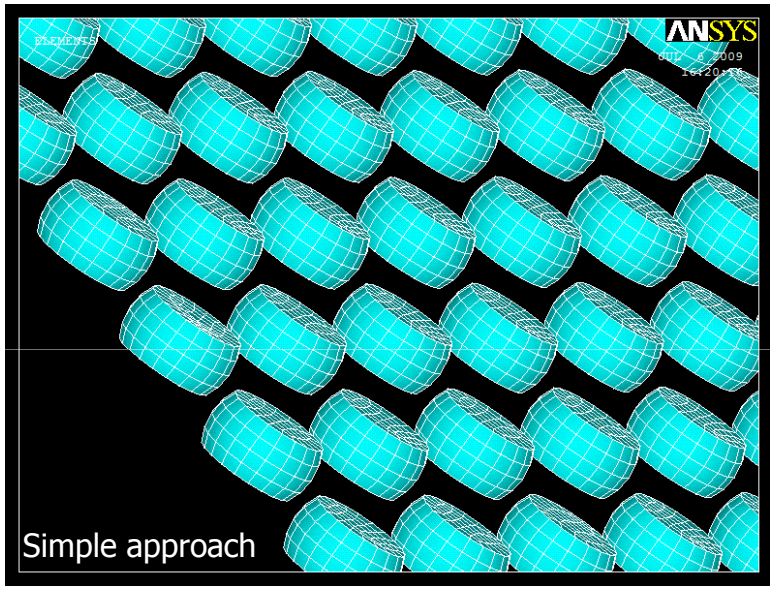


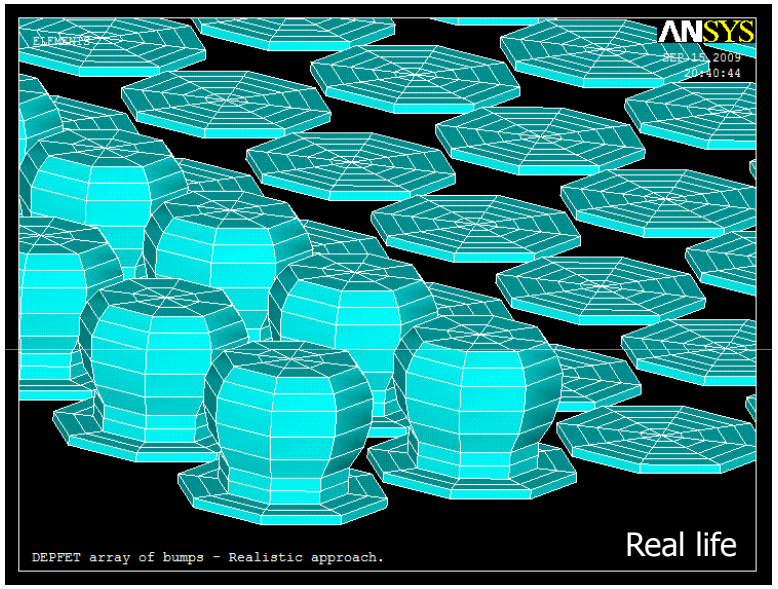


Geometry created in ANSYS package

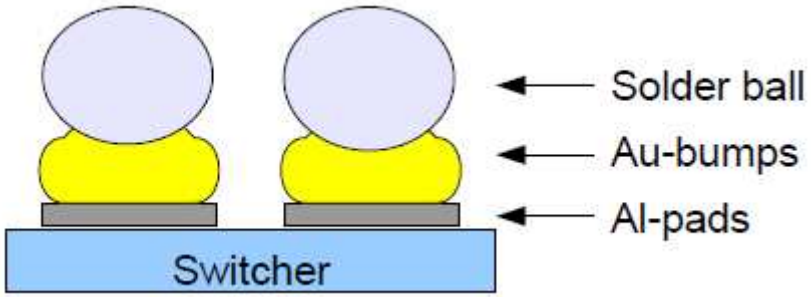
→ Measurements over the real dummy chip will calibrate our simulation

Future studies



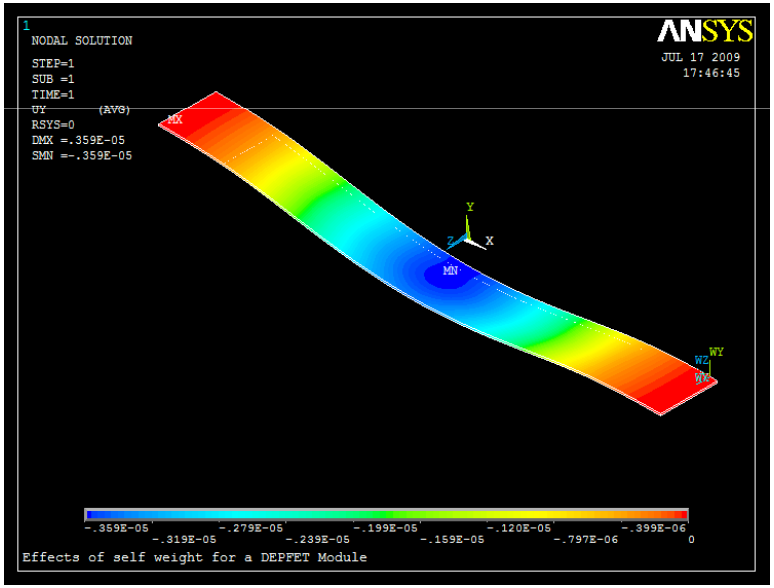


How close we are to reality?



Future plans

- Bowing effects due to the self weight
- Effects of the self weight + Temperature contributions
- Cross-check with metrology measurements
- Vibrations. Natural frequencies
- Thermal stress
- Effects on heat radiation
  - Beam pipe to inner/outer layers
  - Inner layer to outer layer



Summary

- List of parameters for thermal simulations have been created
- A couple of thermal solutions arised
  - Up/ Down cooling
  - Both solutions with pros/cons
- (Valencia) Studies are on the way
  - Working on the "Down" cooling solution
  - Flip-chip thermal studies for any cooling option
  - Self bowing (measurements and simulation) and thermal stress
- "Down" option present good performance if contacts optimized

Thank you very much!