UNIVERSITÄT
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PXD6 Switcher & DCD Balcony Status

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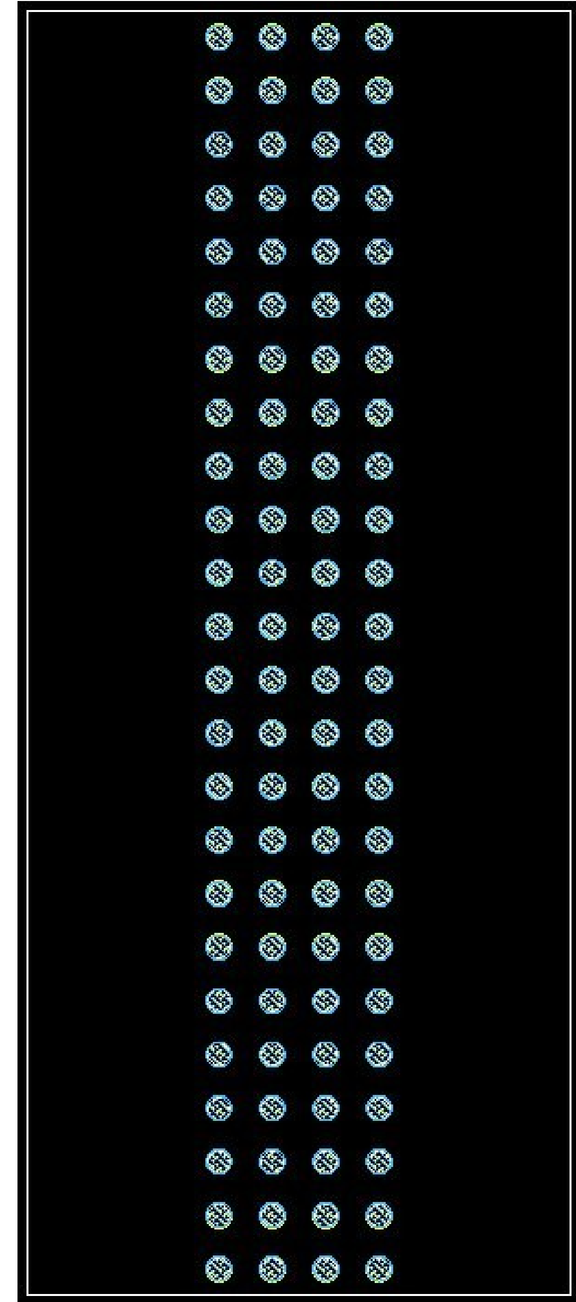
Switcher Balcony

Switcher-B

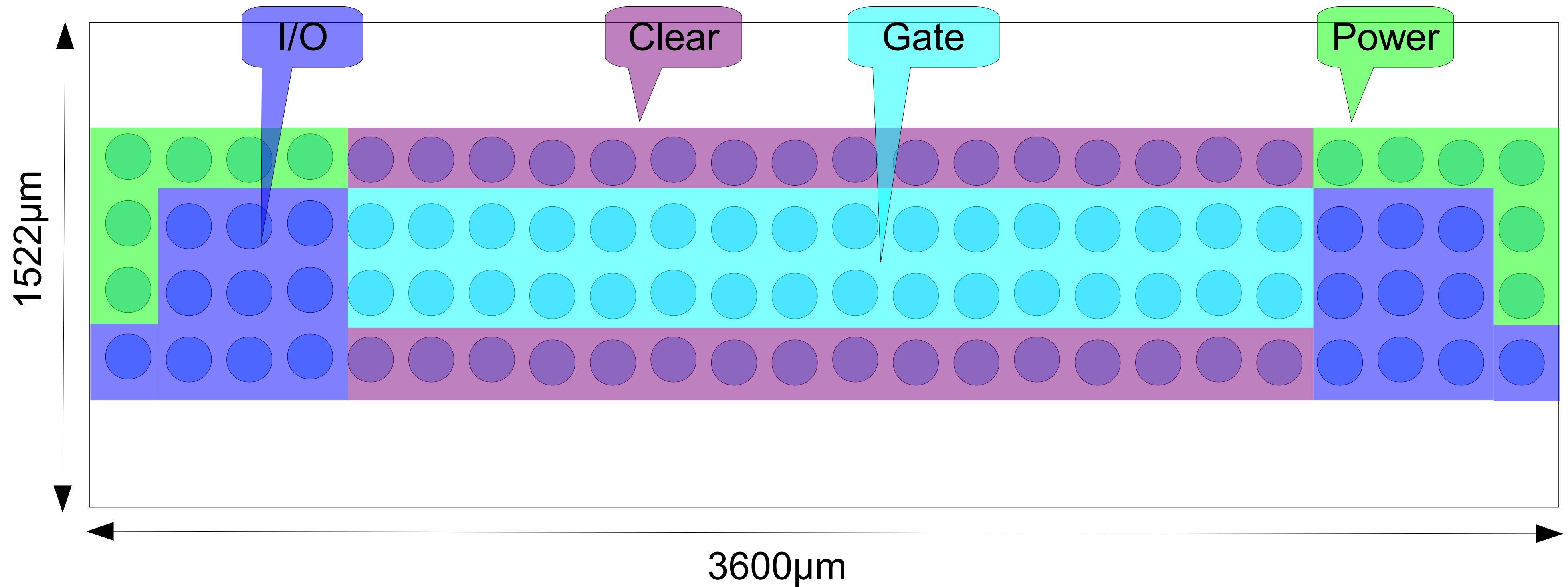
- Switcher for Belle
  - designed for PXD6 and final module
  - preliminary reference manual on Wiki available
- submission planned
  - next date: Nov. 2, 2009
- AMS 0.35µm high voltage technology
  - 1522µm x 3600µm chip size
  - 150µm bump pitch, 70µm Al-pads
  - 96 pads (32 Gate, 32 Clear, 14 Power, 16 I/O)
  - solder bumps or under bump metallization not available for miniasic

Switcher-B Summary

- 32 channels (DEPFET rows)
  - two outputs per channel, max 20V swing
  - GateHi, GateLo, ClearHi, ClearLo Power Inputs
  - channel selected sequencially with shift register
  - channel timing controlled by strobe signals
  - daisy chaining of shift registers of neighboring chips
  - shift clk, serin, serout, strobes are LVDS signals
  - build-in decoupling of Clear and Gate to DEPFET-source potential
- LVDS
  - configurable termination resistor and output current
- JTAG interface
  - testing and configuration of chip
  - configuration bits are triplicated and secured with majority voter
  - SEU can be detected by reading back registers



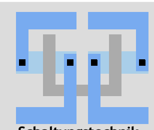
Switcher-B Pad functionality



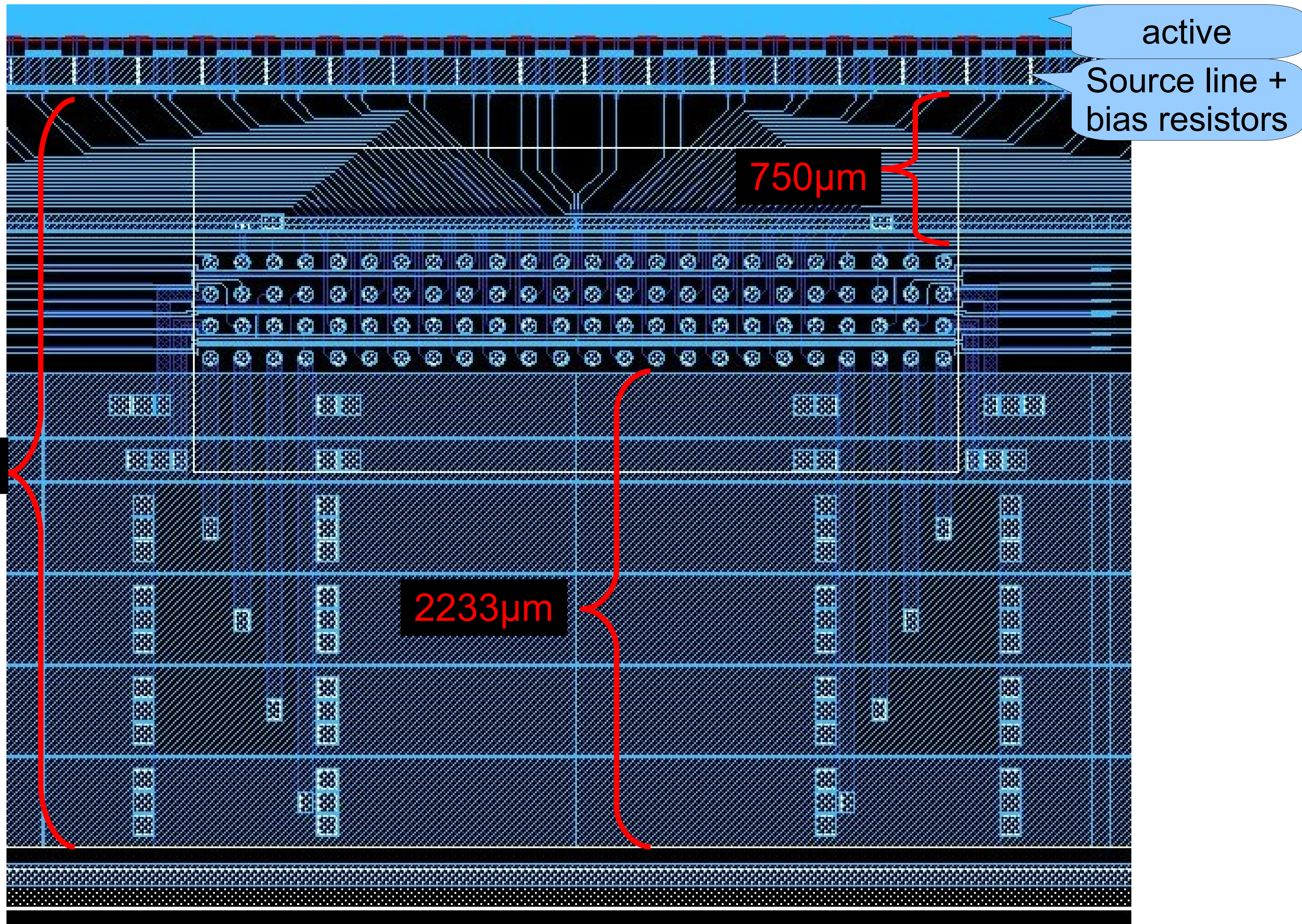
Switcher Bump Pad Layout

Switcher Balcony on PXD6

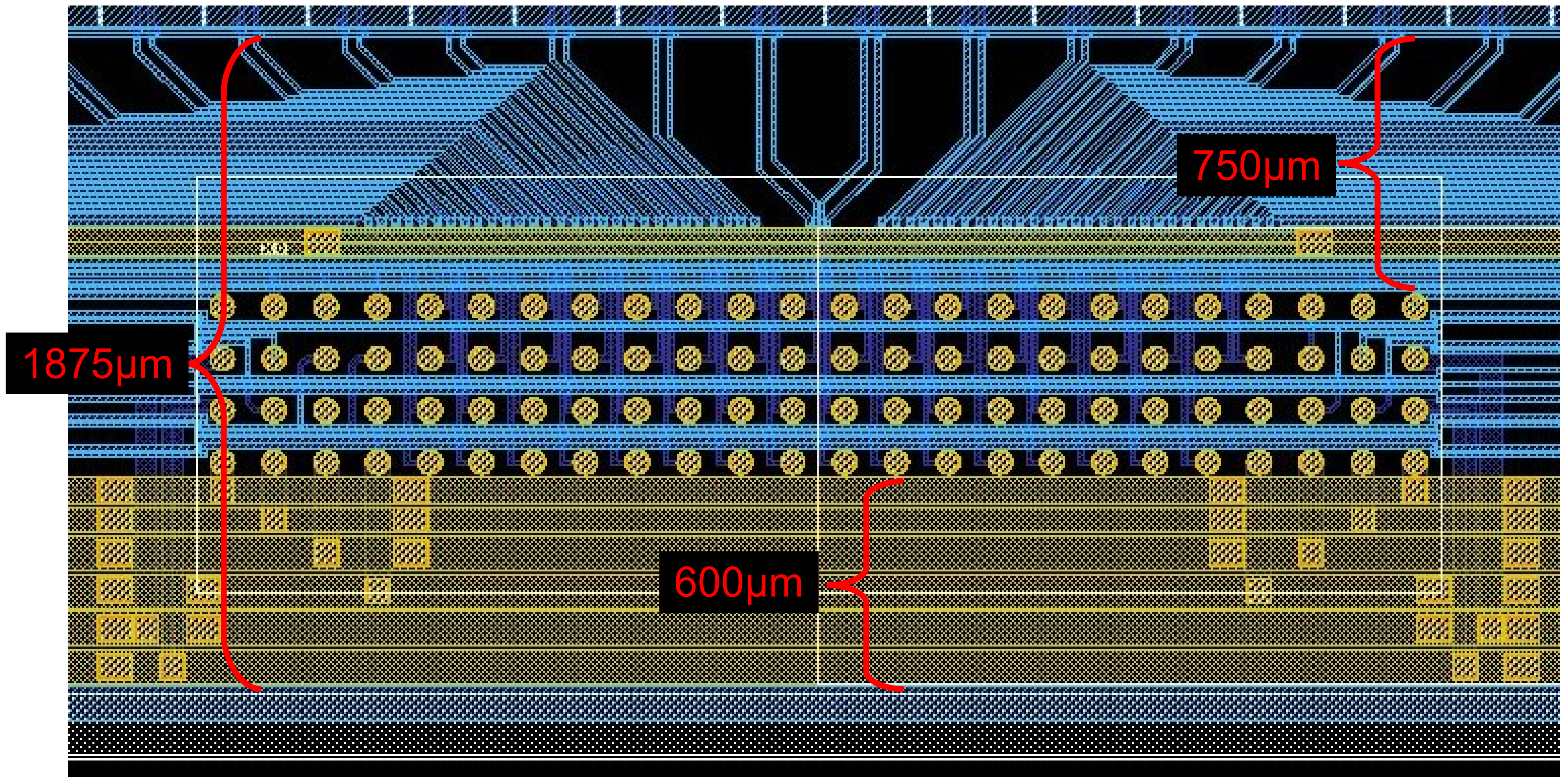
- both metal layer used in parallel to reduce R where possible
- larger gap between control lines to reduce crosstalk
- full available balcony width used for PXD6
  - 2 Al metal layer; 5cm long power busses; 15mΩ/sq
  - no 3rd layer (copper) available
  - gate and clear: 420µm width → 1.79Ω @26.5mA → 47mV drop
  - vdd: 200µm width → 3.75Ω @ 4mA → 15mV drop
  - gnd: 300µm width → 2.5Ω @ 8mA → 20mV drop
- balcony design fits in final module by shrinking power bus
  - 3rd metal layer (copper) will be available to reduce R: 3.75mΩ/sq
  - gate and clear: 100µm width → 1.86Ω @26mA → 49mV drop
  - vdd: 75µm width → 2.5Ω @4mA → 10mV drop
  - gnd: 75µm width → 2.5Ω @8mA → 20mV drop



Switcher Balcony on PXD6



Switcher Balcony on final module

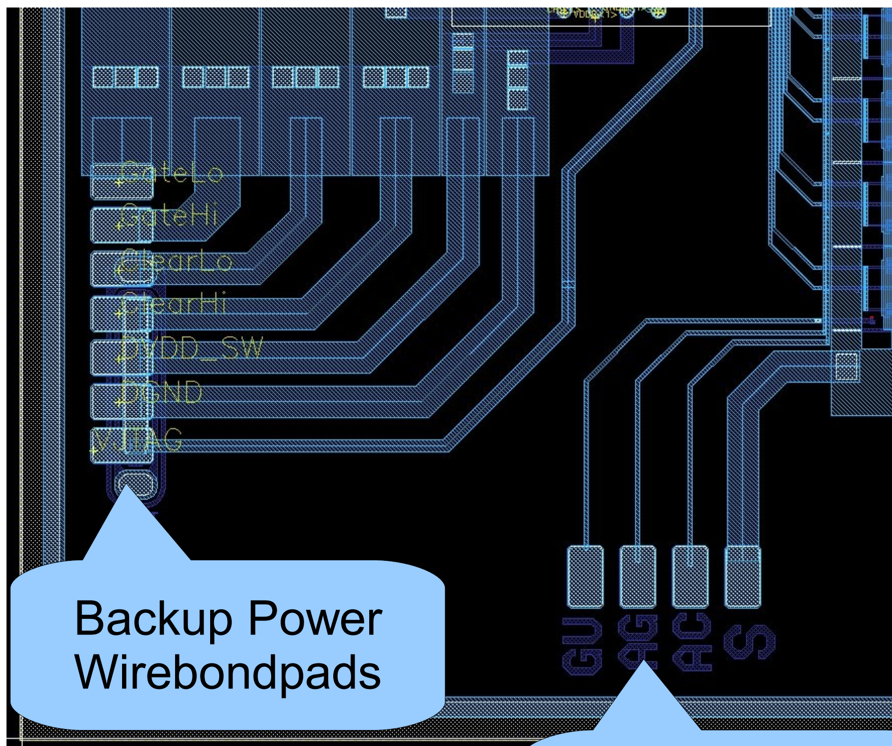


R + C

- rough estimation
  - used worst case on longest PXD6 module (Z100 type)
  - lumped R,C
- control busses
  - ~5cm length
  - 2 metal layers parallel where possible
  - tRC= ~3.6ns
- fanout from switcher to matrix
  - longest line ~6.2mm
  - 2 metal layer, 3rd metal not available due to small trace width
  - adds ~8pF to matrix capacitance
  - tRC = ~830ps (10% ↔ 90%) for 58pF
- ToDo
  - build RC-networks by hand and simulate
  - more precise extraction of RCs

Switcher Wirebonds

- All Switcher connections on DCD-end of the balcony
- Backup power pads on the other end



Control & Power Wirebondpads

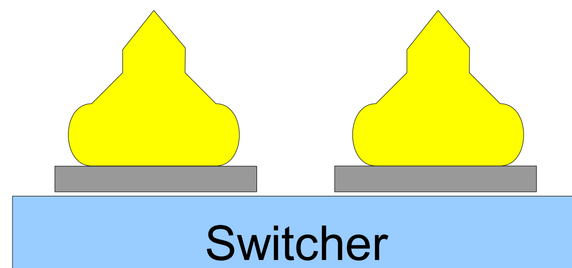
active

Switcher Bumping

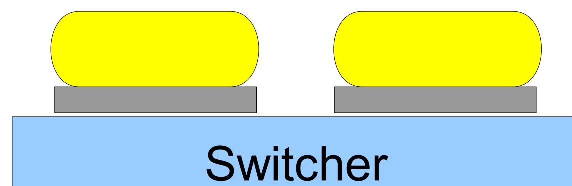
- AMS does not offer solder bumping
- solder bumping benefits
  - to be able to de-solder a broken chip
  - no high bonding force needed → compatible with thinned devices
- Al-pads are not wettable by solder
  - under bump metallization needed to create wettable surface
- have to place our own solder bumps with machine
  - need under bump metallization; use gold studs

Switcher Bumping

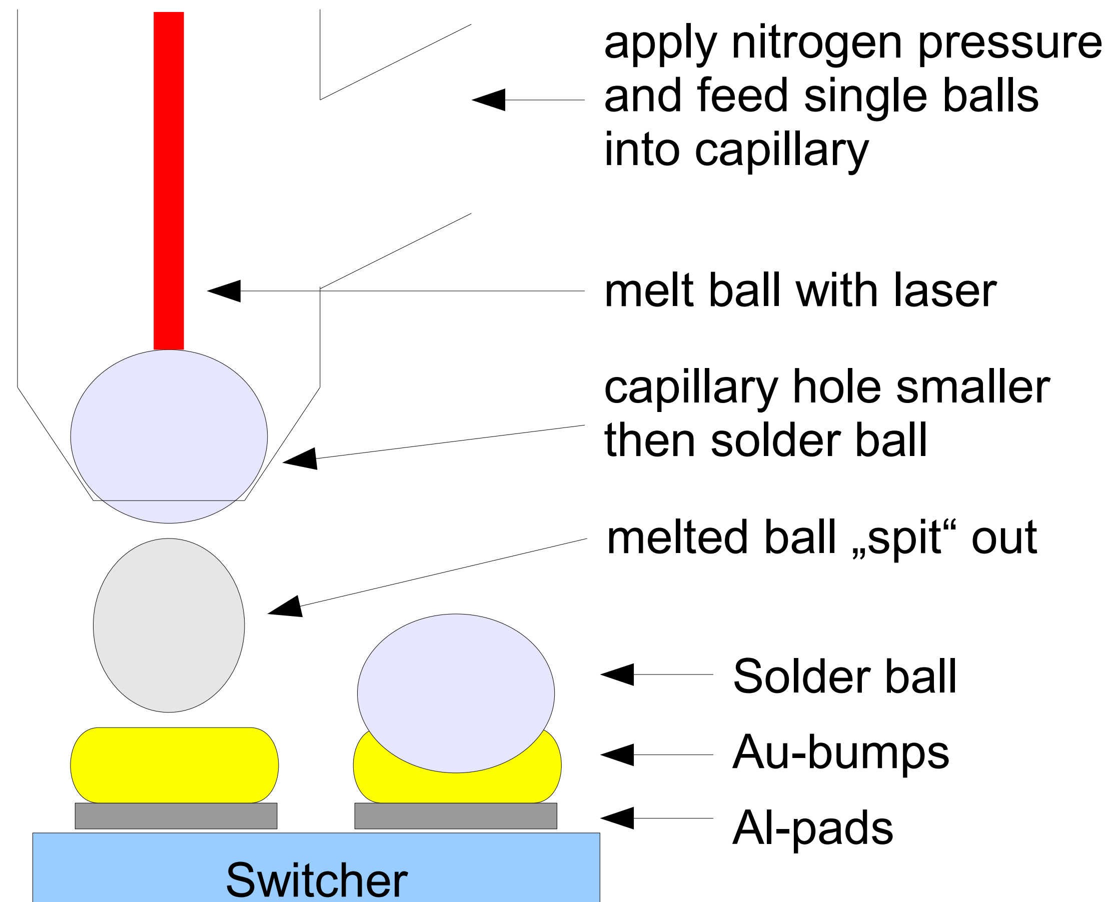
- commercial solder bumping not available for Switcher
- use coined gold studs as an under bump metallization
- place solder bumps ontop using PacTec solder jetting technology
  - 60µm minimum ball size available
  - SnAgCu solder
  - Pb-free



1st : place goldstud



2rd : coin gold studs



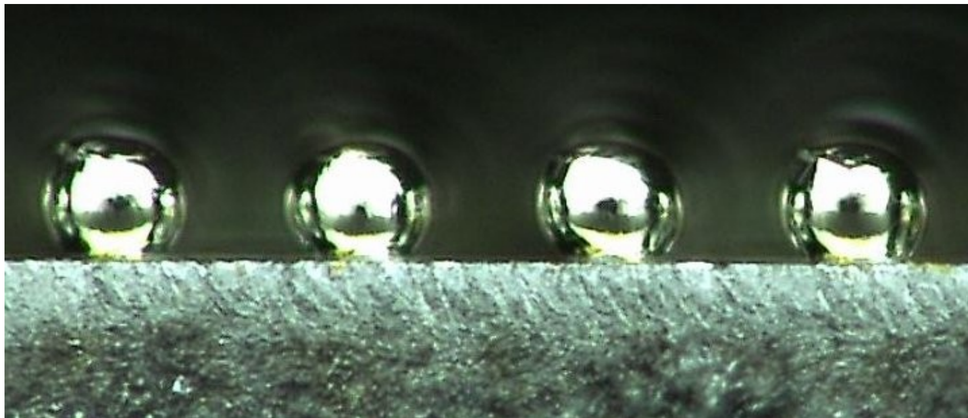
3rd : jet solder balls

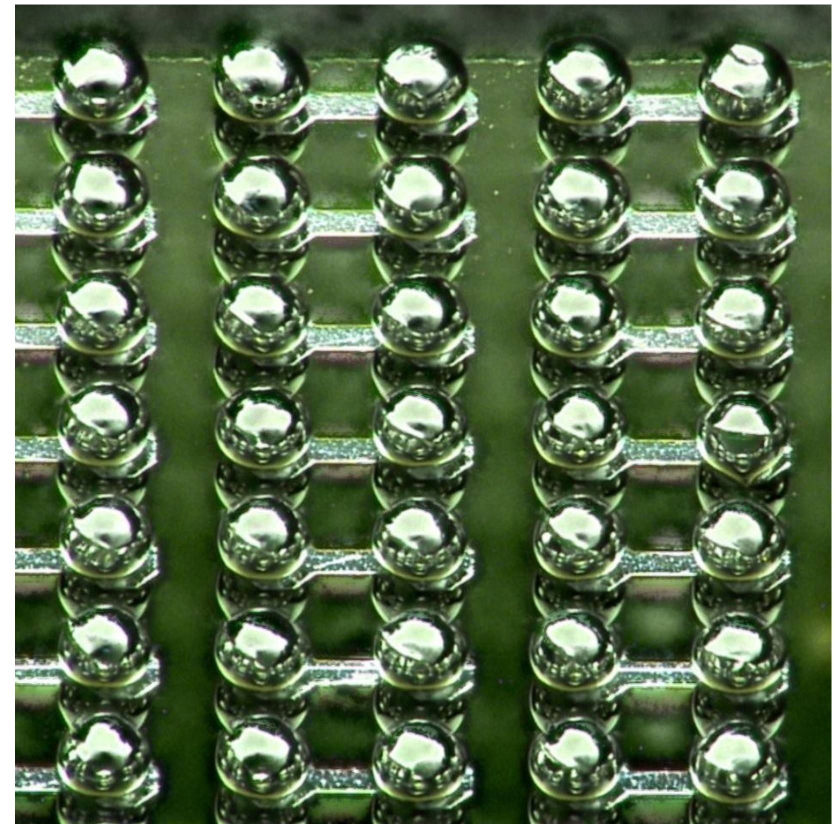
Reliability of solder on gold studs

- concerns about gold-tin intermetallics
- combination of gold-studs and solder used in mass production of commercial DRAM chips
  - Si Chip with gold studs is soldered onto PCB and molded into package
  - AuSn4 intermetallic is brittle
  - different CTE of Si and FR4 causes cracks during bake and cure steps
  - underfilling and soldering at once gives best results
- benefit of all Si module
  - same CTE of chip and substrate
  - underfill stabilizes assembly
  - to be tested with dummy chips
- Woong Sun Lee, et al., “Reliability Issues on the High Speed DRAM Flip-chip Package Using Gold Stud Bump, Lead Free Solder, and Underfill”, IEEE Electronic Components and Technology Conference 2008

Switcher Bumping

- send some dummy chips with coined gold bumps to PacTec
- PacTec placed solder bumps using solder jetting technology
- received back solder balled samples
  - 100μm ball diameter

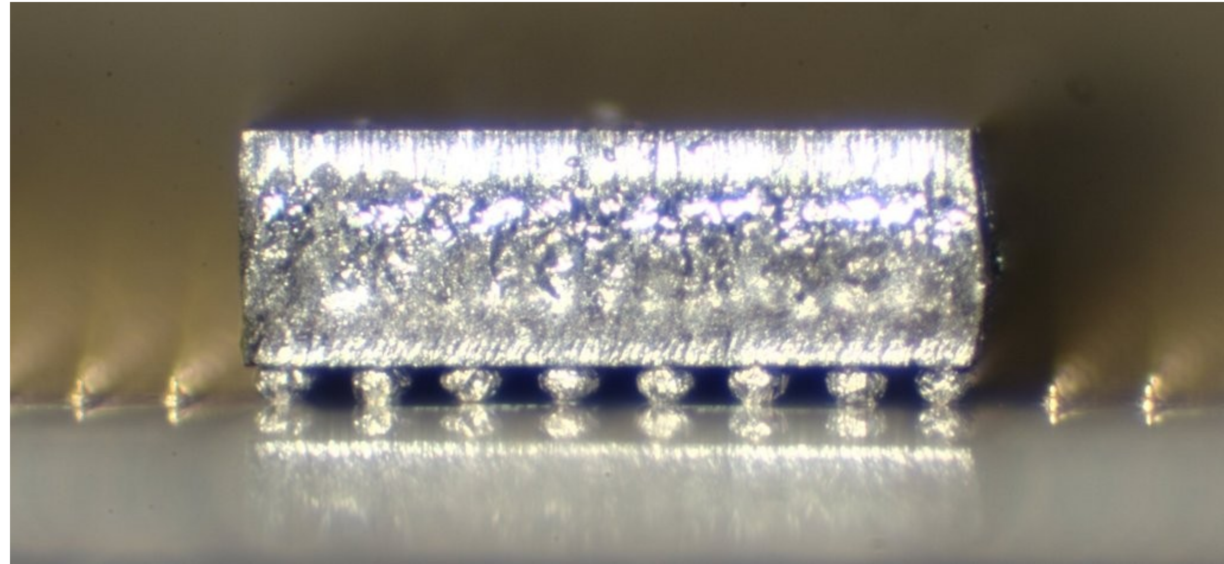




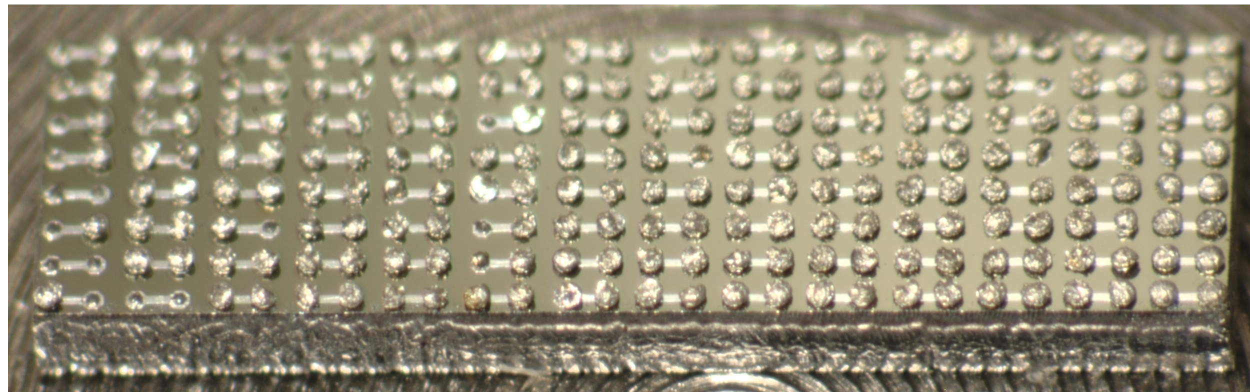
side and top view of dummy chip with PacTec solder ball placed ontop of coined gold bumps

PacTec solder bumping

- successfully soldered
- good connection
- successfully desoldered
- need to remove solder residues after desolder
  - PacTec machine has vaccuum solder cleaner option



side view of one soldered chip on a tripple substrate

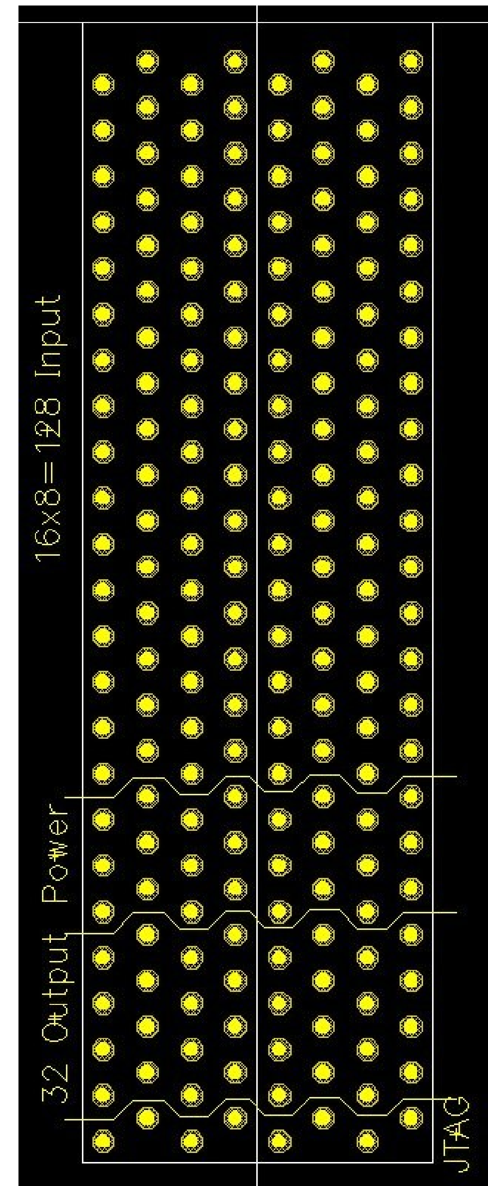


top view of an desoldered chip

DCD

commercial DCD bumping

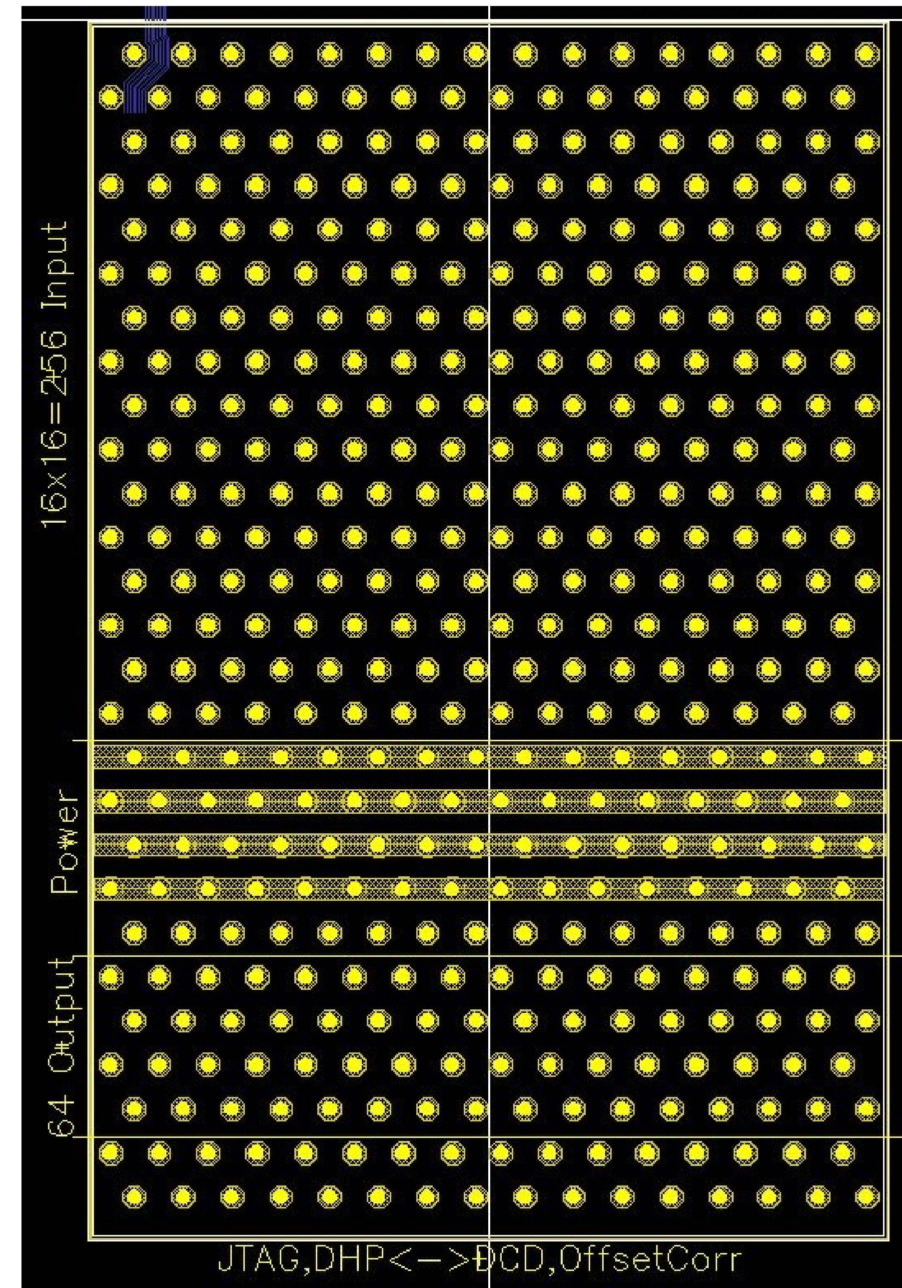
- commercial bumping is available for UMC 0.18µm technology on a multi-project wafer run
  - 200µm pitch required, 140µm gap
  - Eutectic, high lead and leadfree available
  - printing, plating and ball drop available
  - Al redistibution metal layer available
  - BCB, PI or no passivation available
- old DCD design didn't match new bumping rules
- several new design options checked
  - some were not drc clean
  - some didn't have enough input pads
  - some didn't have enough power pads



unsuitable DCD design

new DCD geometry

- new geometry
  - 2x3 miniasic: 3280µm x 5000µm chip size
  - bump pitch: 200µm in x, 180µm in y (staggered), DRC clean design
  - 431 bumps
  - 7th metal layer available for connecting bump pads to input cells
    - 6th metal layer free: routing and wide power busses → low voltage drop
  - 256 Inputs
    - 3 DCD for PXD6
    - 4 DCD for final design (1000 drains)
  - input cell size: 200µm x 130µm
  - plenty of pads for power and control
  - planned submission: Nov. 2, 2009



new DCD features

- 8 slices per chip
  - 32 analog inputs
  - ADC values multiplexed to 8-bit parallel output
  - 2-bit offset correction inputs
- JTAG interface for slow control and chip testing
- single ended data in- and outputs
- single ended DHP<->DCD control signals
- smaller cell size
  - gained space for onchip decoupling or offset correction memory
  - lower voltage drop across cell array
- power pads are lined-up to create rails with max line width

DCD on PXD6

- high power consumption of DCD problem on PXD6
  - only 2 metal layers
  - trace resistance high due to space restrictions
  - → need to supply each DCD seperately
  - → uses sense lines
- drains are connected sequencially to DCD inputs
  - fanout has to use both metal layers and minimum trace width
- connection to DHP only one metal layer
  - second (and 3rd) metal layer can be used for horizontal power bus

DCD at PXD6

suppy splitted to left and right module side

700µm

6500µm

supply of left DCD

supply of right DCD

540µm

1030µm

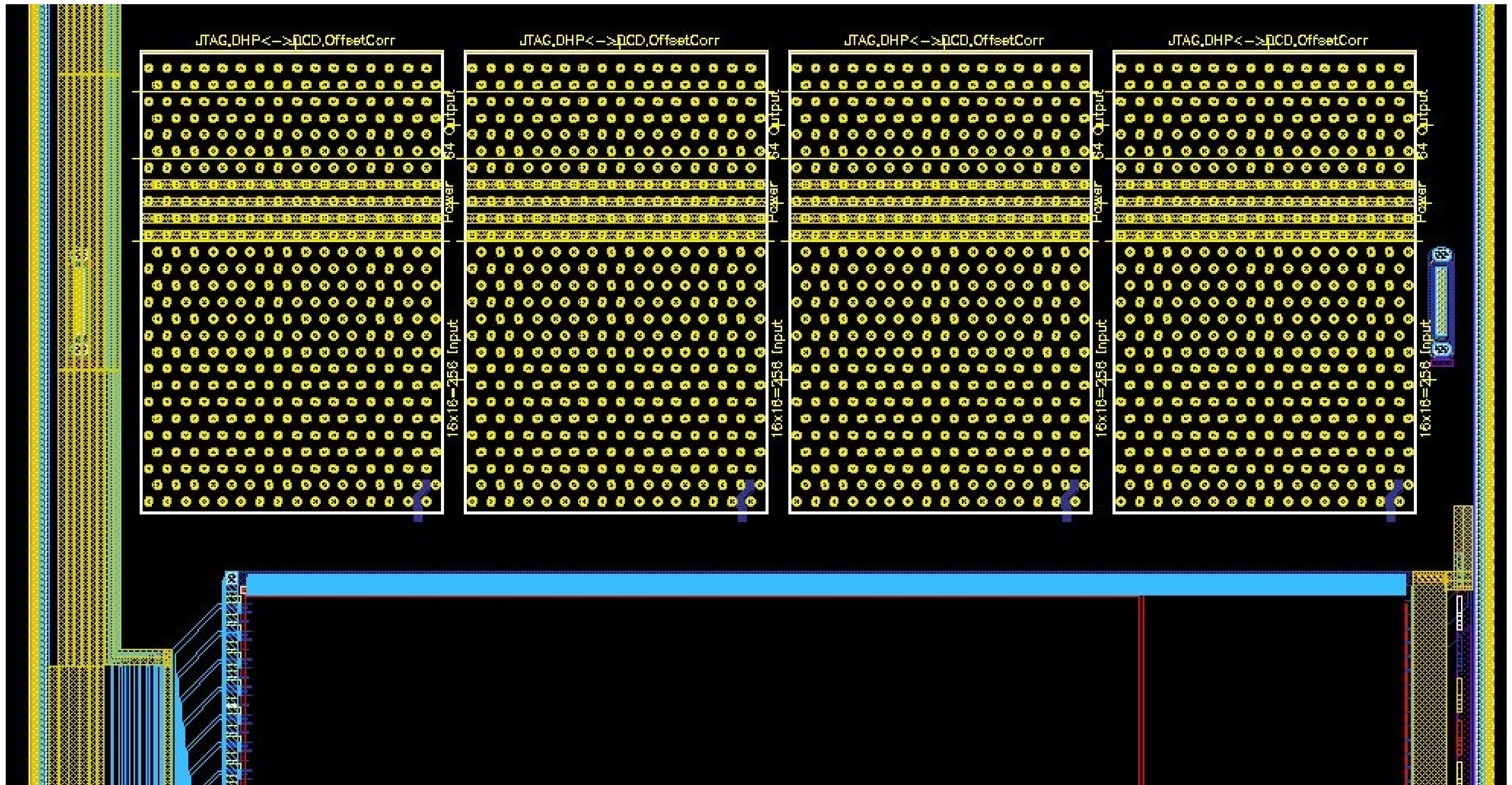
Switcher Control Busses

Matrix Supply

DCD on final module

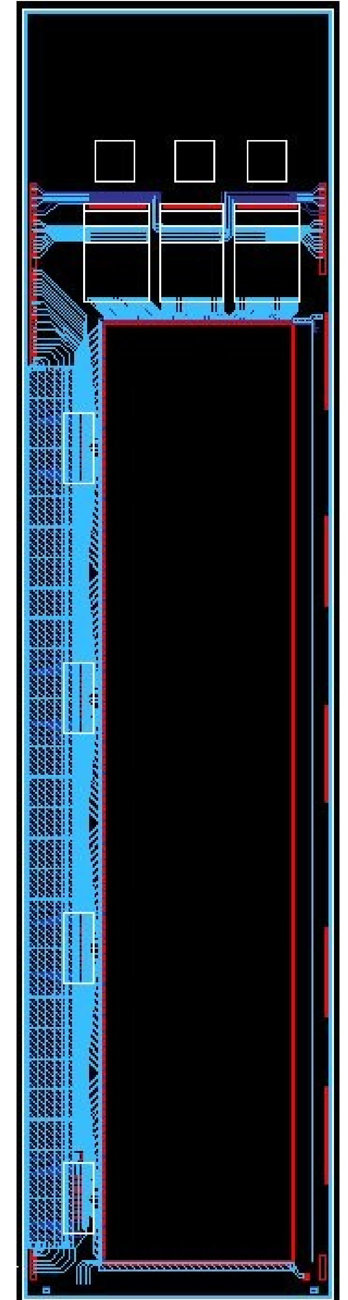
- 4 DCDs
  - 3280µm design width
  - cutting edge: 55-65µm
  - gap between chips >200µm
  - space needed: 13720µm
- active area 12500µm width
- 1220µm wider than active area: 610µm left and right
  - left side ok: 750µm space between active and switcher control busses
  - right side:
    - ~350µm occupied for matrix supply (Source, Bias), could be smaller with copper layer
    - 470µm needed for the right DCD if chips are left-aligned

DCD on final module



ToDo

- PXD6
  - detailed simulation of risetimes (RC-networks)
    - extract or calculate more precise RC of traces
  - LVS check of Switcher and DCD wiring
    - created LVS config files for PXD6
    - simple LVS test already works
  - finish layout
- Dummy chips
  - wirebond adapter for Switcher and DCD
  - layout for testing connector mounting



Thank you!