Data Handling Hybrid (DHH) Design Ideas and Issues

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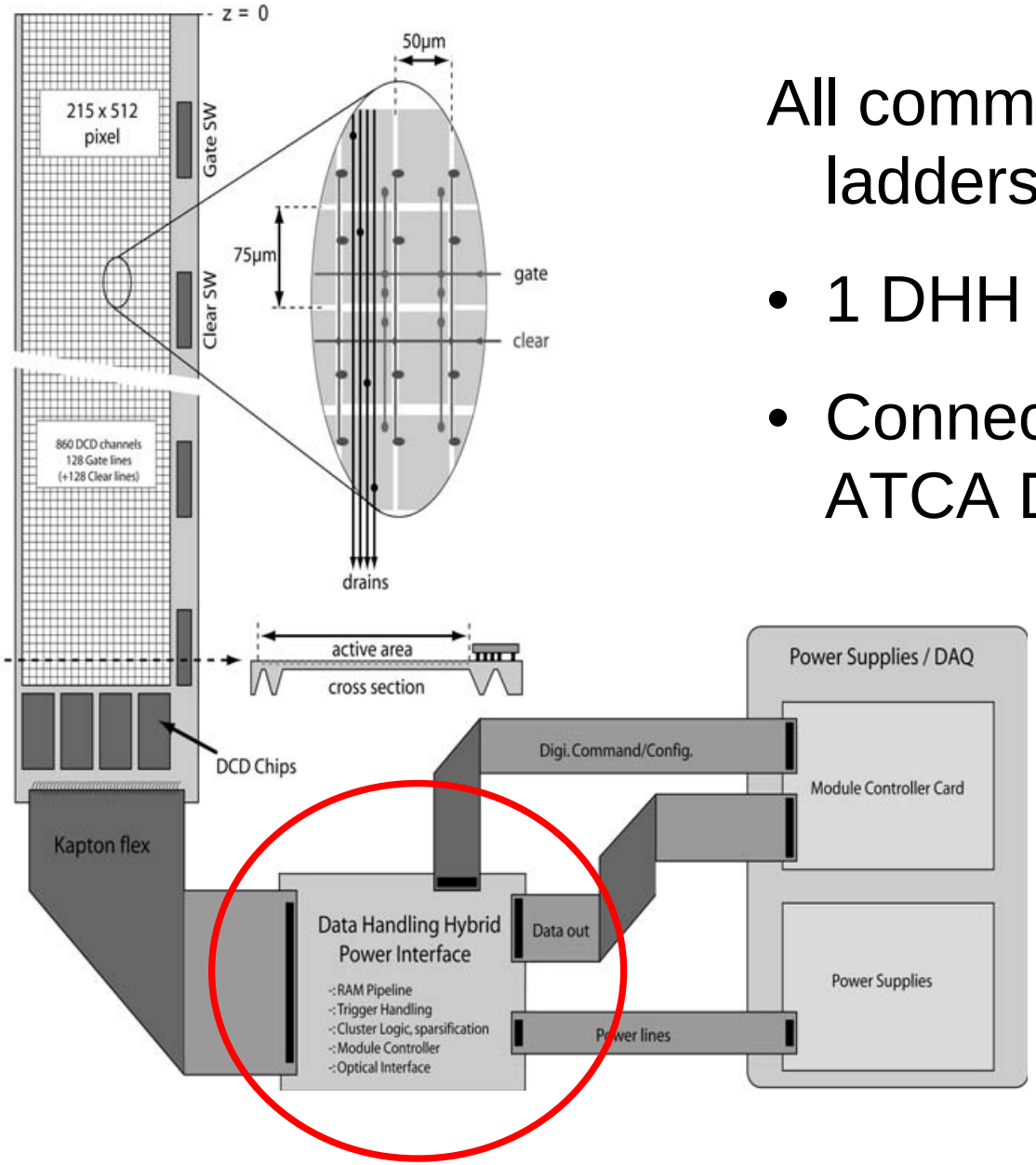
Tasks of the DHH



All communication from and to the ladders goes through the DHH !

- 1 DHH per half-ladder (total 40)
- Connection between DHP and ATCA DAQ system

- **Impedance matching**
- **Electrical ↔ optical**
- **Power filtering**
- **Local power regulation (?)**
- **Slow control (JTAG)**

DHP requirements

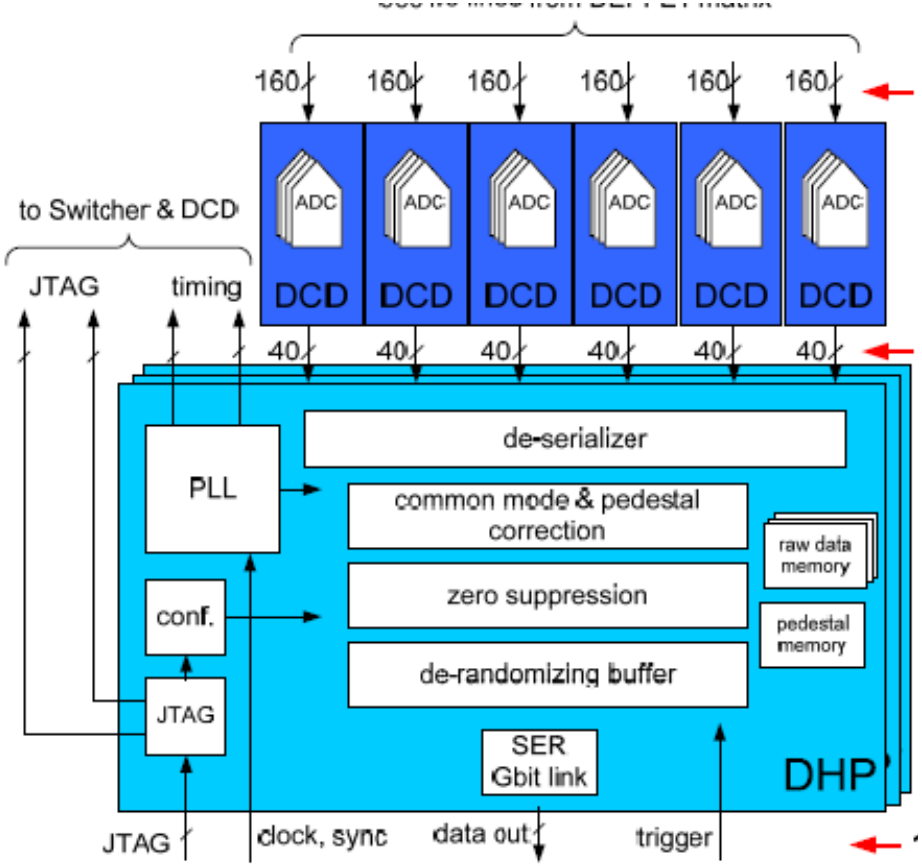


Table of signals for the DEPFET module

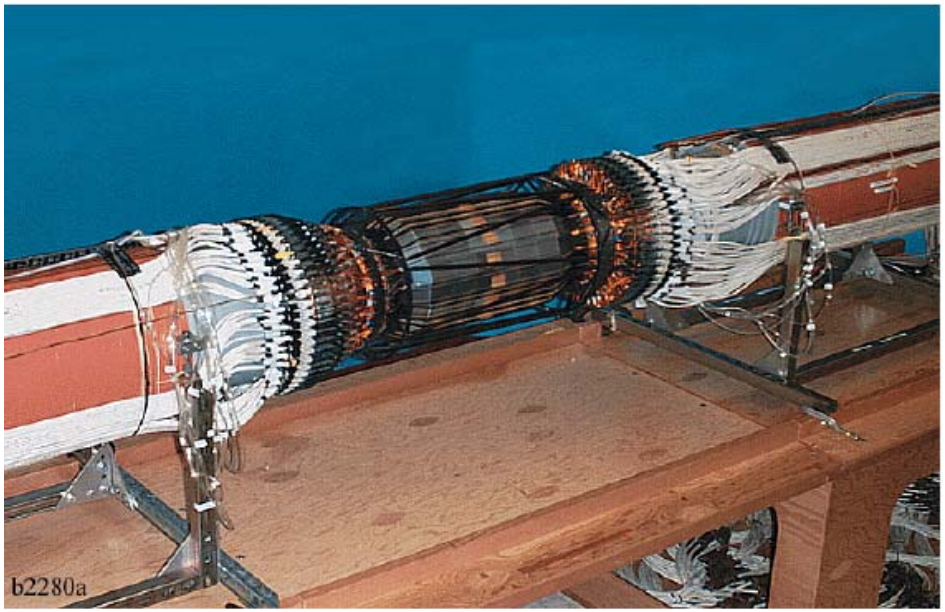
Signal name	Type	Description	Comment
GCK	LVDS in	42.3 MHz (?) system clock	RF clock (F0) devided by 12
FCK	LVDS in	99.2 kHz frame clock	synchronous to the beam gap
TRG	LVDS in	trigger	10-30 kHz
TMS	LVCMOS in	JTAG mode select	change to LVDS?
TCK	LVCMOS in	JTAG clock	
TDI	LVCMOS in	JTAG data in	
TDO	LVCMOS out	JTAG data out	
RST	LVCMOS in	reset	for all chips? polarity?!
DO[5:1]	CML out	DHP data out	one per chip

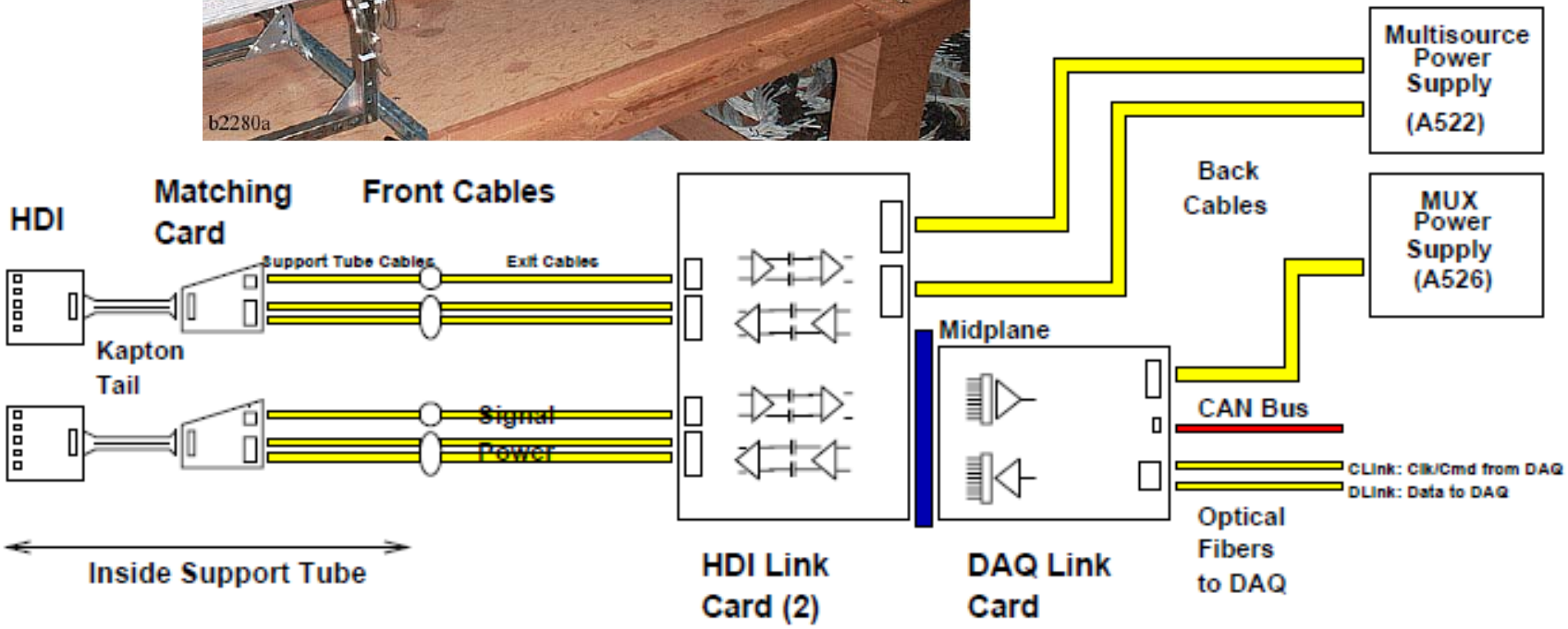
+ power lines

From Hans Krüger

- un-triggered r/o → 6-8 Gbit/sec per module, 1-1.3 Gbit per link (x6)
- triggered r/o (10 kHz) would require 1.8 Gbit per module only

Data Transmission for the BaBar SVT





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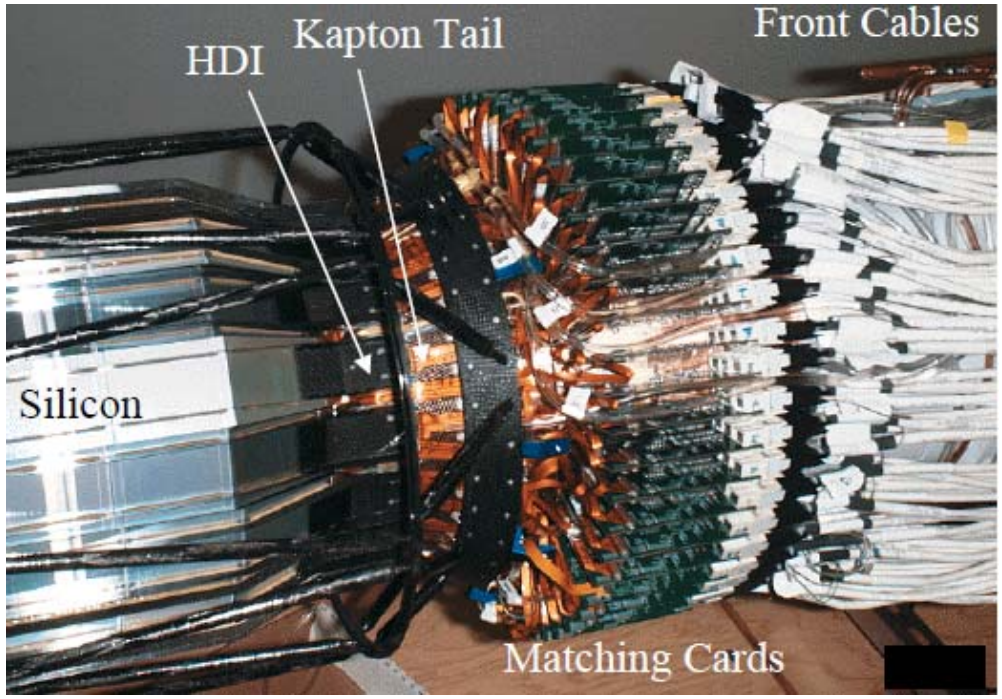
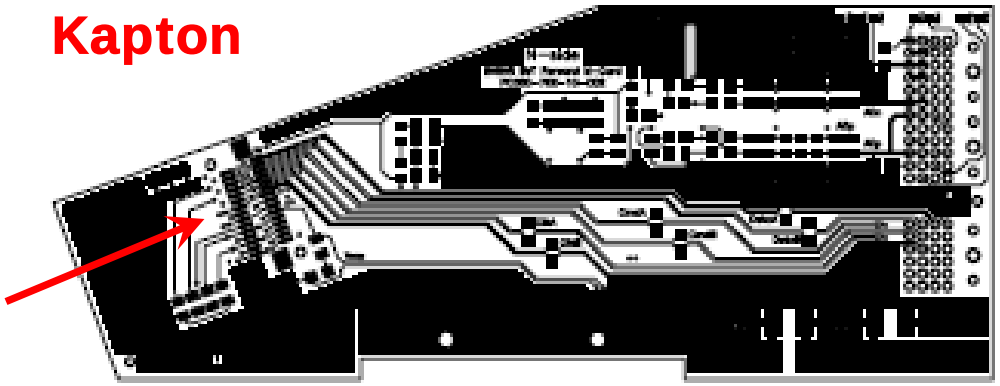
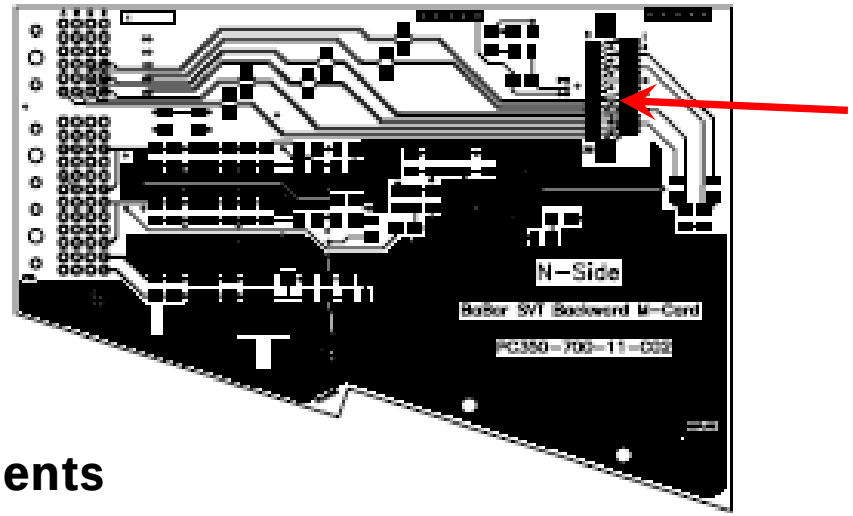


Twisted Pair cables

(24 AWG)

Kapton





Only passive components

“Patch Panel Card”

Proposal: small interconnect card very close to the Ladders (~ 40 cm)

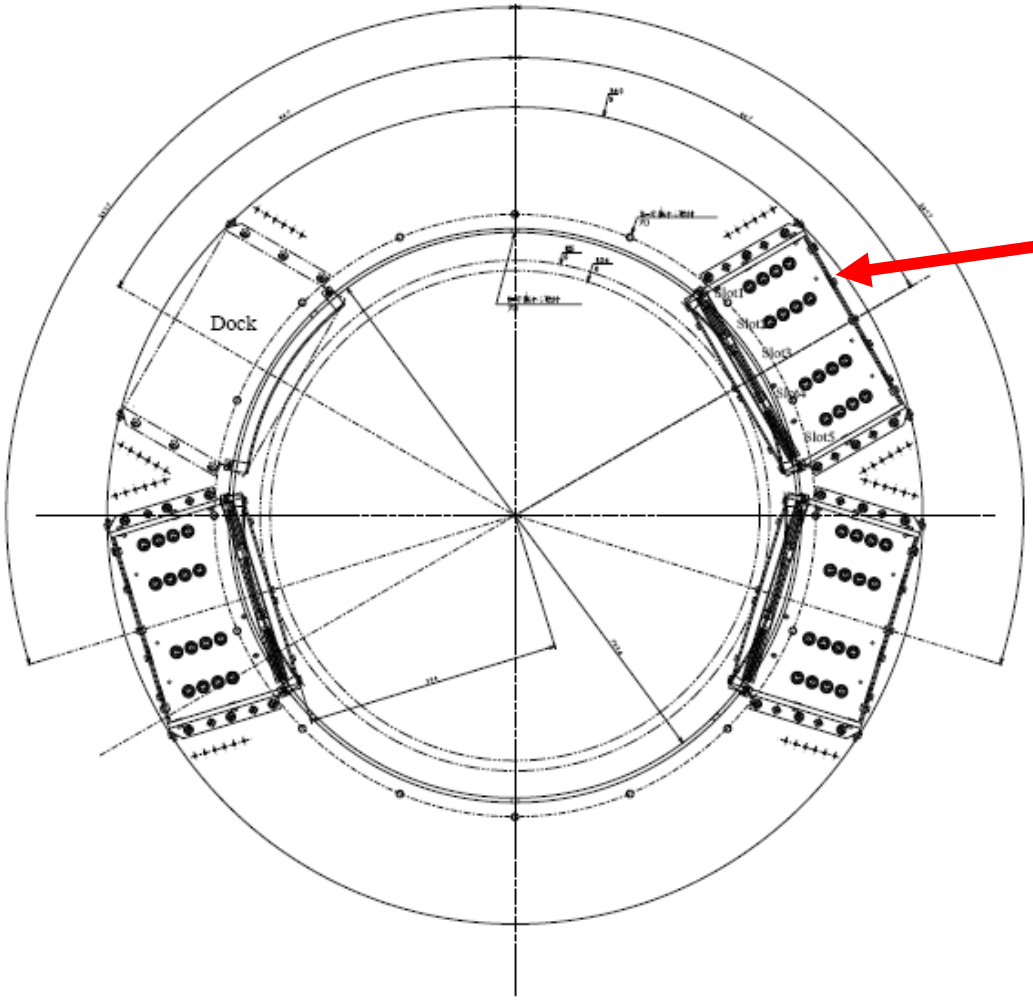
- Impedance matching (& voltage sensing ?)
- Power filtering
- Kapton ↔ cable
- Cannot be just passive, need at least line drivers and probably do optical conversion for high speed data

Finisar
FTLF8519P2BNL

- **5,66 x 1.48 x 1.243 cm^3**
- **Single power supply (3.3V)**
- **Up to 2.125 Gb/s**
- **~ 0.8 W**
- **Radiation tolerance ??**

DOCKs

Or find a way to make it to the docks...



40 x 20 x12cm (LxWxH)
Al boxes, water cooled,
overcrowded now,
at cooling limit
Only 4 ‘compartments,
on each side
Probably more needed
for the new strip det.
+ PXD !
→Request to mechanics
designers to forsee
more space

From Pablo Vazquez, Ringberg

Figure 20: Cross section of DOCK in BELLE complex at forward direction

DHH

- Small interconnect card (mounted on magnets?), rough size estimate: connector edge ~5 cm, ~ 60 cm^2, trapezoidal shape, ~ 1.5 W (if optical conversion)

  HOW MUCH SPACE AVAILABLE ?

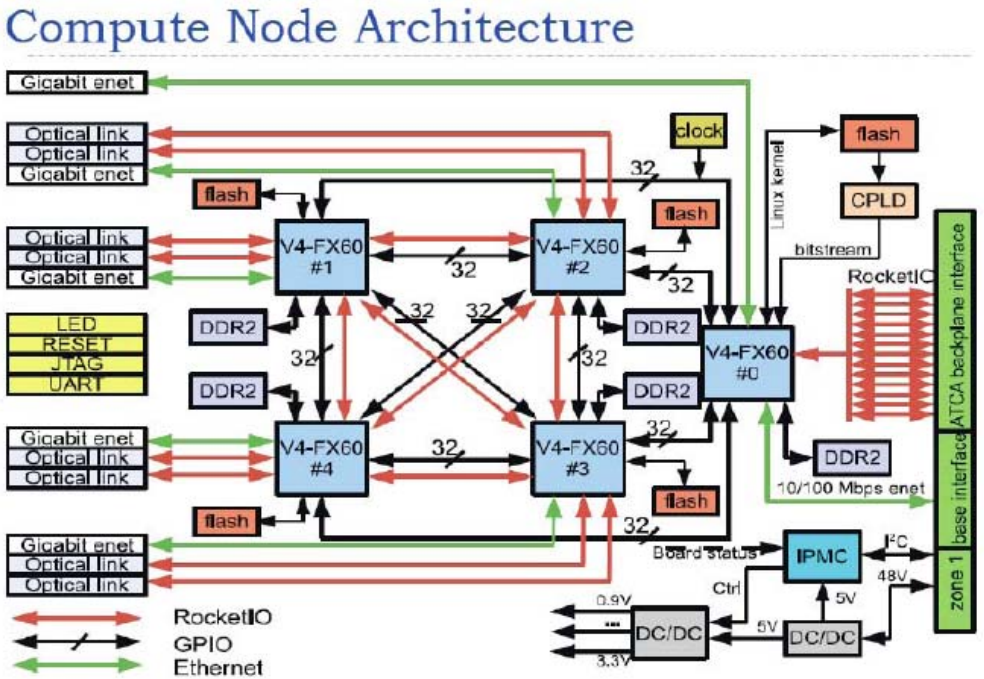
- Connects to board either outside of the detector or inside the docks containing FPGA (slow control master). Slow control system ? Sent to DAQ via optical link ?
- Power is routed from regulator boards to the small interconnect card.
- Trigger and clock do not come through optical link, but through separate cables.

DAQ Proposal

Compute Nodes

(Giessen)

5 VIRTEX4 FPGAs



ATCA System

(developed for HADES)