Data Handling Processor Slow Control

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3rd International Workshop on DEPFET
Detectors and Applications

Analog and DFT

Analog blocks

Digital To Analog Converter: 8 bits, slow (DC), 1V or 1V2 power supply, radiation tolerant.
Bandgap: 1V or 1V2 power supply, radiation tolerant.

Design For Testing

Automatic insertion of test and control logic compliant with IEEE 1149.1.

Slow Control Interface

User Data Registers connected to JTAG.

Boundary Scan

Boundary Scan Chain connected to the same JTAG.

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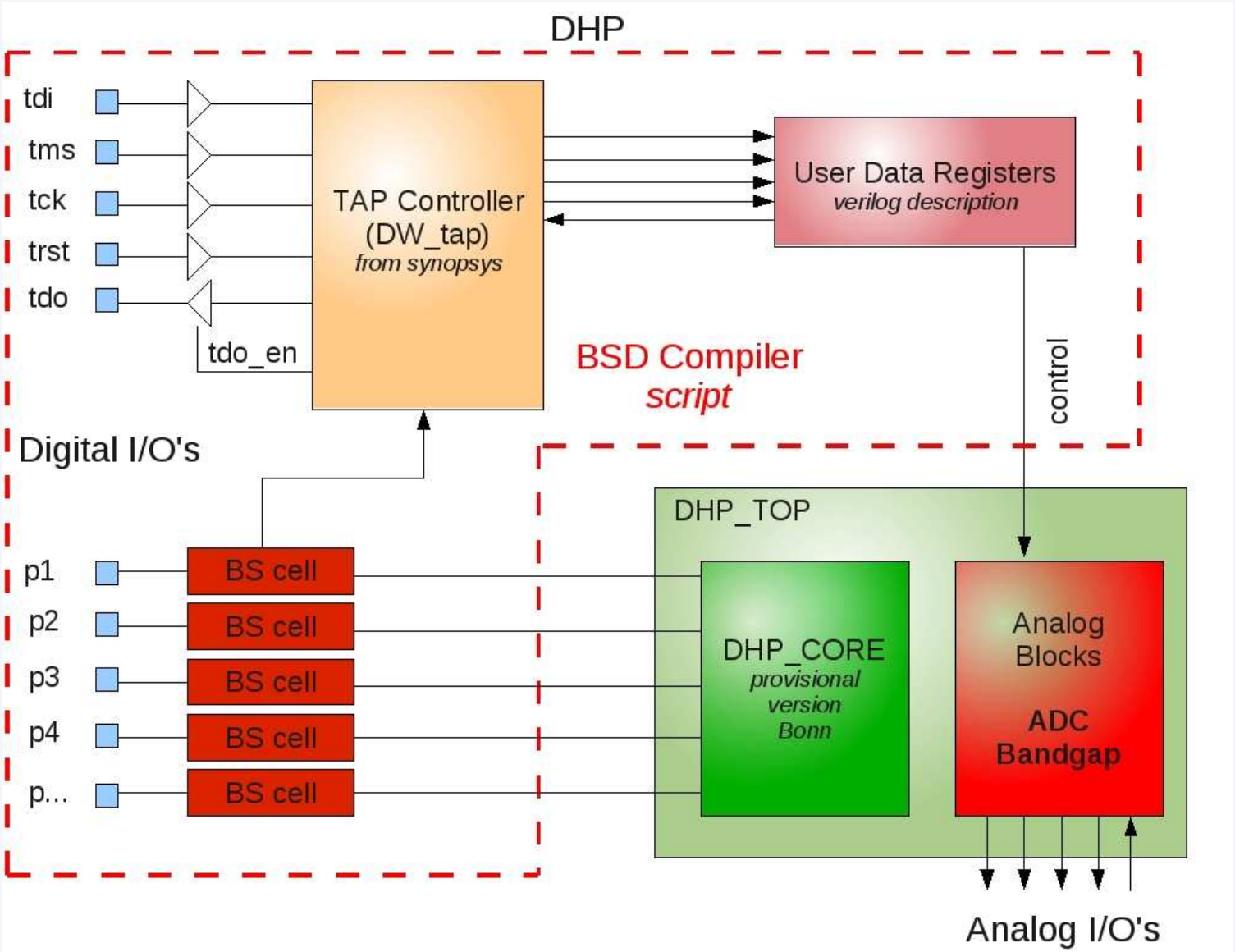
DFT on DHP


DHP
tdi
tms
tck
trst
tdo
tdo_en
TAP Controller
(DW_tap)
from synopsys
User Data Registers
verilog description
BSD Compiler
script
control
Digital I/O's
DHP_TOP
p1
p2
p3
p4
p...
BS cell
BS cell
BS cell
BS cell
BS cell
DHP_CORE
provisional
version
Bonn
Analog
Blocks
ADC
Bandgap
Analog I/O's

DFT Design Flow

Read RTL Netlist *(hdl file)*

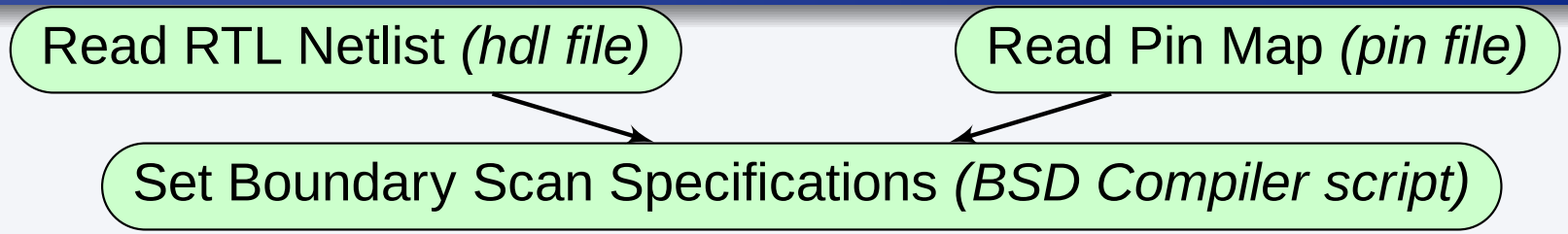
Read Pin Map *(pin file)*

User input

Design Vision operation

Design Vision output

DFT Design Flow



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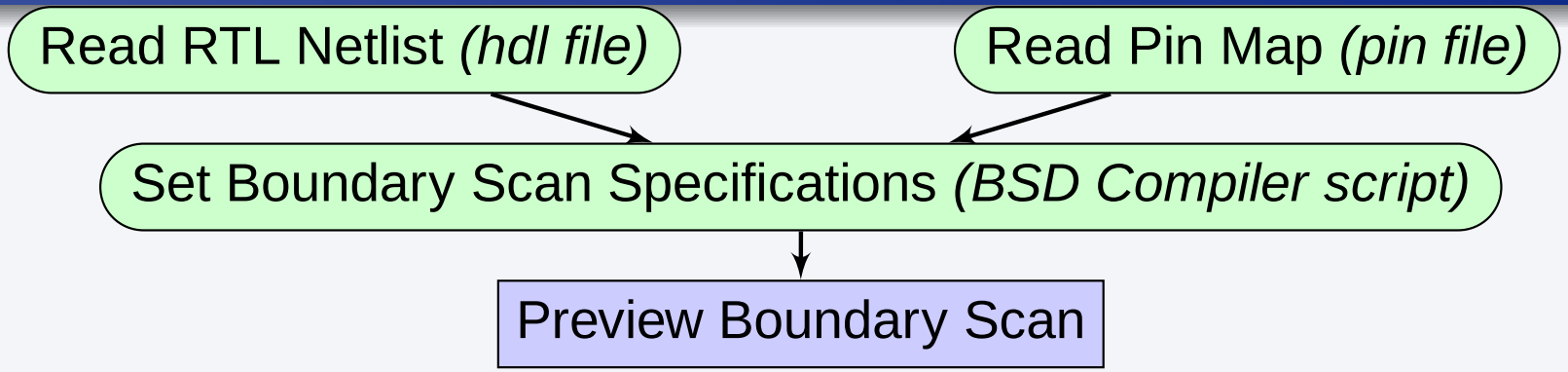
DFT Design Flow

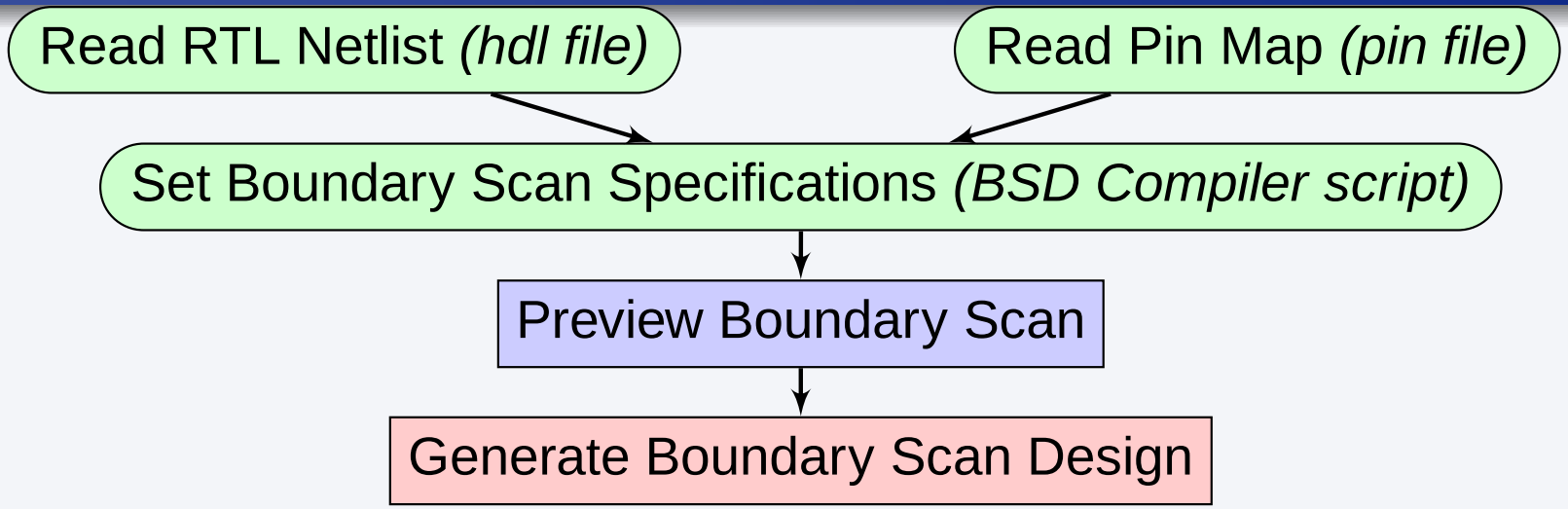


User input

Design Vision operation

Design Vision output

DFT Design Flow

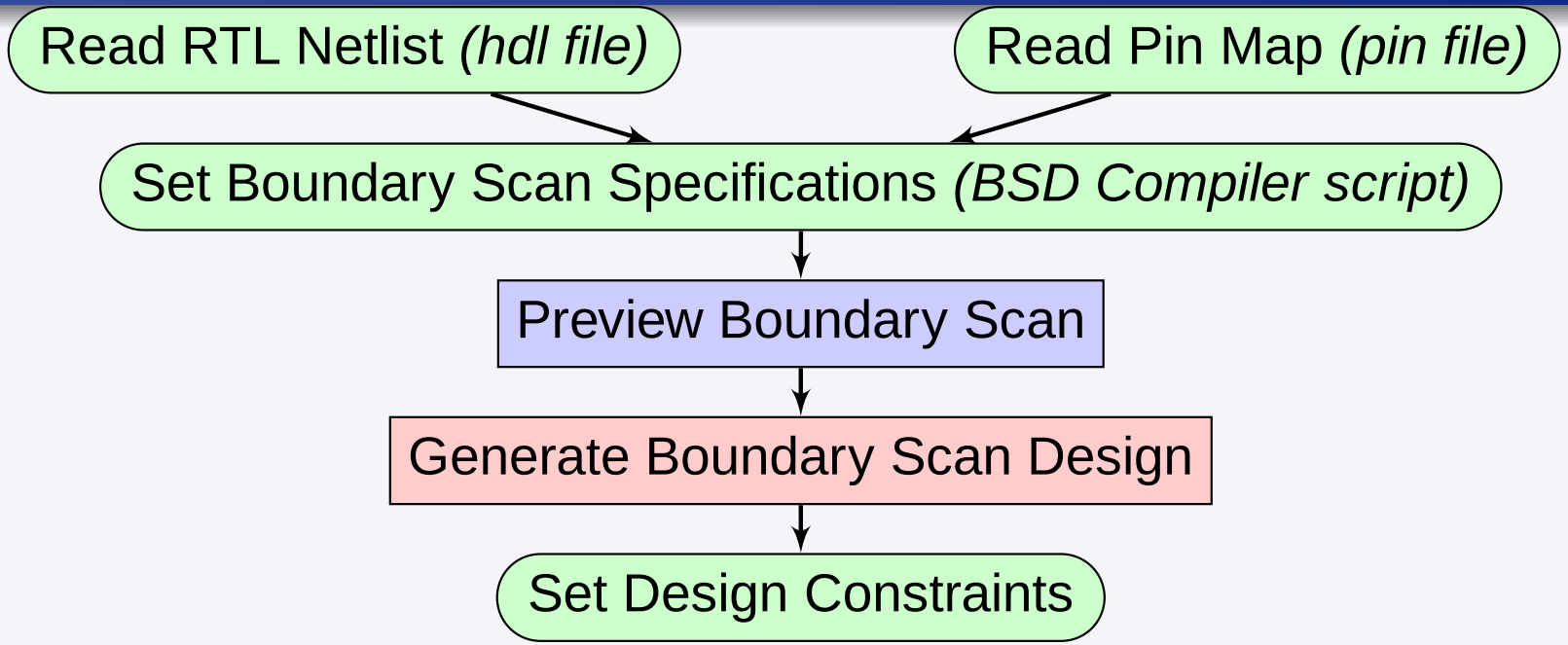


User input

Design Vision operation

Design Vision output

DFT Design Flow



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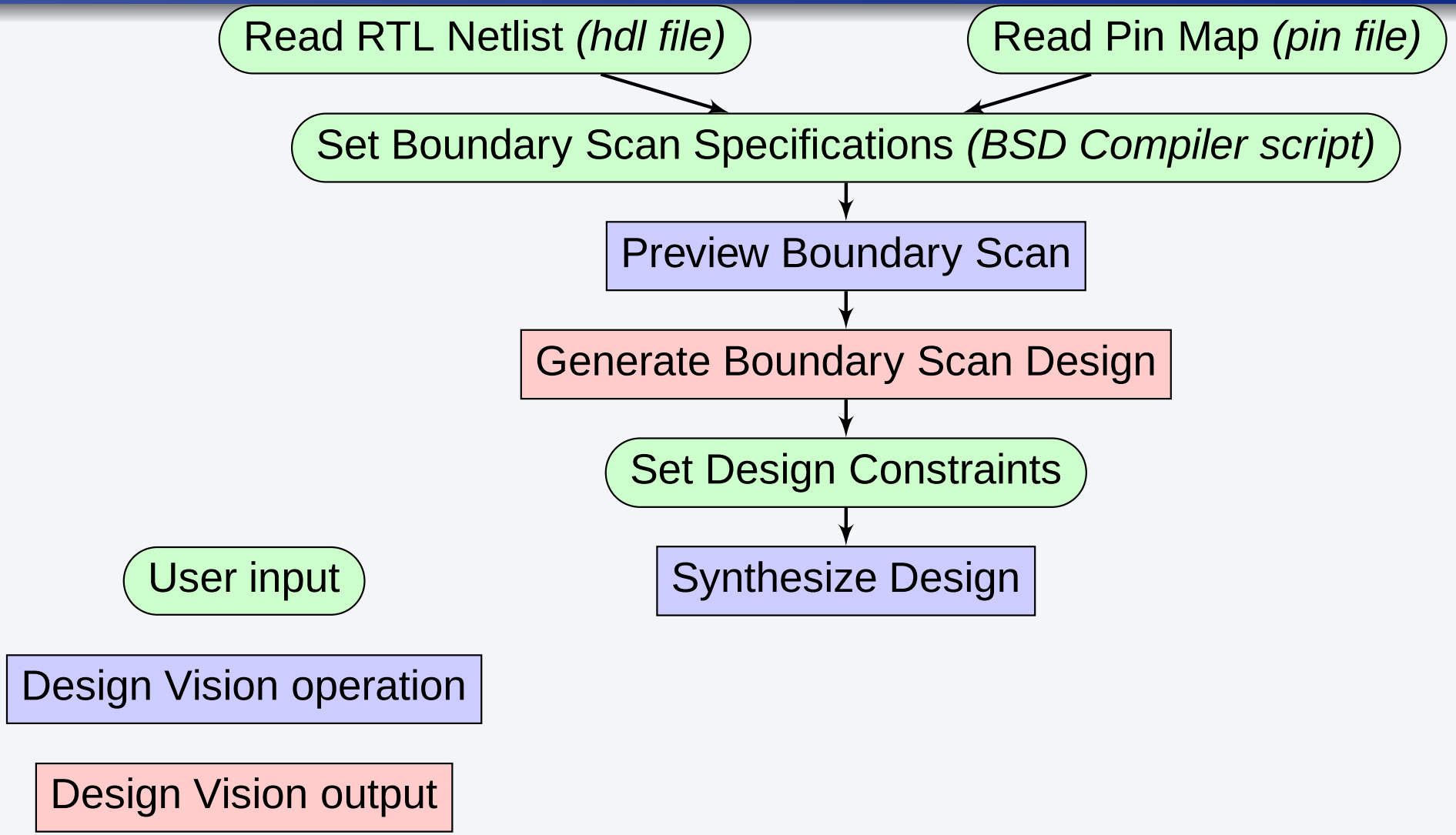
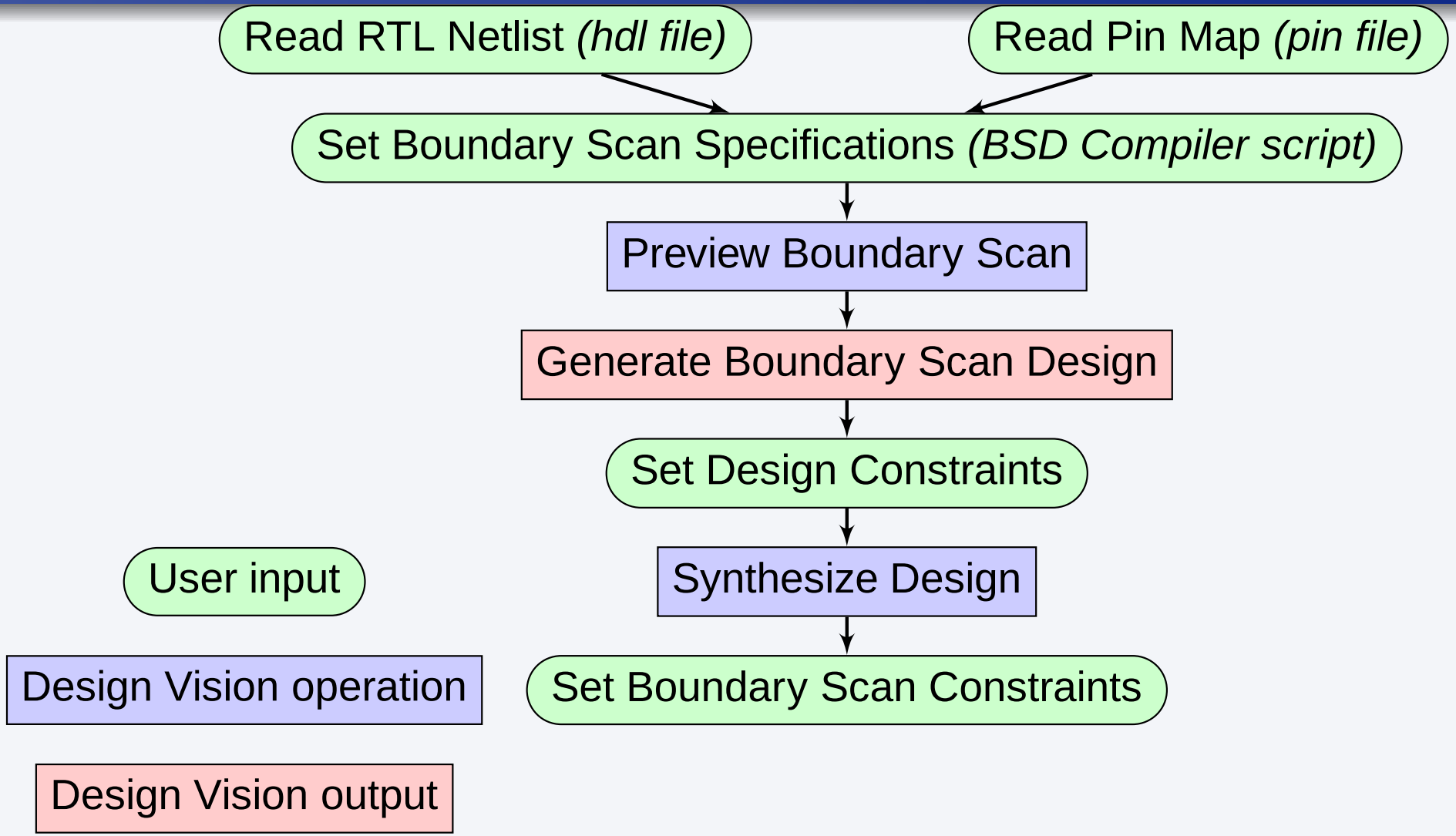
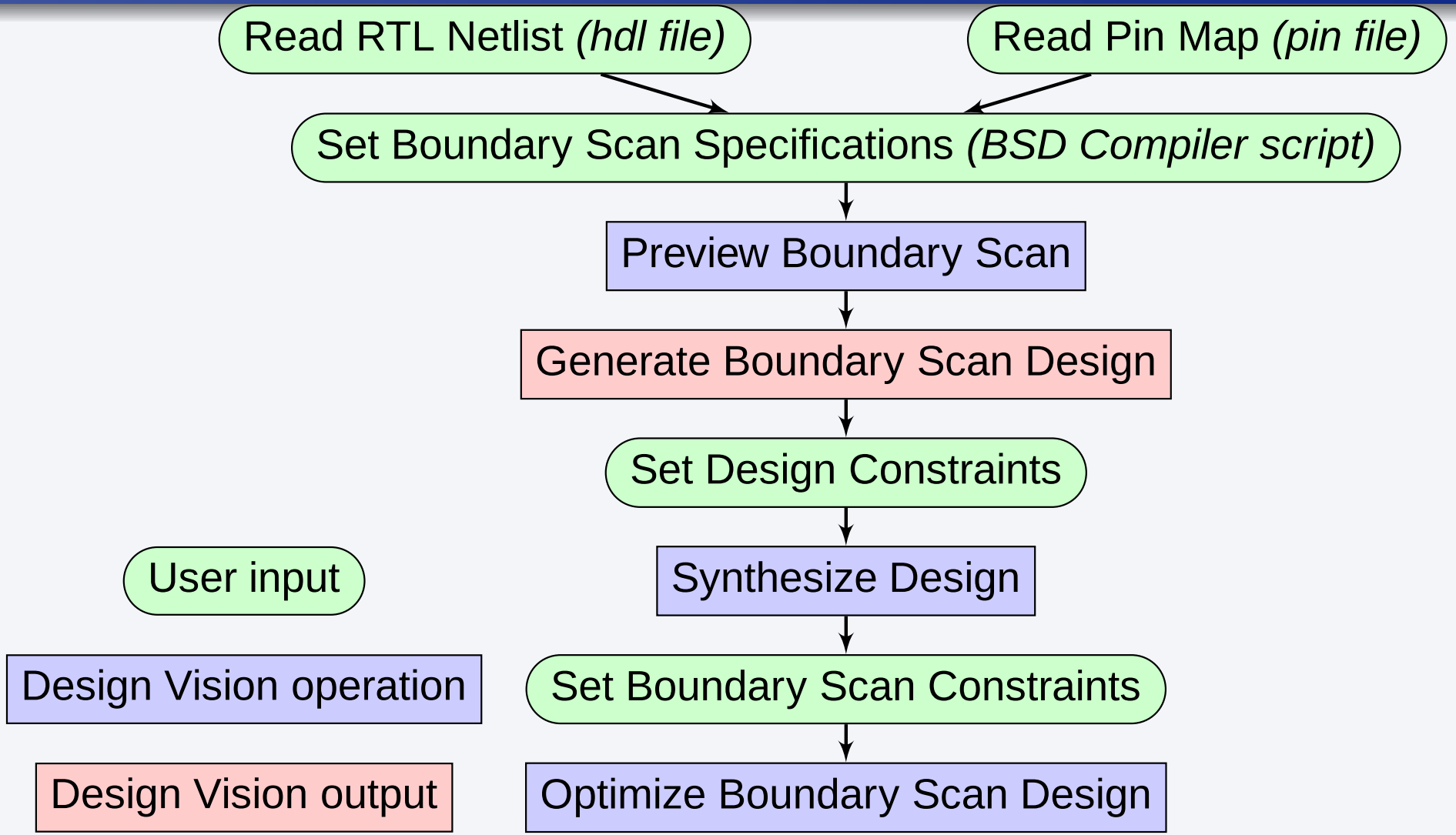
DFT Design Flow



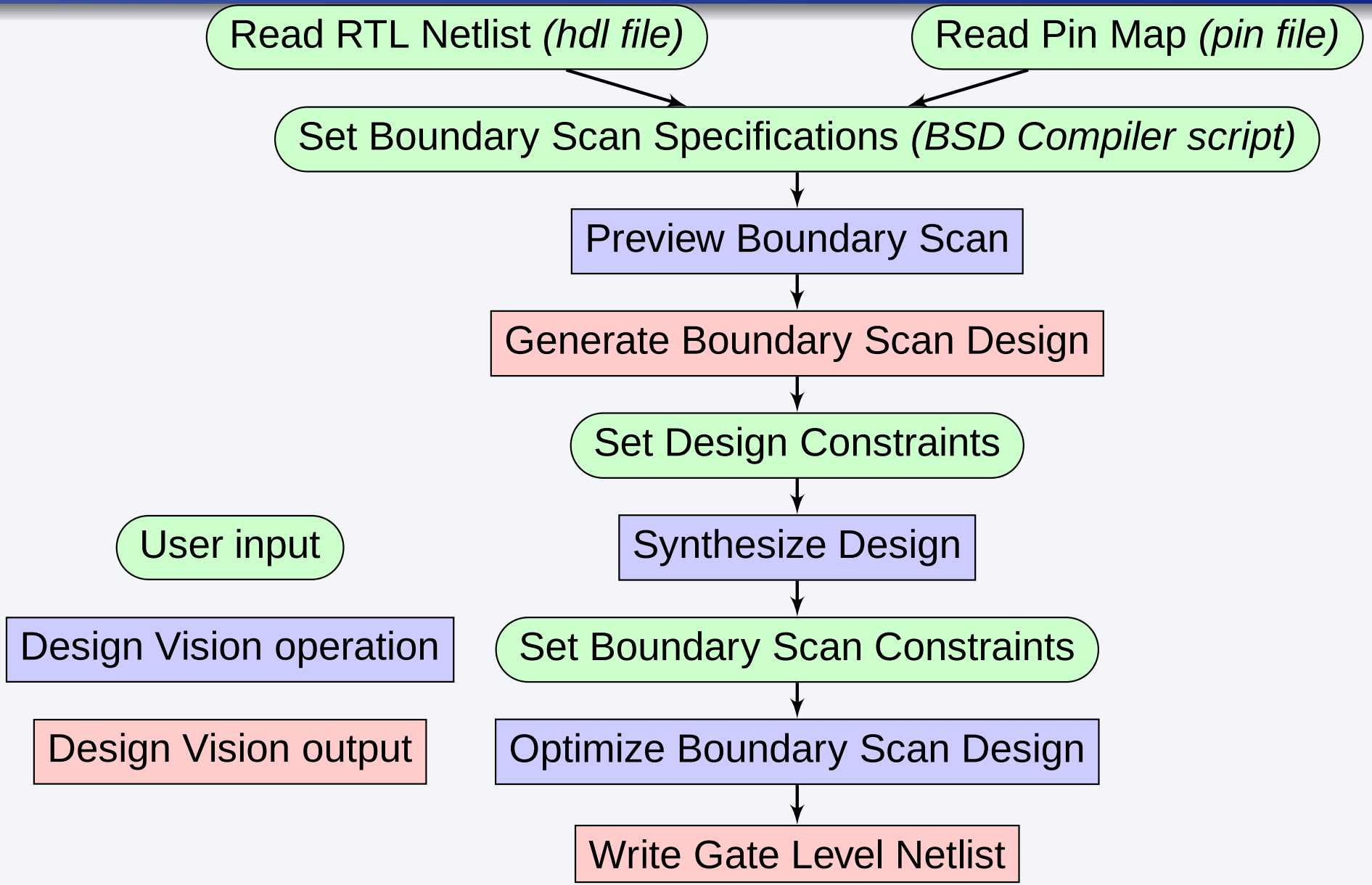
DFT Design Flow



DFT Design Flow



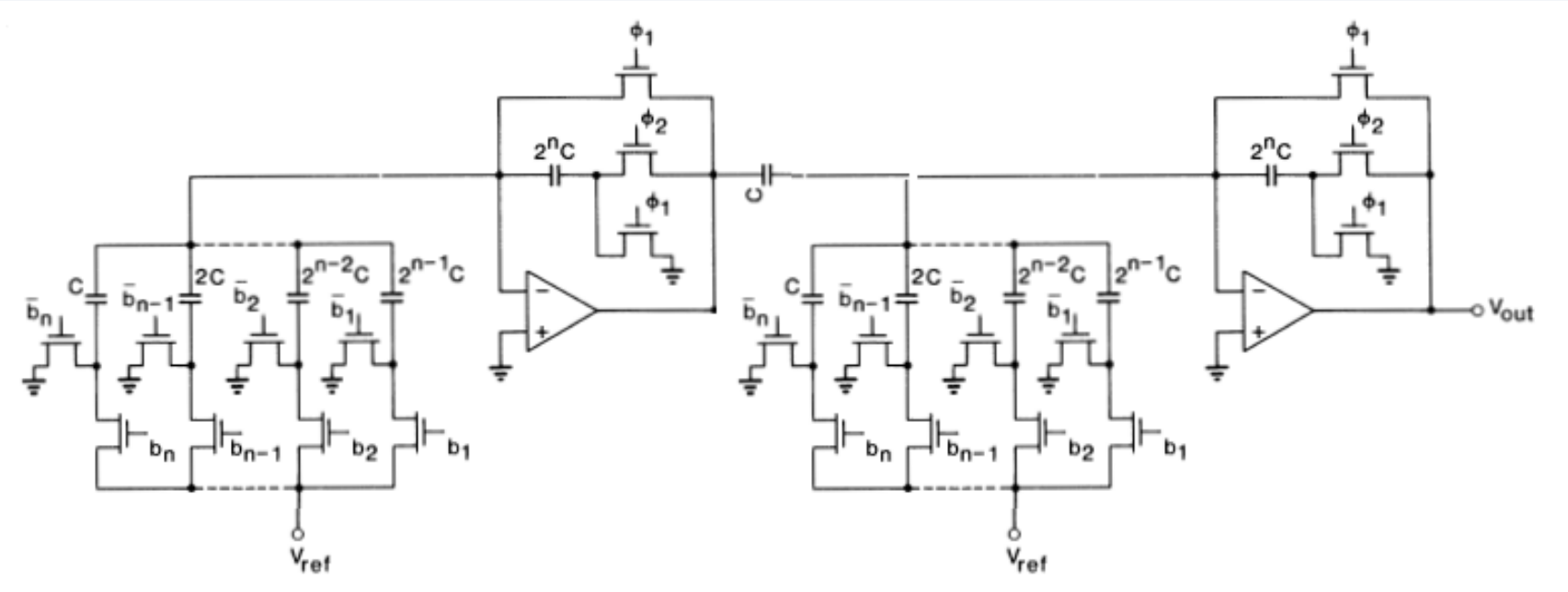
DFT Design Flow



DAC

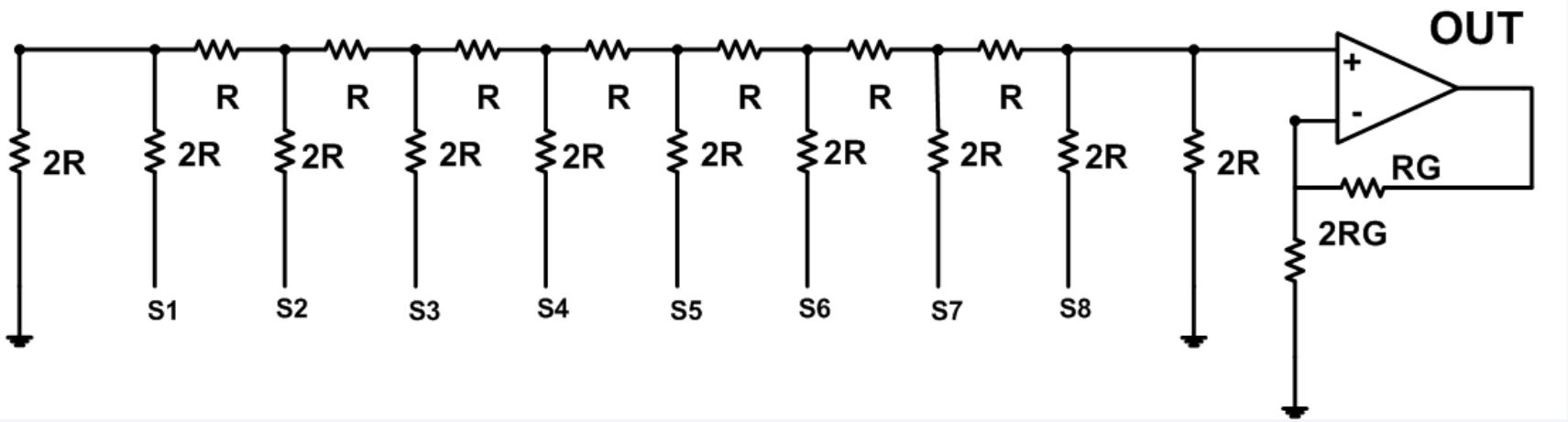
Capacitive DAC

- A charge mode DAC or Switched capacitor has some advantages:
  - Low power consumption.
  - Small area needed.
  - Radiation tolerant.
  - But has an important drawback; **the leakage in the switch** which makes it unusable for a slow DAC.



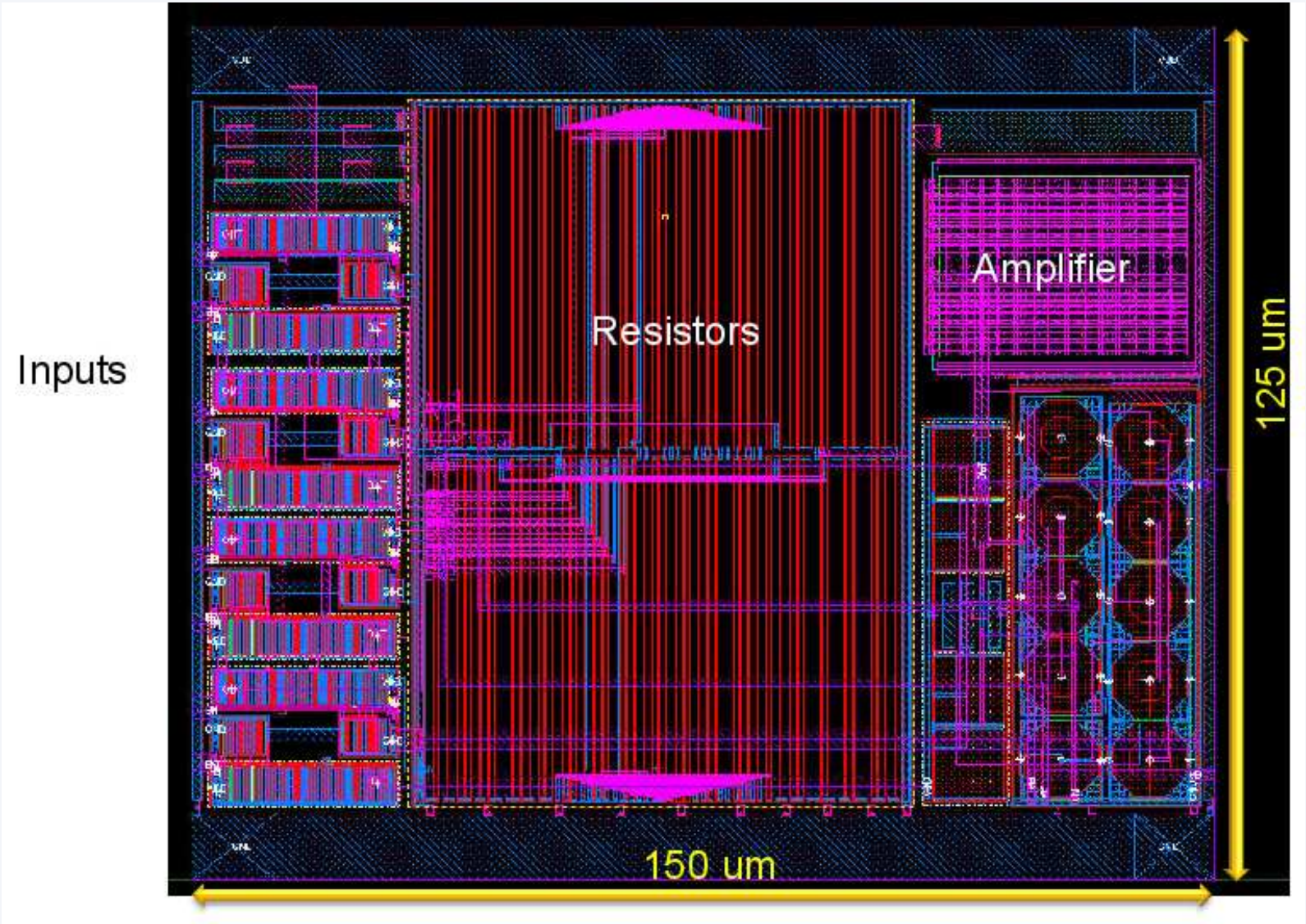
R-2R DAC

- Compared to a Switched capacitor DAC has some disadvantages:
  - More power consumption.
  - More area needed.
  - Less precision.
  - But **it can be used in DC**.

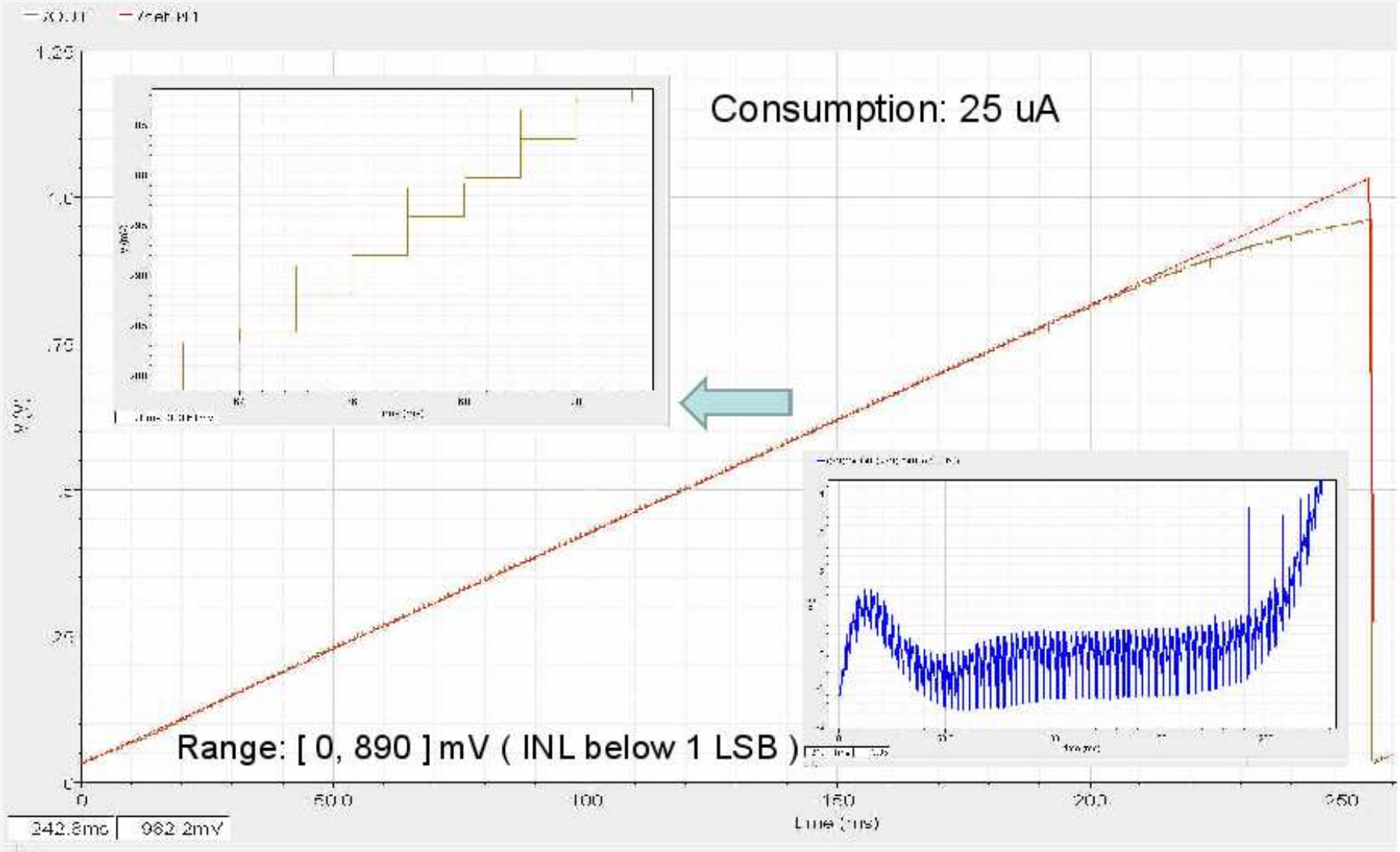


R = 80kΩ

Layout

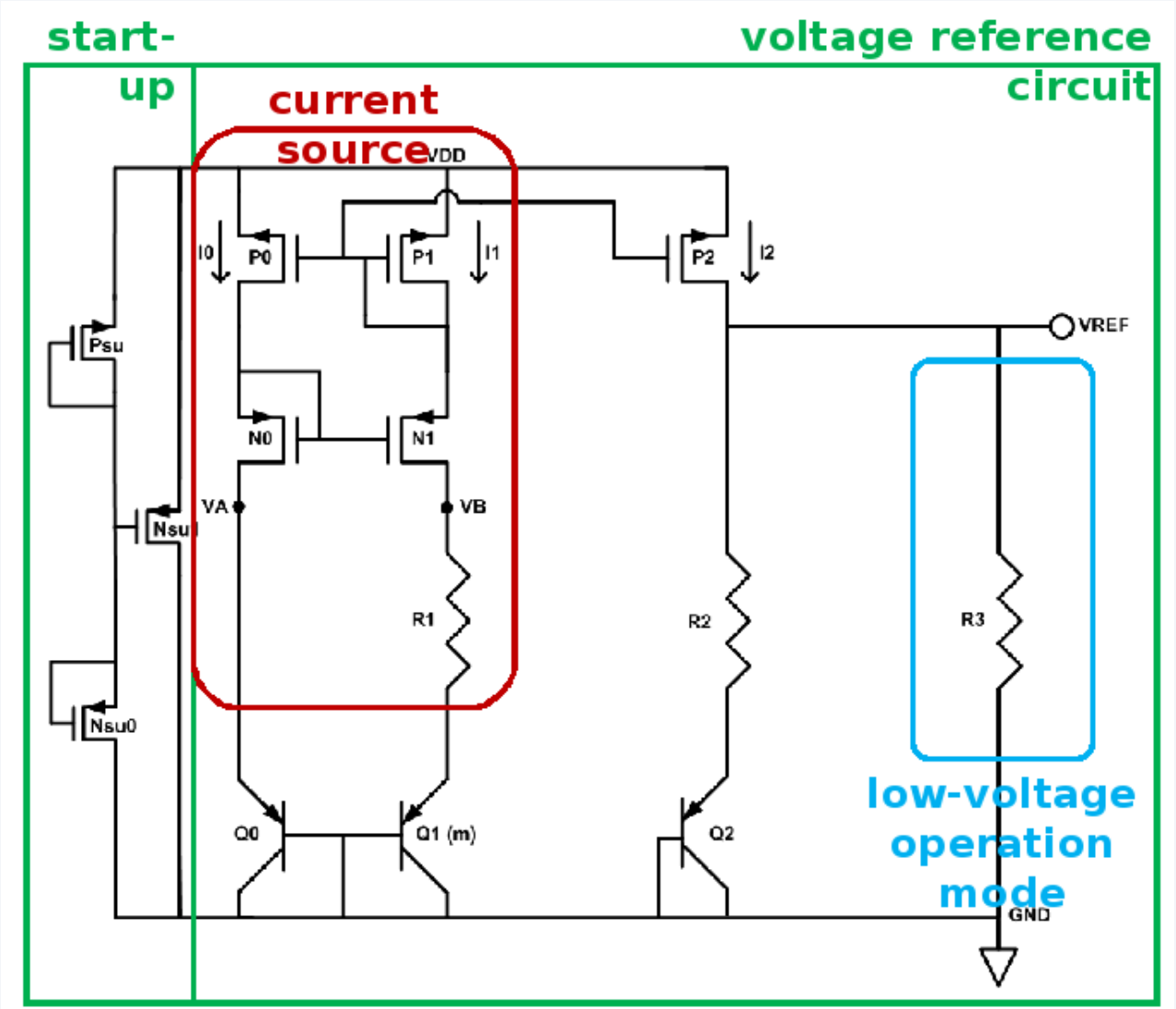


Simulations

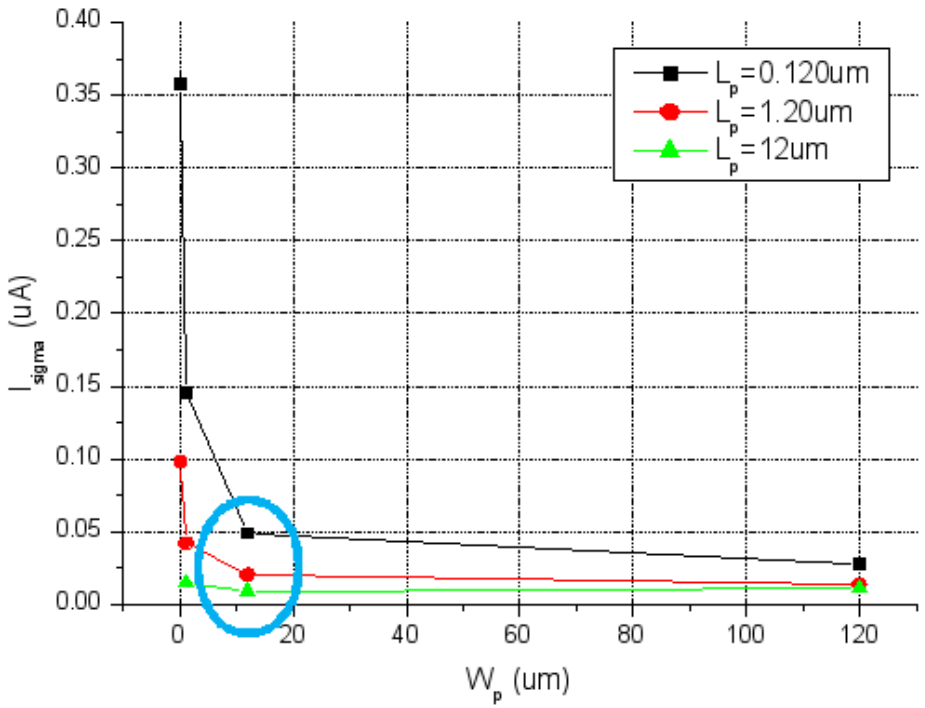


Bandgap

Proposed circuit

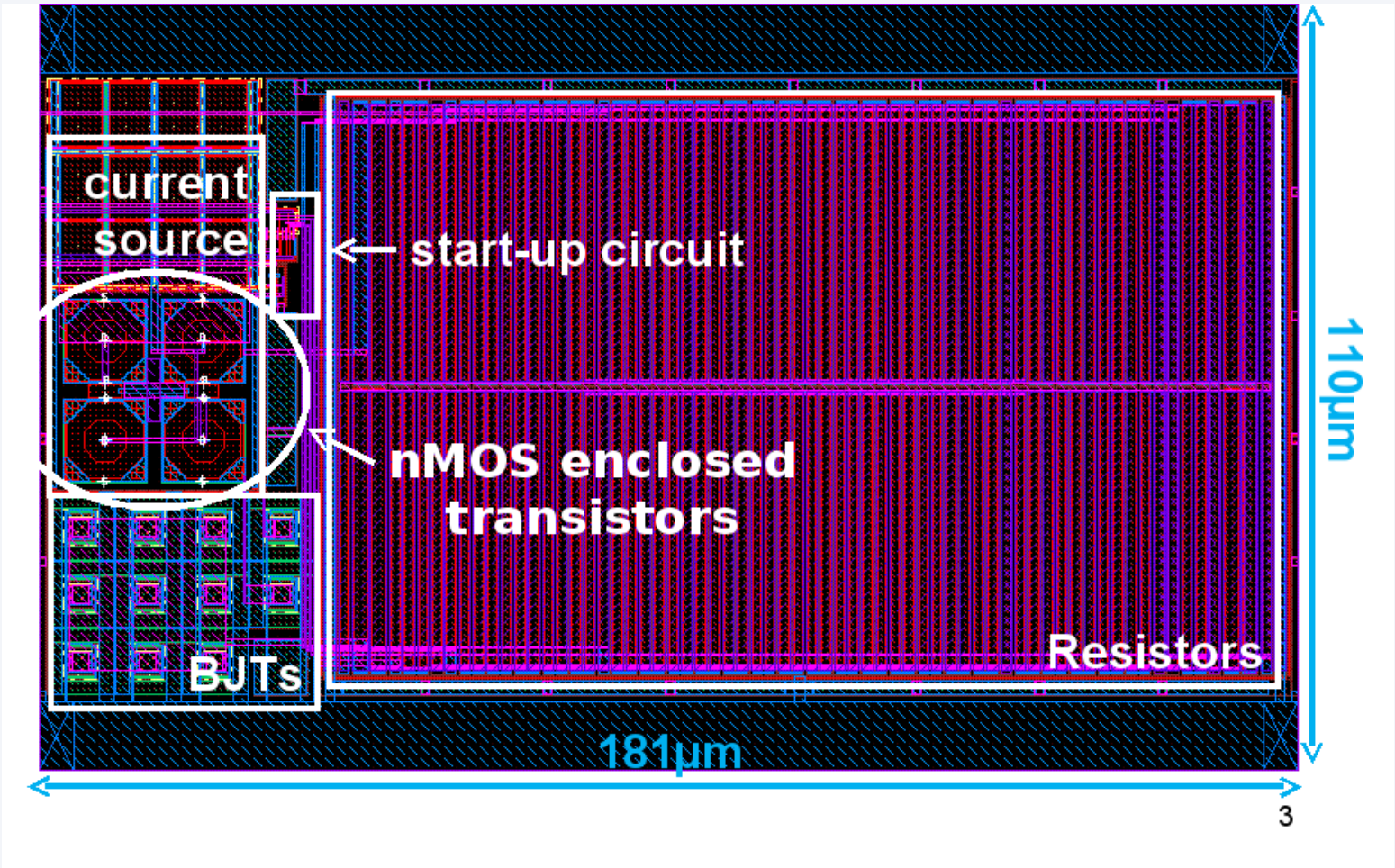


Design stage



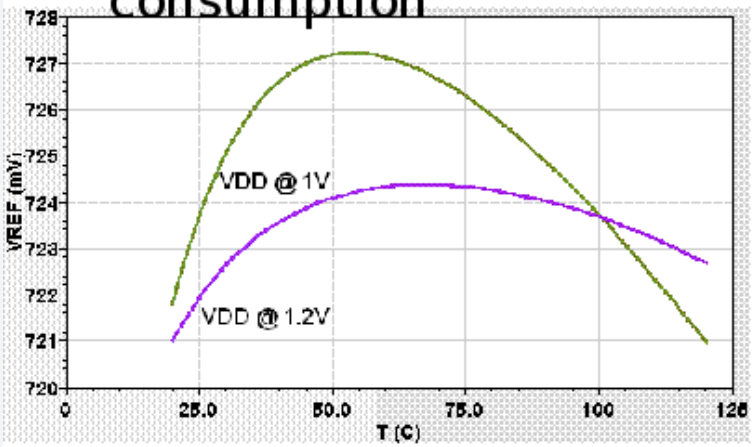
Pre-design **Monte Carlo simulations** show a major stability when **MOS transistors**' dimensions are kept a few **µm** large

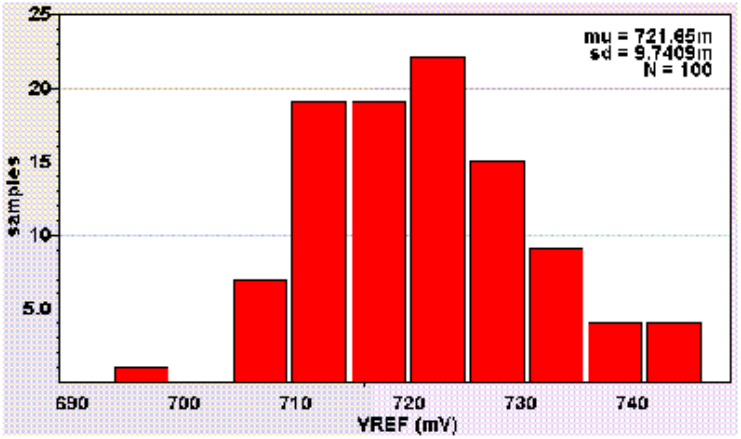
Layout


current source
start-up circuit
nMOS enclosed transistors
Resistors
BJTs
110µm
181µm
3

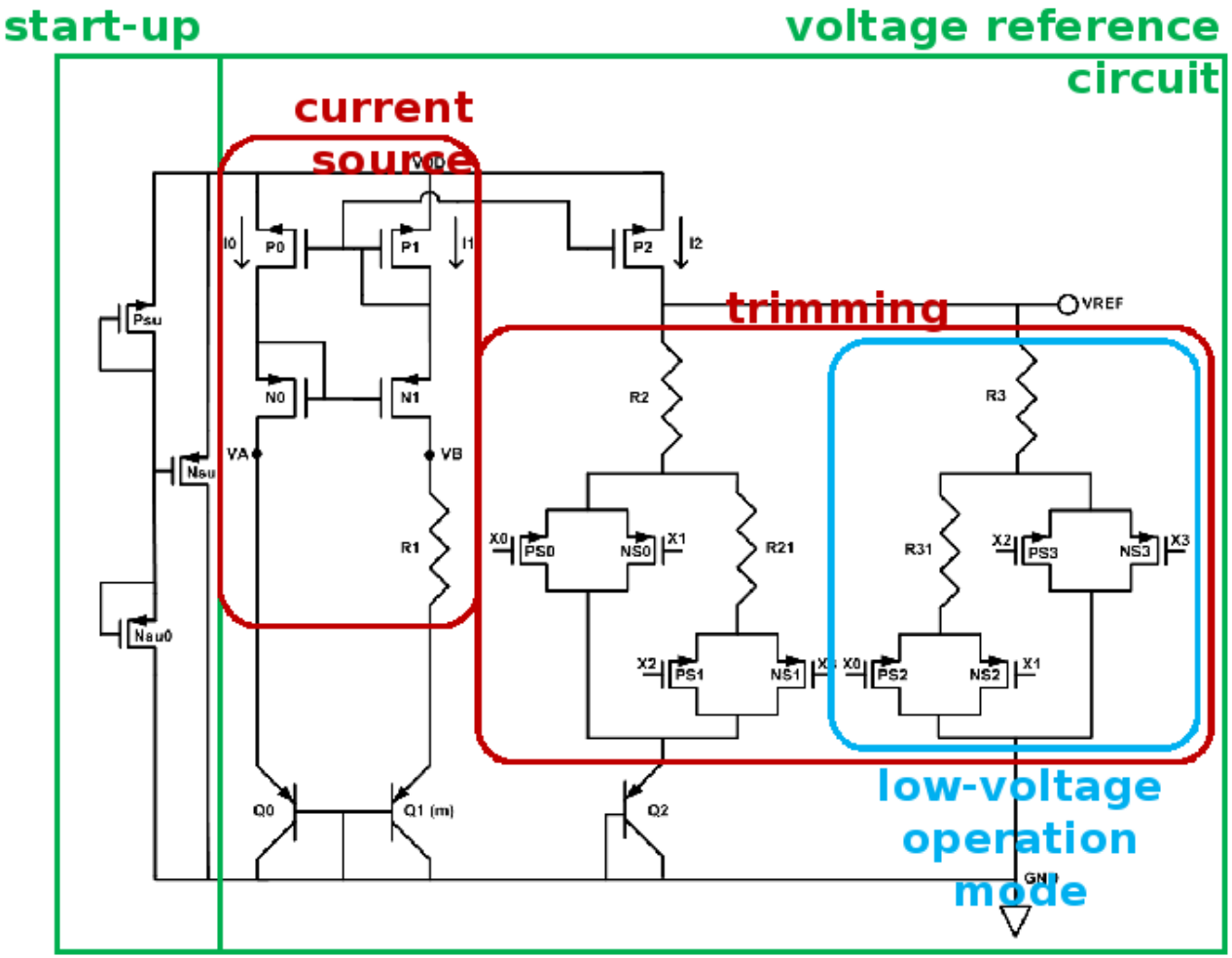
Results

Parameter	V_{DD}=1V	V_{DD}=1.2V	Unit
Temp. Range	20 → 120	20 → 120	ºC
V_{REF} @ 27ºC	724.3	722.3	mV
Max. ΔV_{REF}	6.2	3	mV
Monte Carlo mean	724.4	721.65	mV
Monte Carlo sigma	10.15	9.74	mV
Power consumption	18.70	55.18	µA





Final circuit



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Next steps

Next steps

1. Finish current chip design in **Bonn** during week 12-16th october.
2. Analog blocks left:
   Slow **Analog to Digital Converter** 10bits.
   Analog mux for multiplexing ADC input.
   High speed RX PAD 400MHz 1.8V HSTL compliant for data input from DCD.
3. Digital: add ADC and MUX control registers.
4. Test current prototype analog and digital blocks.

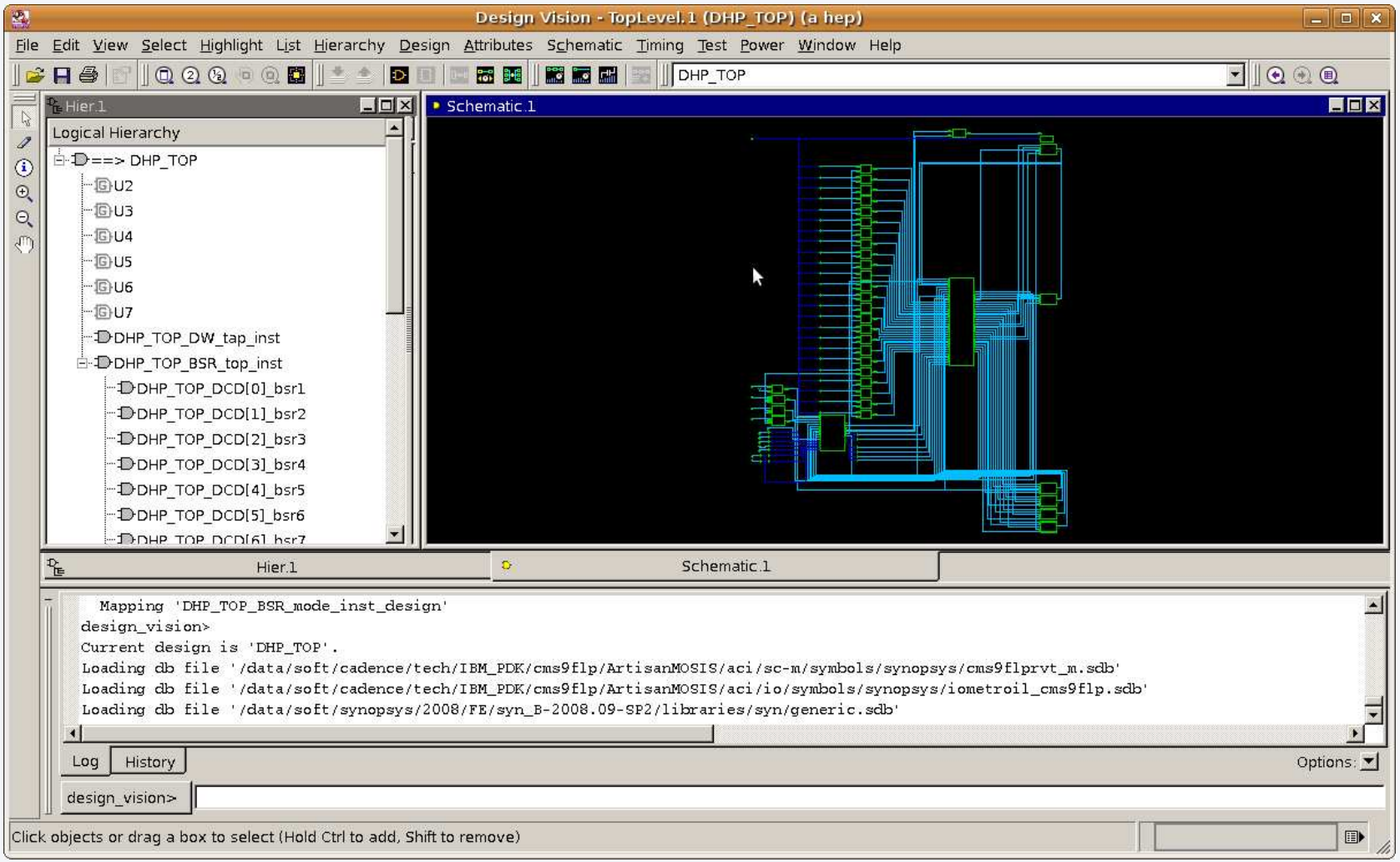
Questions?

End

More...

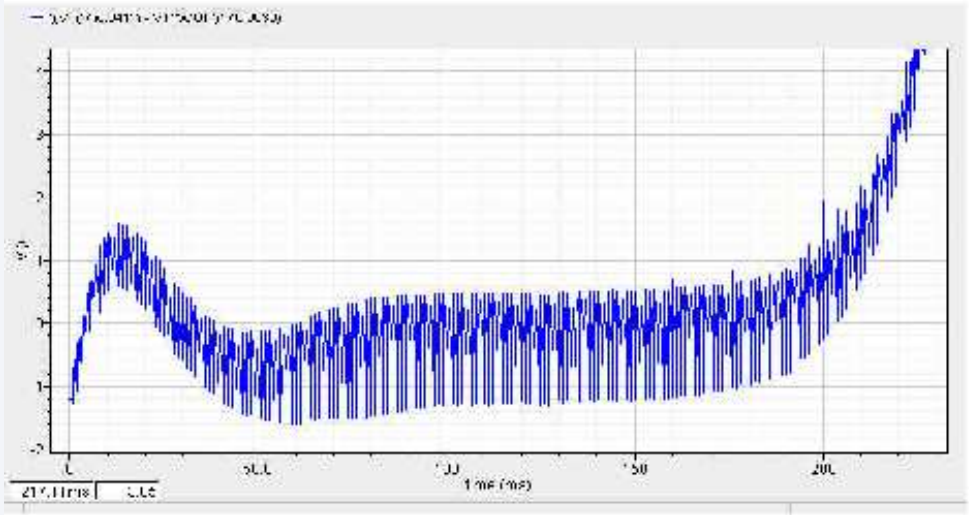
Extra slides

Design Vision



DAC R-2R

- Range: [0, 890] mV (INL below 1 LSB)
- Area: 150 um x 125 um
- Consumption: 25 uA.
- Value of R: 80KΩ
- We can use in the ADC.
- Matching techniques.



T	W	L
2*T0 Nmos	25u	5u
4*T1 Nmos	10u	5u
4*T2 Nmos	10u	5u
2*T3 Nmos	25n	5u
2*T4 Pmos	10u	10u
2*T6 Pmos	10u	10u
T7 Pmos	500n	5u
T8 Pmos	500n	5u
2*T9 Nmos	25u	5u
Mimcap	100u	10u