DCD2 test system and results
(DEPFET matrix measurements)

Barcelona 10/2009

Manuel Koch

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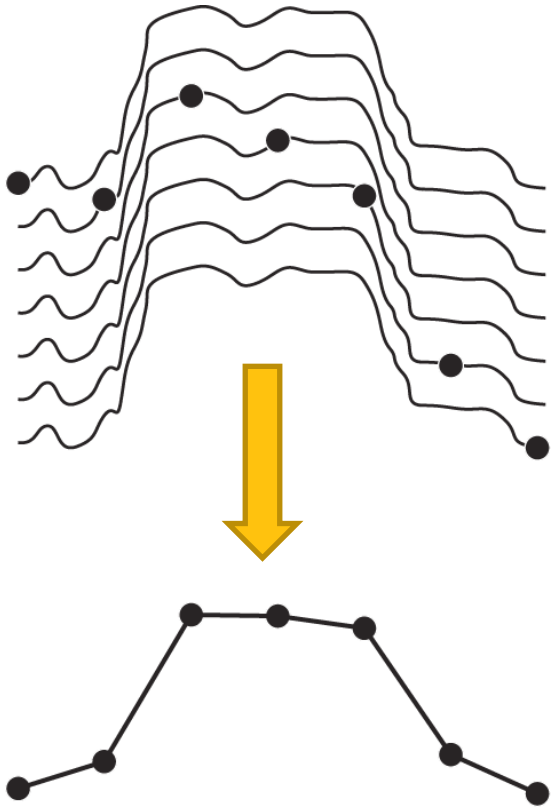
time resolved measurements with the DCD

- DCD can take **one** sample per T_{row}
- use **sequential sampling:**
  - **One sample** is taken from each of a number of similar waveforms.
    - or average over more samples
  - time shift the sampling point
  - The samples are **assembled** to form a composite waveform.
- requires periodic and stable input signals
- current implementation allows 96 samples per T_{row}
- time resolution depends on DCD speed
  - eg. T_{row} = 1500ns : steps of 15.6ns
  - eg. T_{row} = 96ns : steps of 1.0ns
- this technique is used for
  - rise time measurements
  - time resolved DEPFET current output
  - investigation / setting of optimal sampling points
  - …



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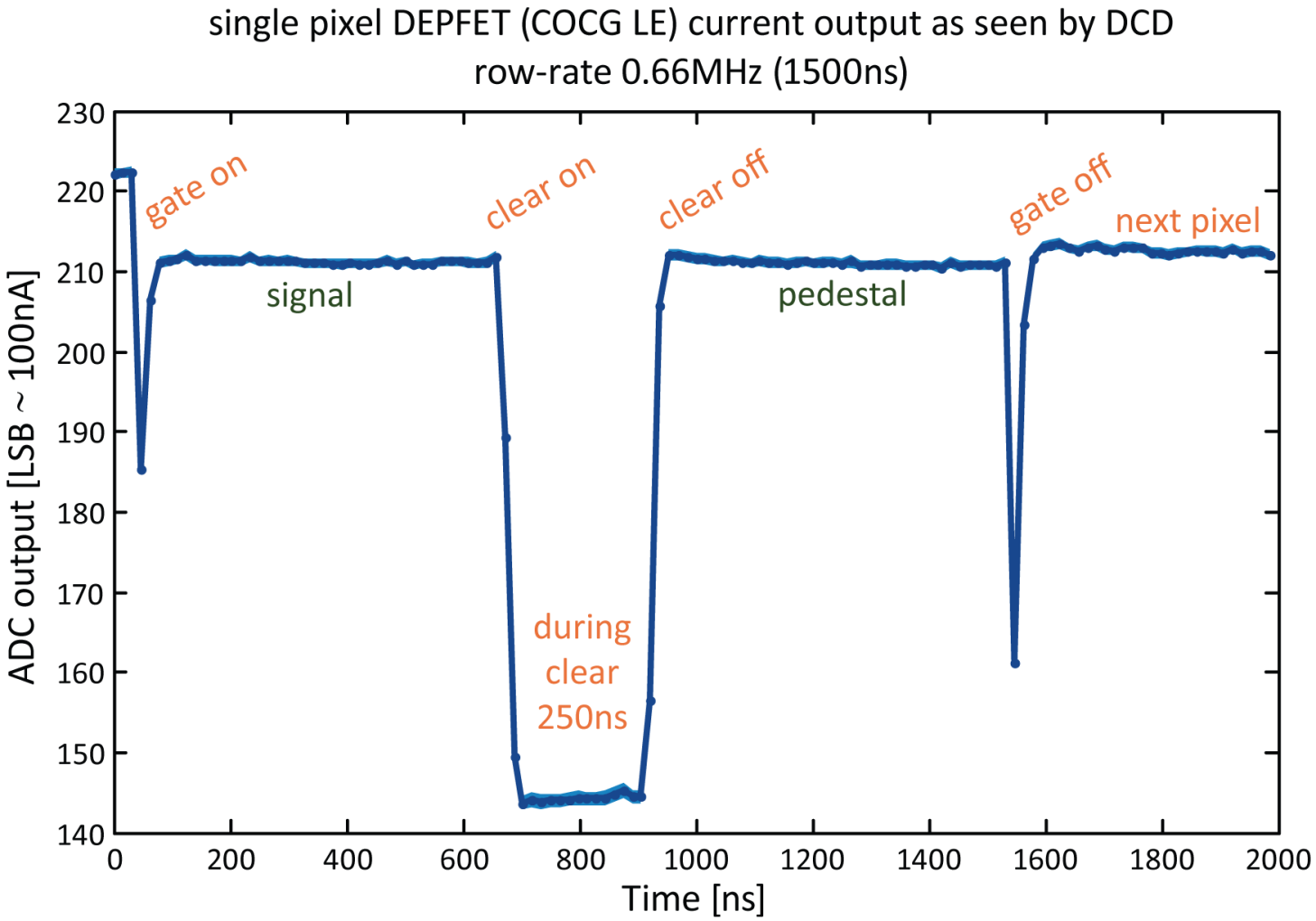
Time resolved DEPFET output current (very slow)



- Row-time divided in 96 steps
- each point sampled 1000 times, then averaged

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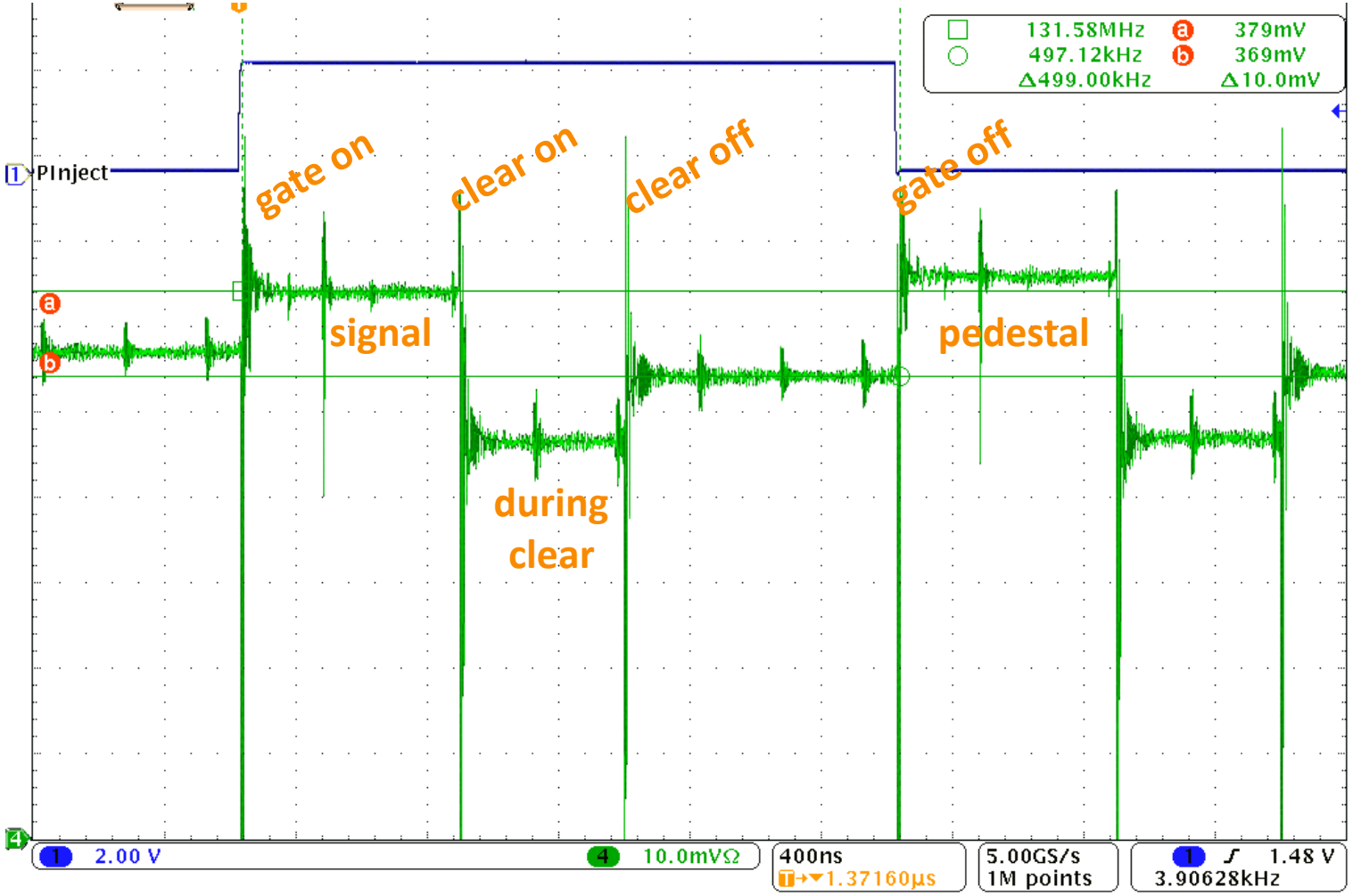
Direct TIA output of DEPFET @500kHz row-rate



- note: crosstalk due to DCD internal CK; switcher CK falling edge
- advise to put switcher falling edge CK within clear period
- TIA: AD8015 chip, same as on S3B

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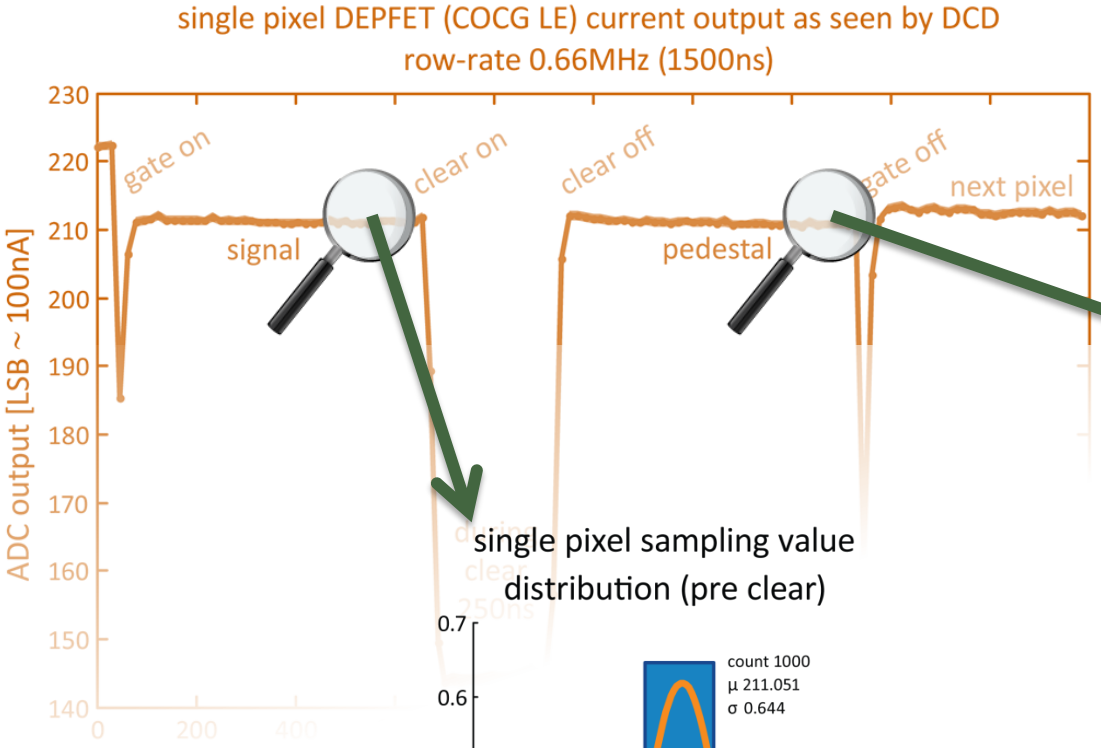
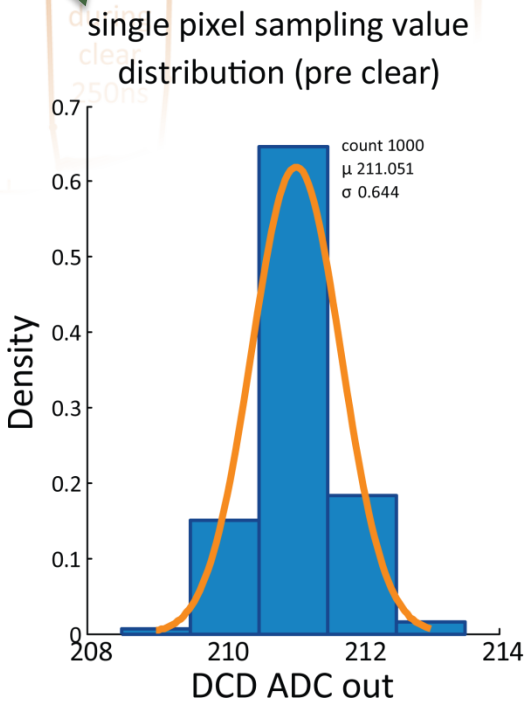
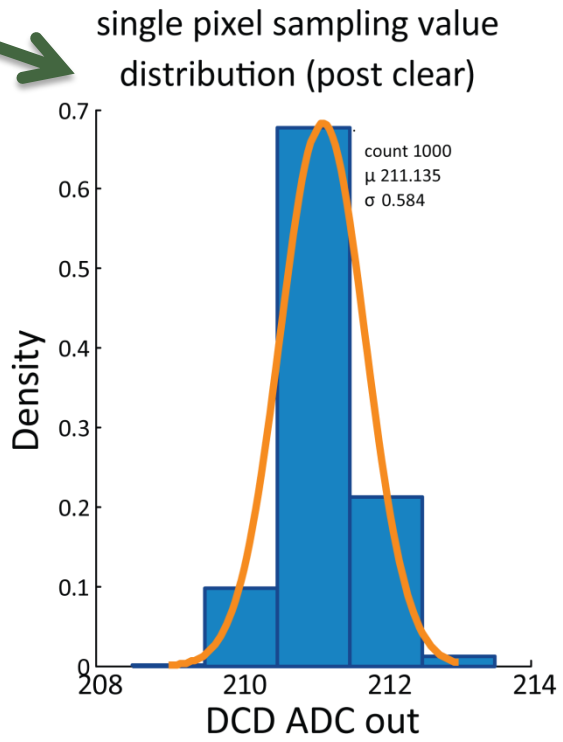
Time resolved DEPFET output current – statistics



single pixel value distribution
- slow readout -





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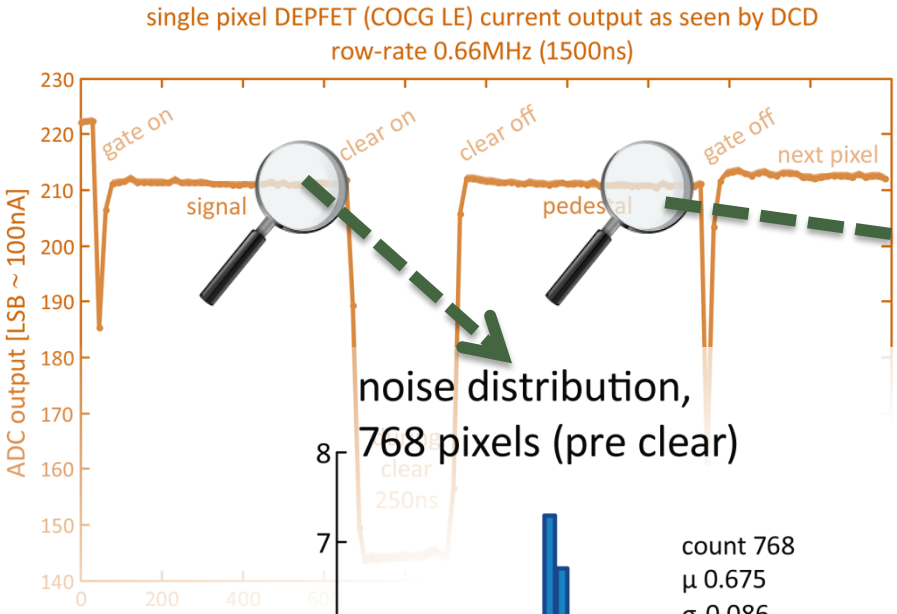
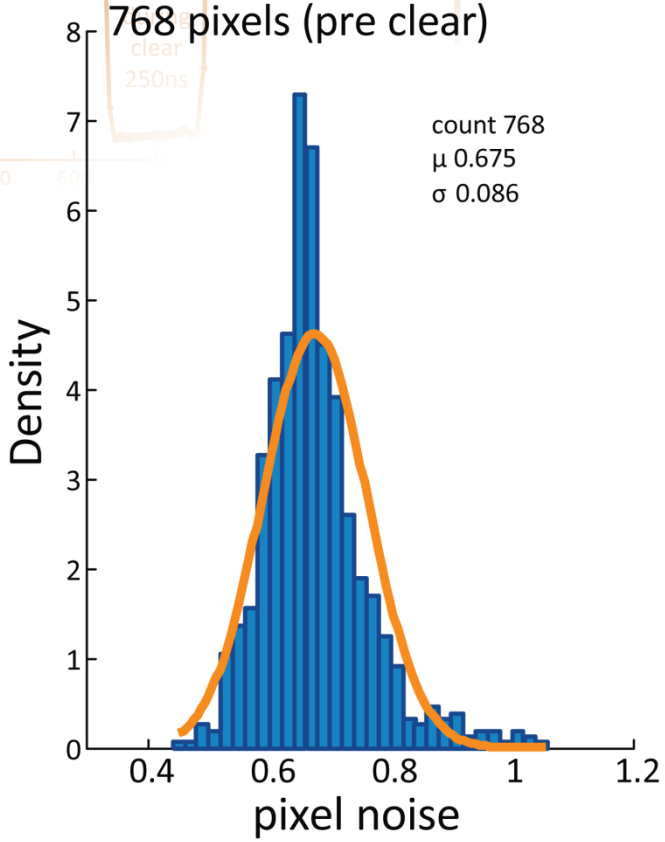
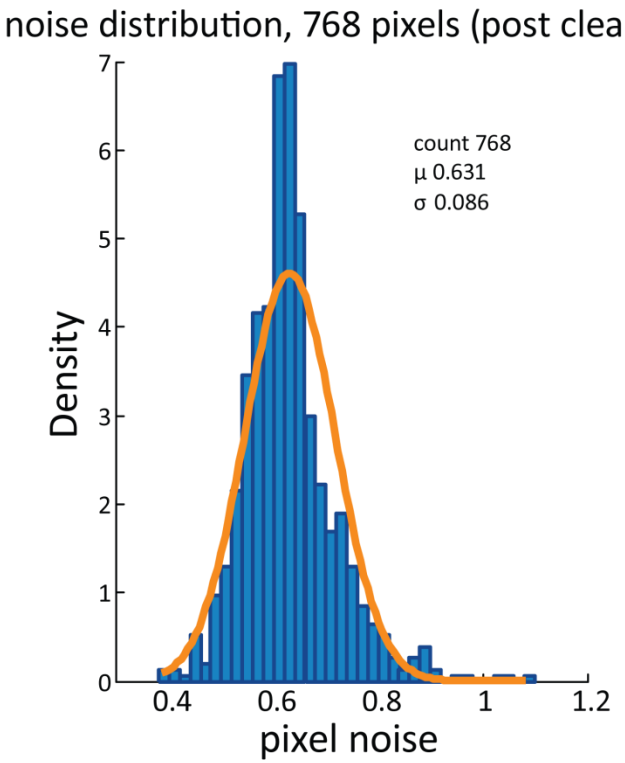
Time resolved DEPFET output current – statistics





768 pixels noise distribution
- slow readout -



no significant change even during
6h run with 6M samples per pixel
(excluding warm-up)

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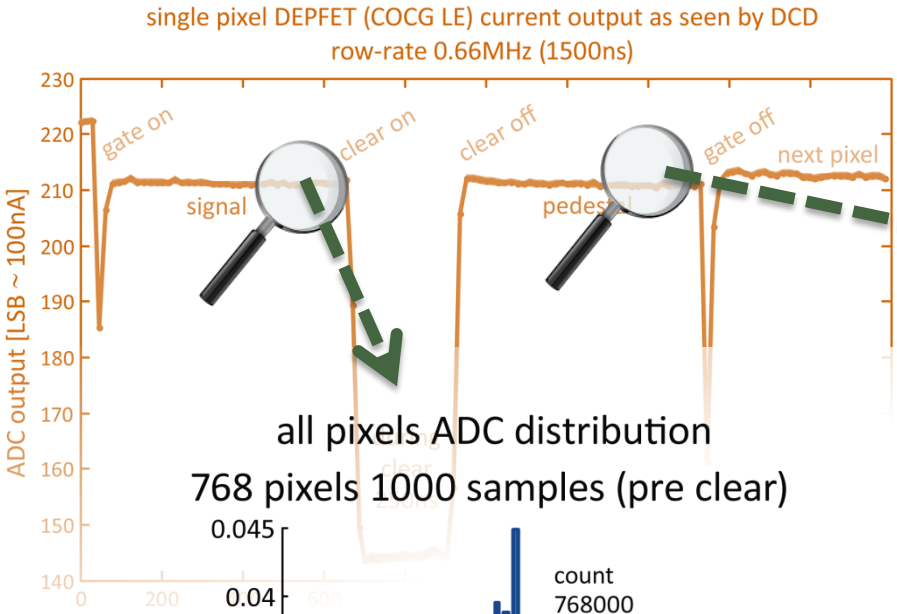
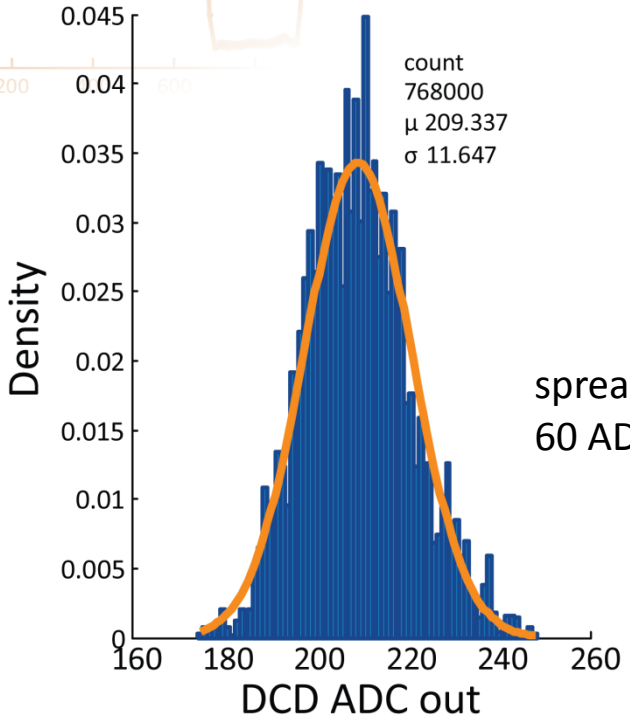
Time resolved DEPFET output current – statistics



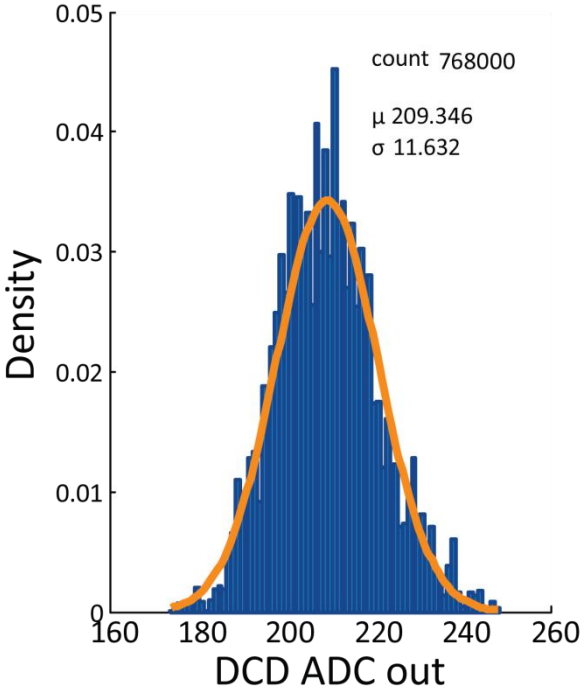
all pixels ADC distribution
768 pixels 1000 samples (pre clear)



spread is rather large!
60 ADC ≈ 6μA

768 pixels signal distribution
- slow readout -

all pixels ADC distribution
768 pixels 1000 samples (post clear)



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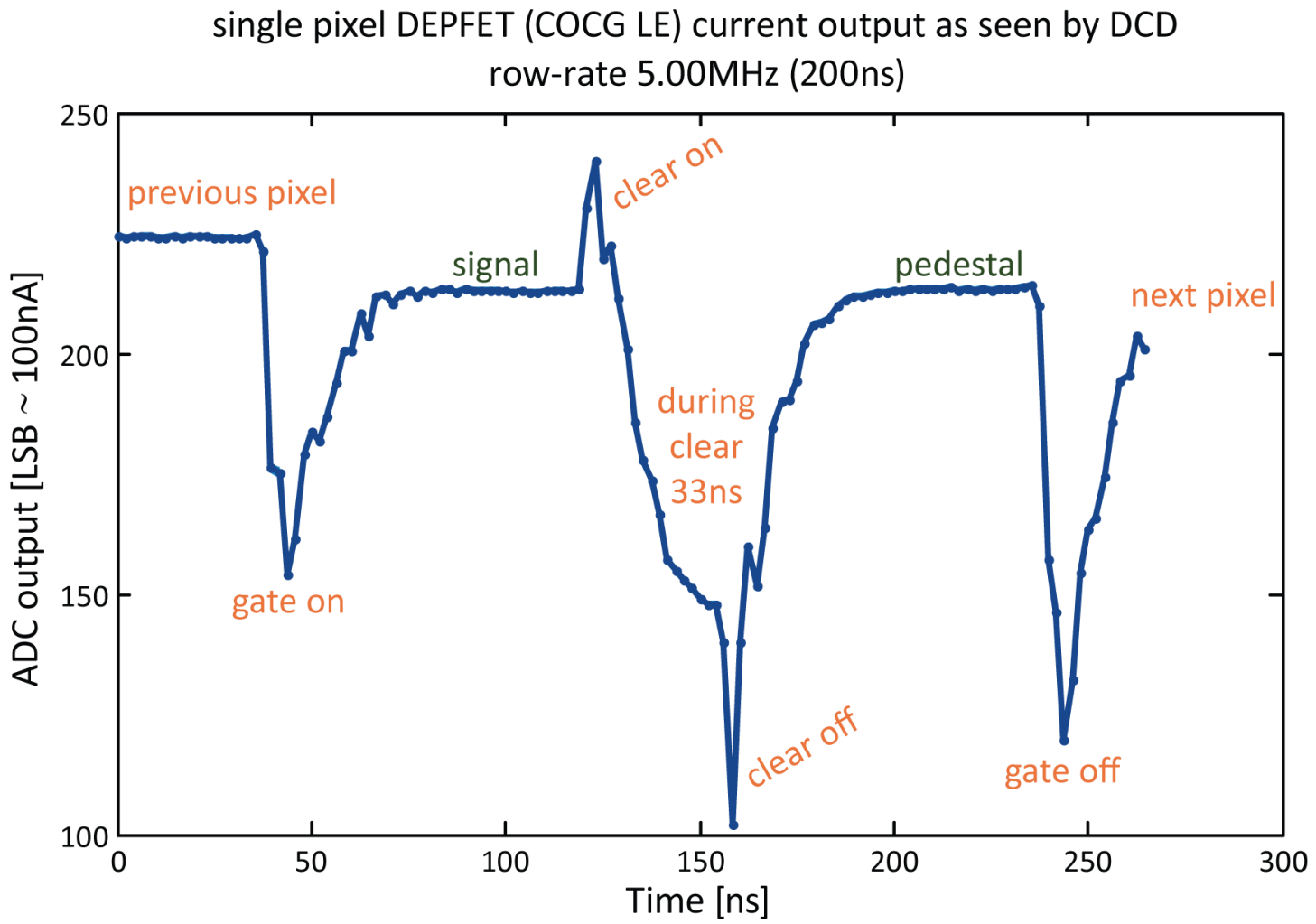
Time resolved DEPFET output current (still to slow)



- noise still very low, spikes and valleys are (reproducible) really there
- long drain recovery time after DEPFET gate/clear switching
  - → overlapping Gate-Switcher outputs?

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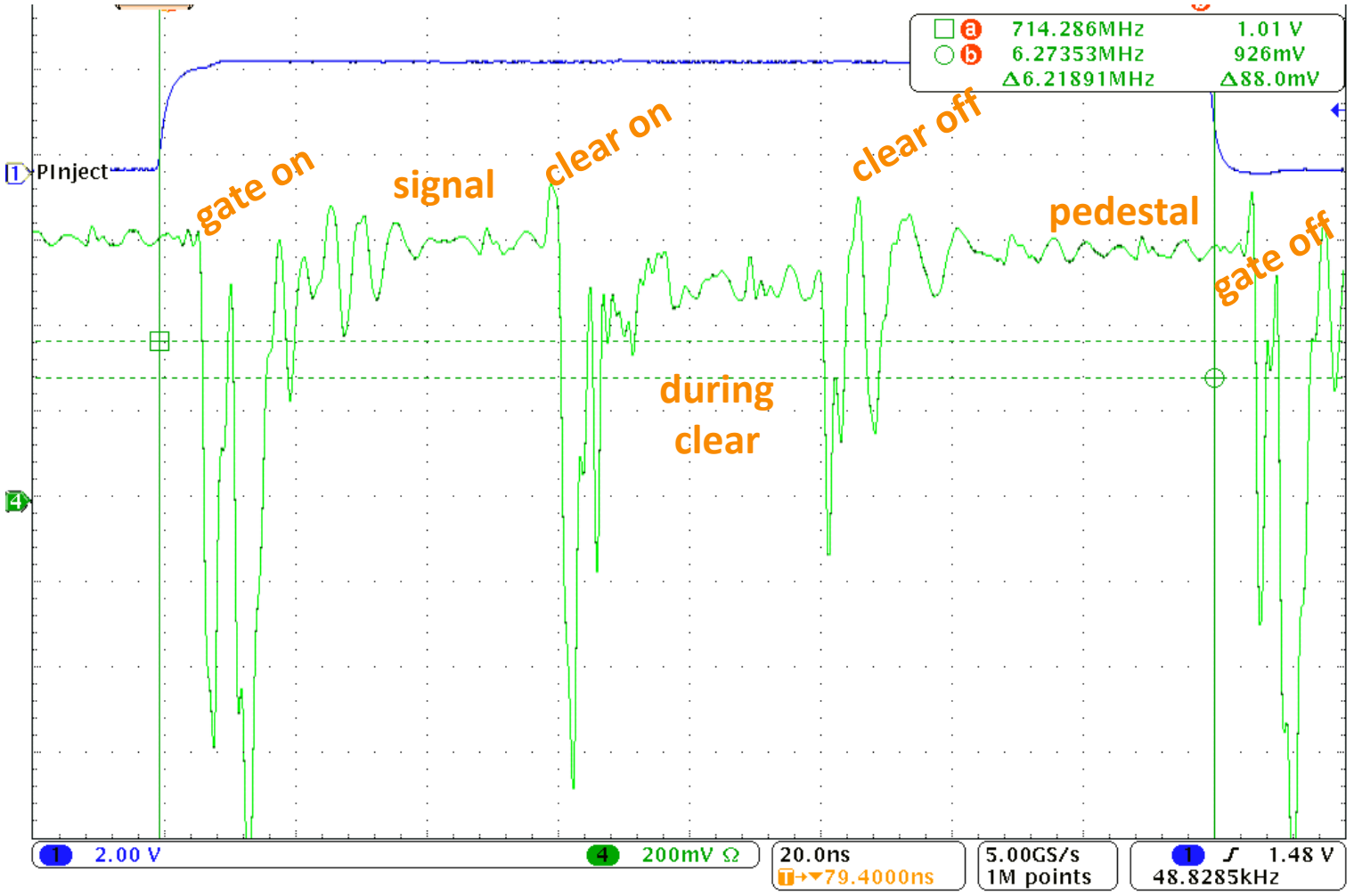
Direct TIA output of DEPFET @6.2MHz row-rate



- note: noise/oscillations due to wide bandwidth of TIA , simple setup and crosstalk

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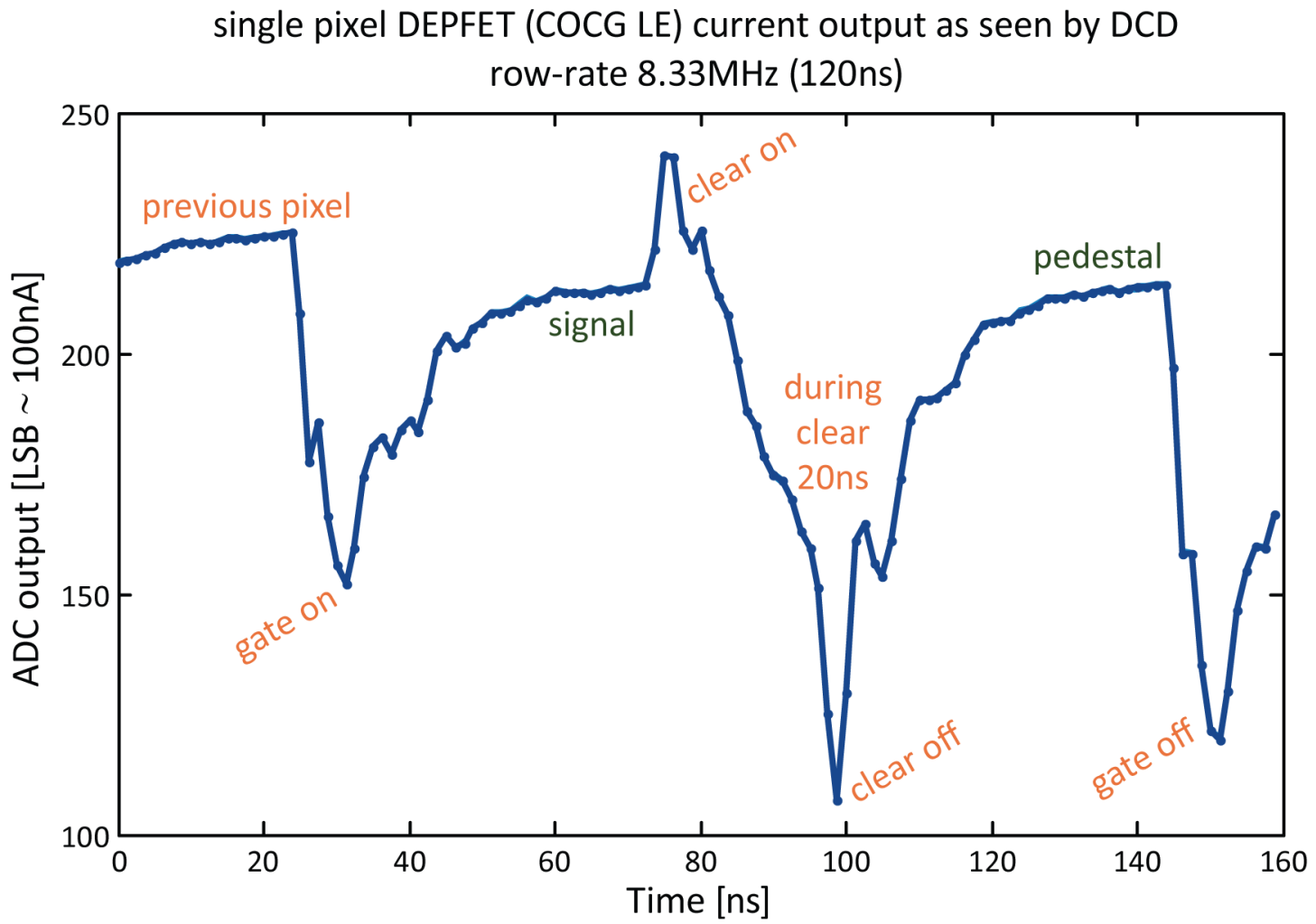
Time resolved DEPFET output current (half of target speed)



- settling time is more dominant now
- sampling steps now 1.25ns → more details on edges

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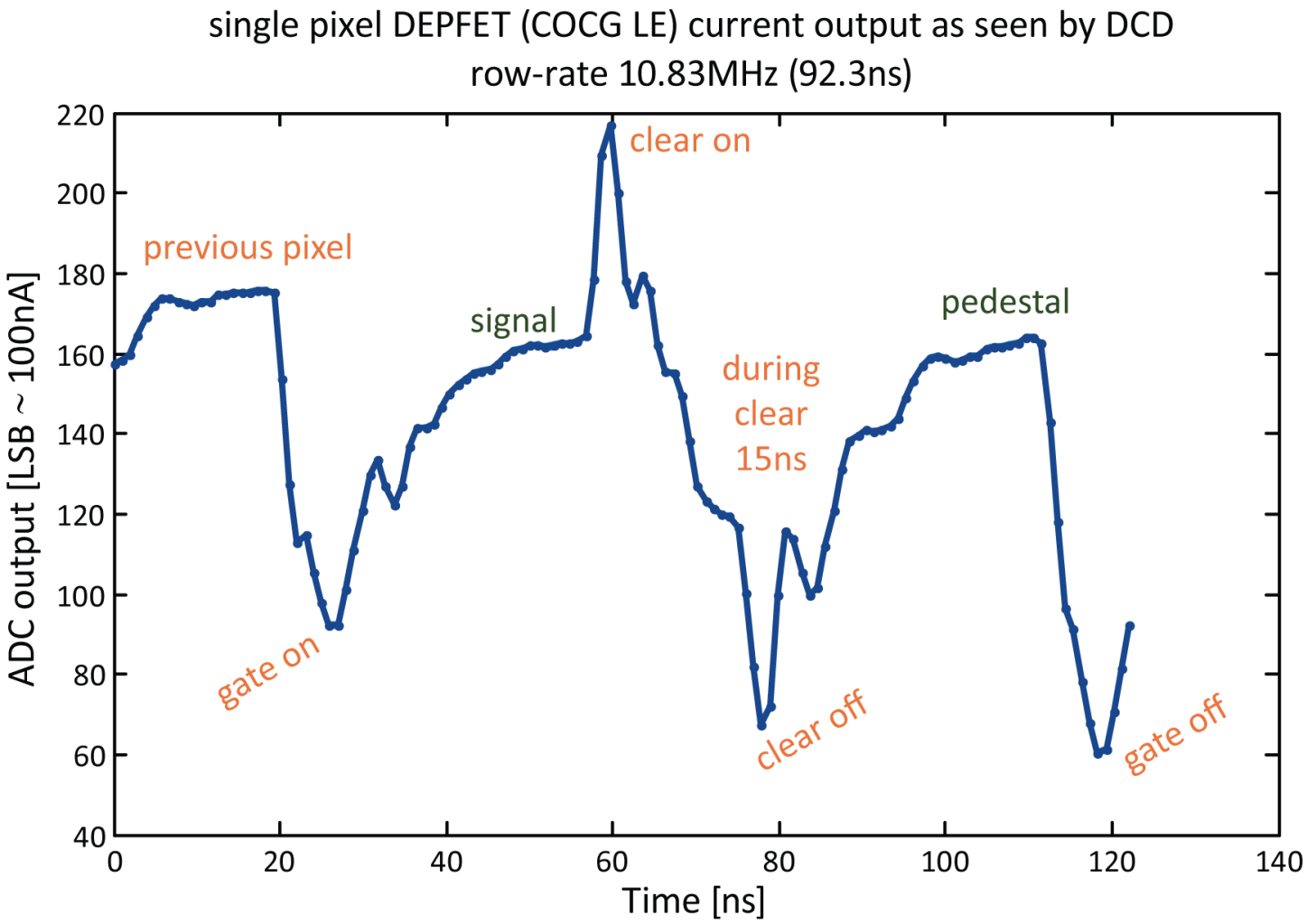
Time resolved DEPFET output current (maximum speed so far)



- no longer good settling behavior!
- sampling steps now 0.96ns
- speed limits given by DCD and FPGA implementation

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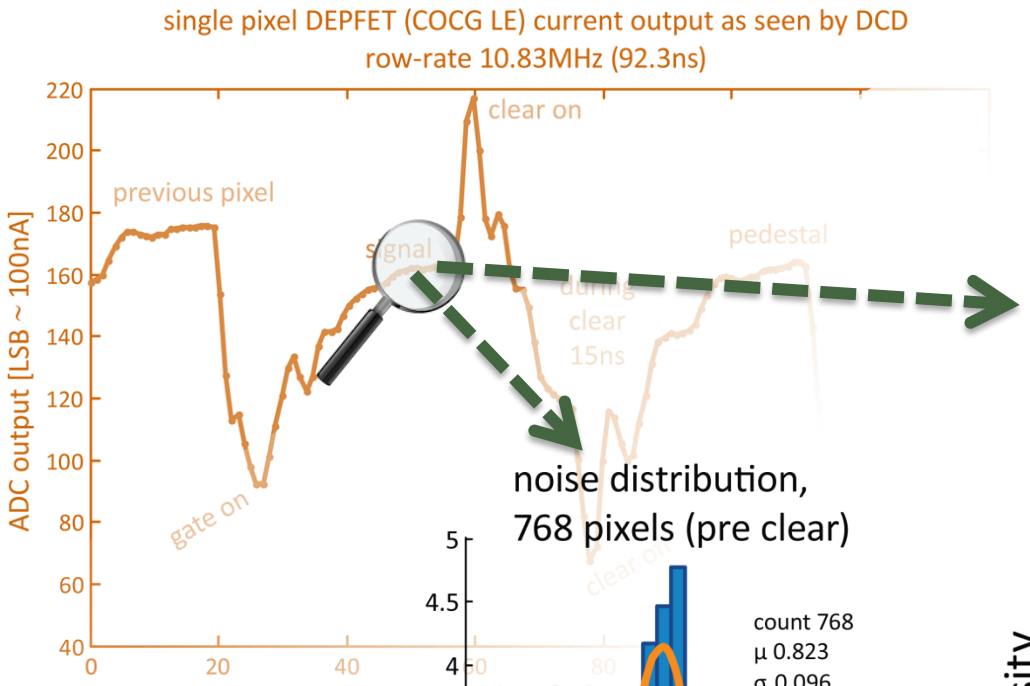
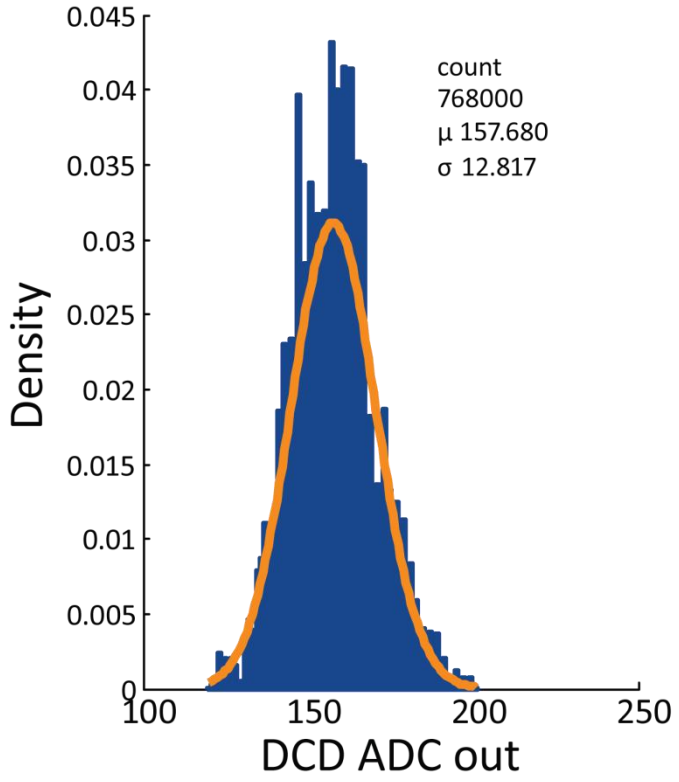
Time resolved DEPFET output current – statistics

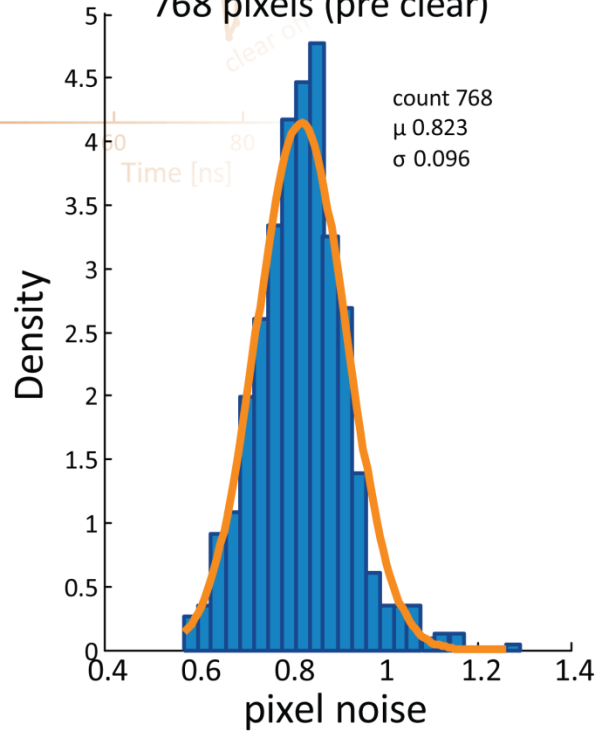


768 pixels signal and noise distribution - fast readout -

all pixels ADC distribution
768 pixels 1000 samples (pre clear)



noise distribution,
768 pixels (pre clear)



expect changes
for larger devices!
This is low-cap
COCG L E

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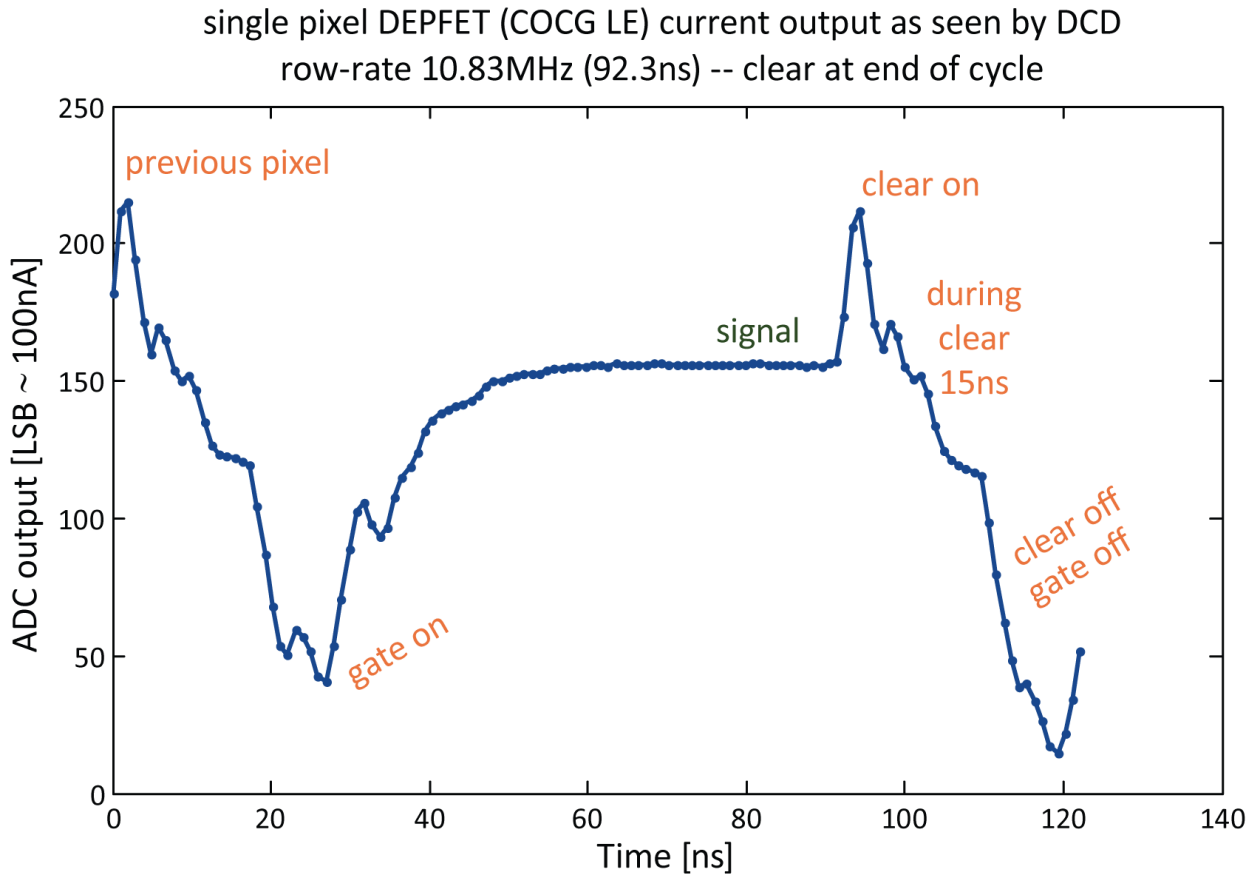
Time resolved DEPFET output current – late clear for single sample



- put clear at end of time, sample only once with DCD
- safety margin for
  - large devices / long drains
  - longer gate/clear rise times (quad-rows, CCCG, length, …)
  - jitter, delay on lines, …

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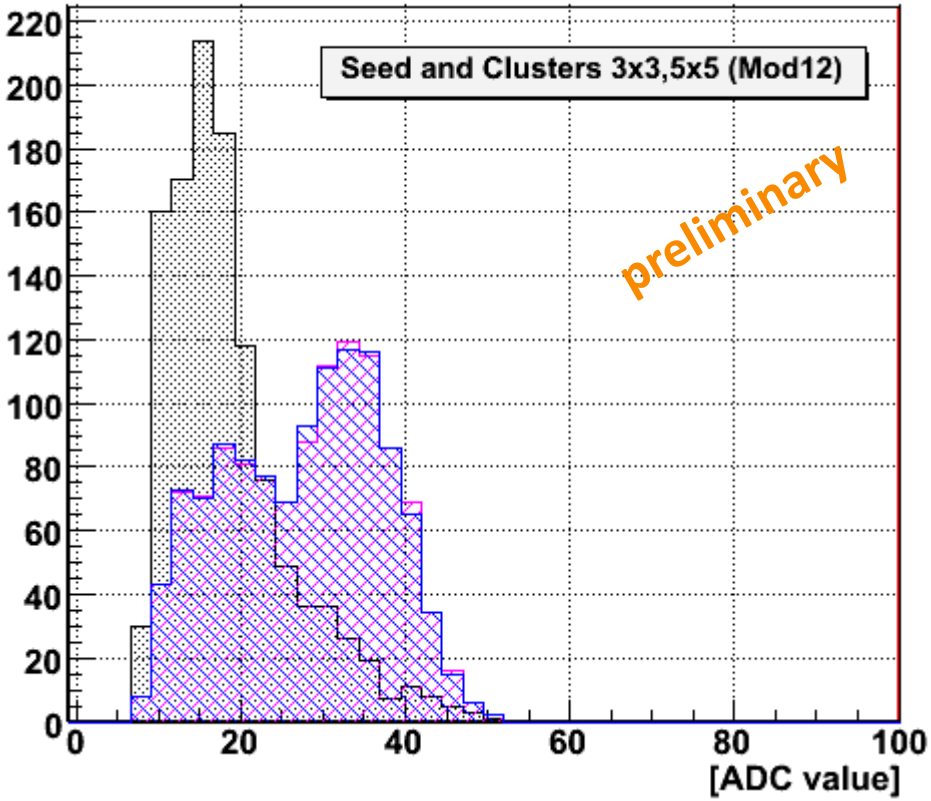
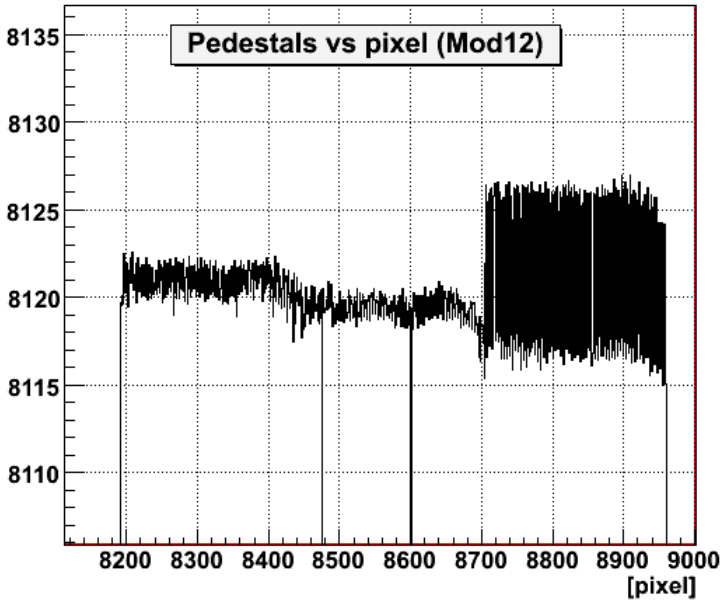
Am241 Source – double sampling

- only one row (256 pixels) available for seeds
- measured 300k frames
- preliminary look on the data with modified existing Monitor Software
- T_{row} 2000ns





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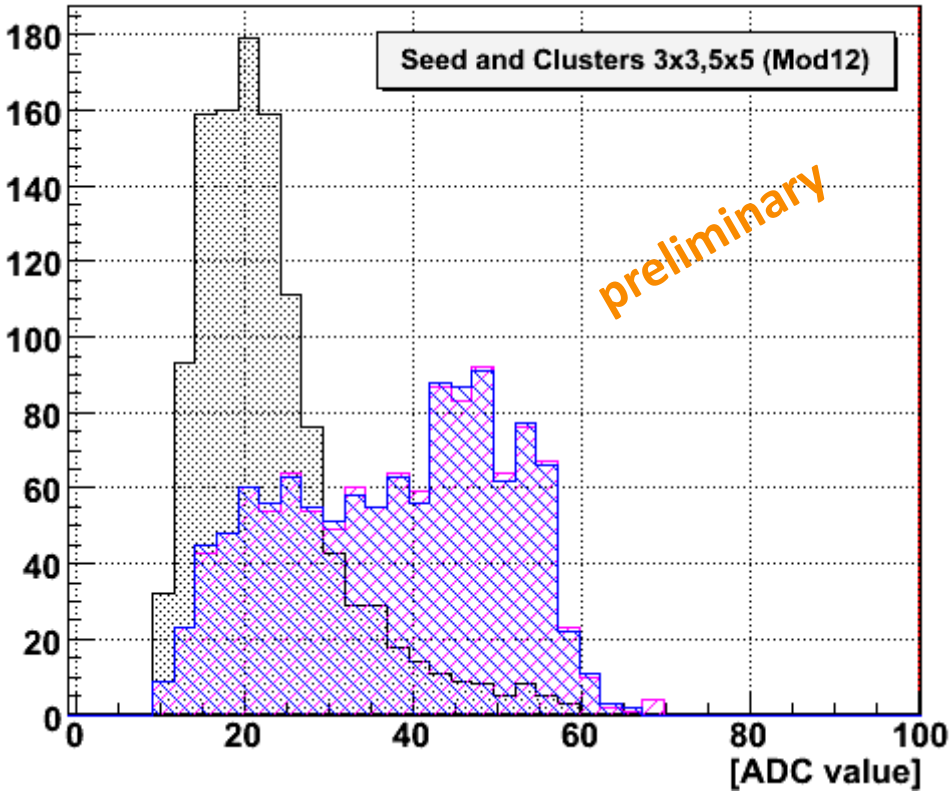
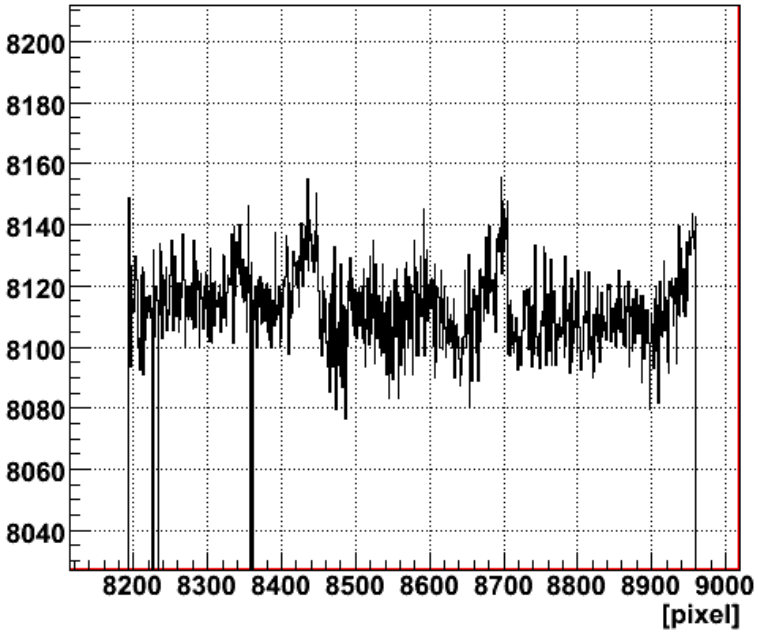
Am241 Source – single sampling

- no longer double sampling with DCD
- pedestals given by first 1000 frames





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Summary

- DCD system allows time resolved studies of DEPFET signals
- DEPFET / DCD sees first source signals!
- directly connected TIA is a great educational tool!
- next step: use available PXD5 large DEPFET matrix

- For T_{row} 90ns double sampling barely allows settling of signal
  - extrapolating for larger DEPFETs: no longer possible
  - unless we enhance the Switcher (overlapped outputs)
- single sampling works (technically)
  - need more studies with source/laser at high speed readout
    - try running-average 'digital double sampling'
    - DEPFET pedestals stable (even for long runs ~6h)

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DCD2 test system and results

Barcelona 10/2009

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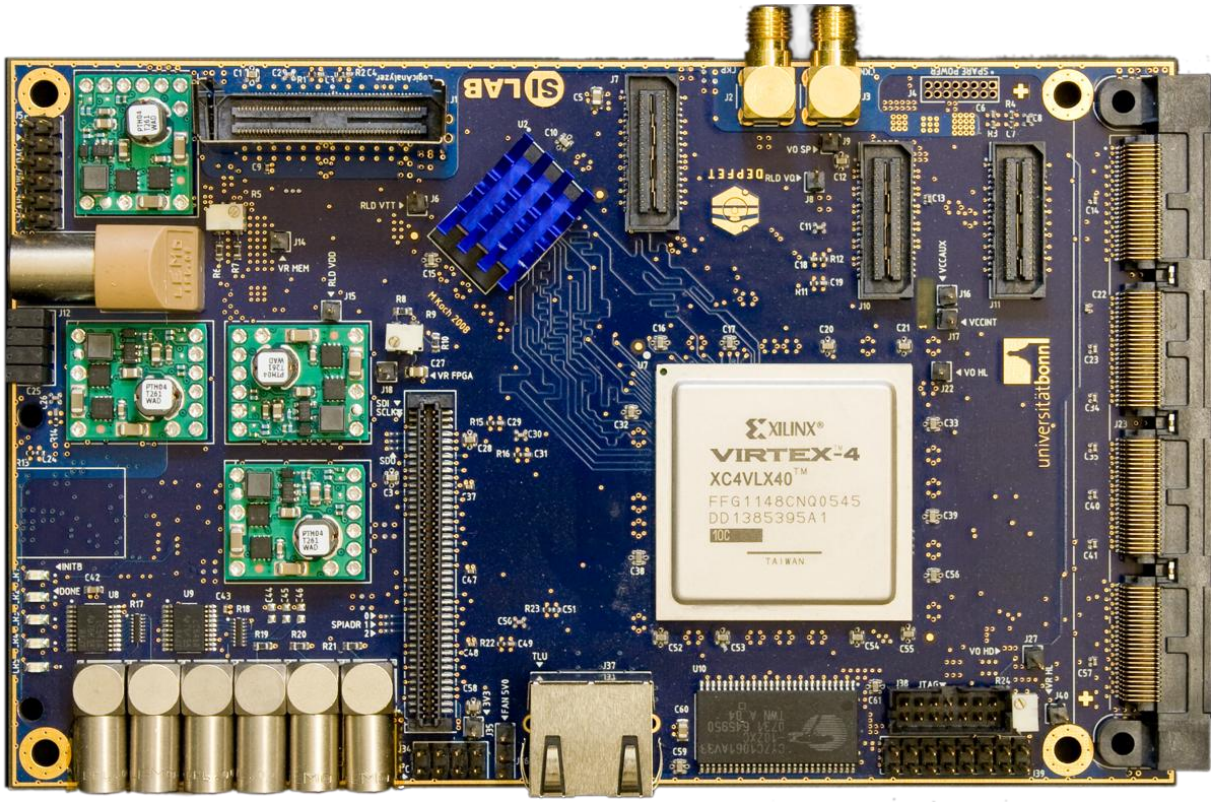
DCD2 Test system (FPGA PCB) - Introduction

- XILINX Virtex 4 LX40-1148
- 288Mbit RLDRAM
- USB 2.0 connection
- 16Mbit async. SRAM
- EUDET TLU connection
- Multiple high speed connectors
- FPGA handles 600MHz data input from DCD
- stable power supplies at high loads



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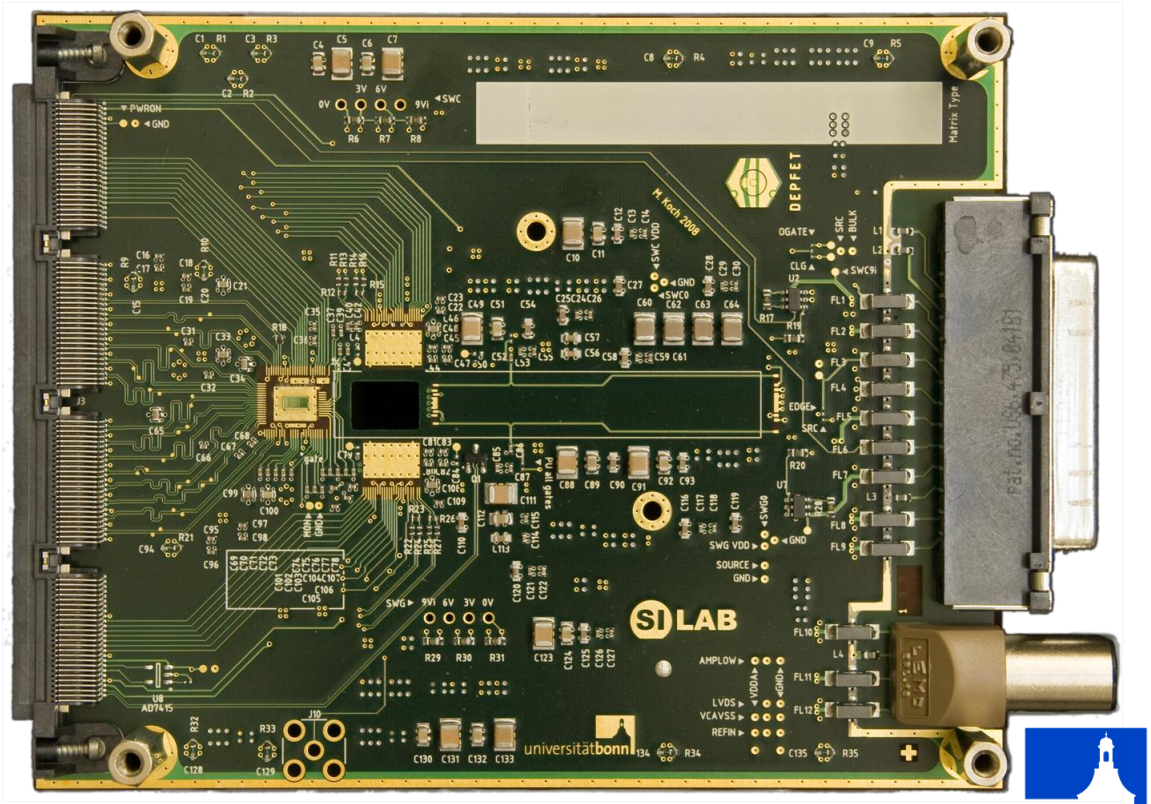
New Hybrid (Bonn v4) - Introduction

- integrates DCD2, Switcher3
- 128x128 matrix &
  256 x 1024 (2 Switchers)
- design focused on
  - signal integrity for DCD
  - stable power supply
  - low noise design
  - testability



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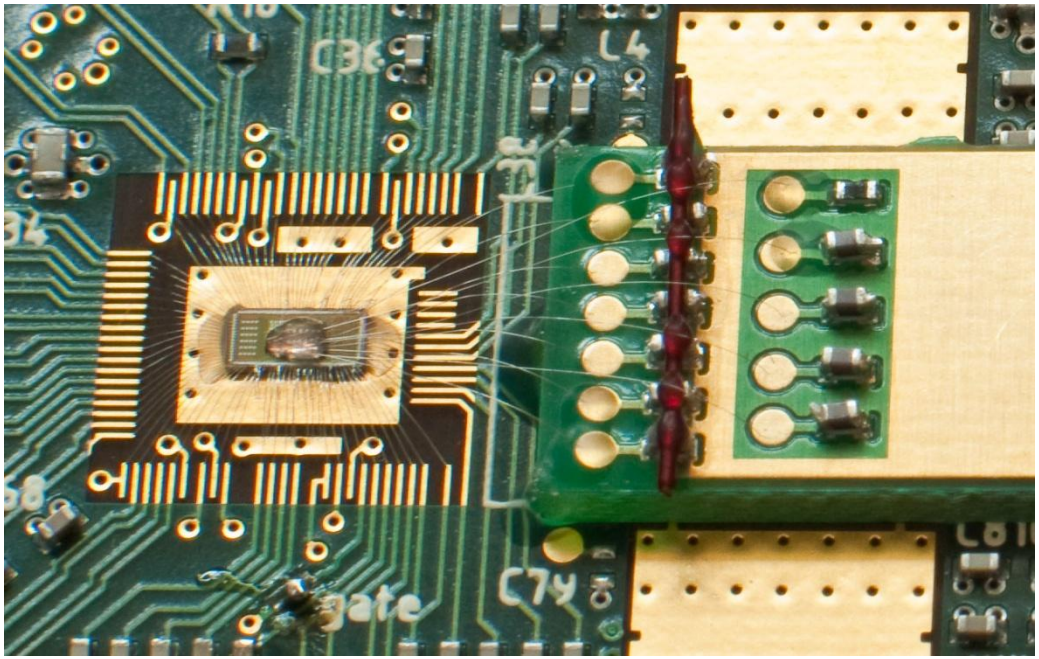
DCD noise vs. direct input capacitance

- 11 values of input capacitance
- 4pF … 82pF
- bonded directly to DCD's input bump-pads



- noise (almost) independent of operating frequency

- note: changes expected for larger devices
  - C distributed over long resistive line

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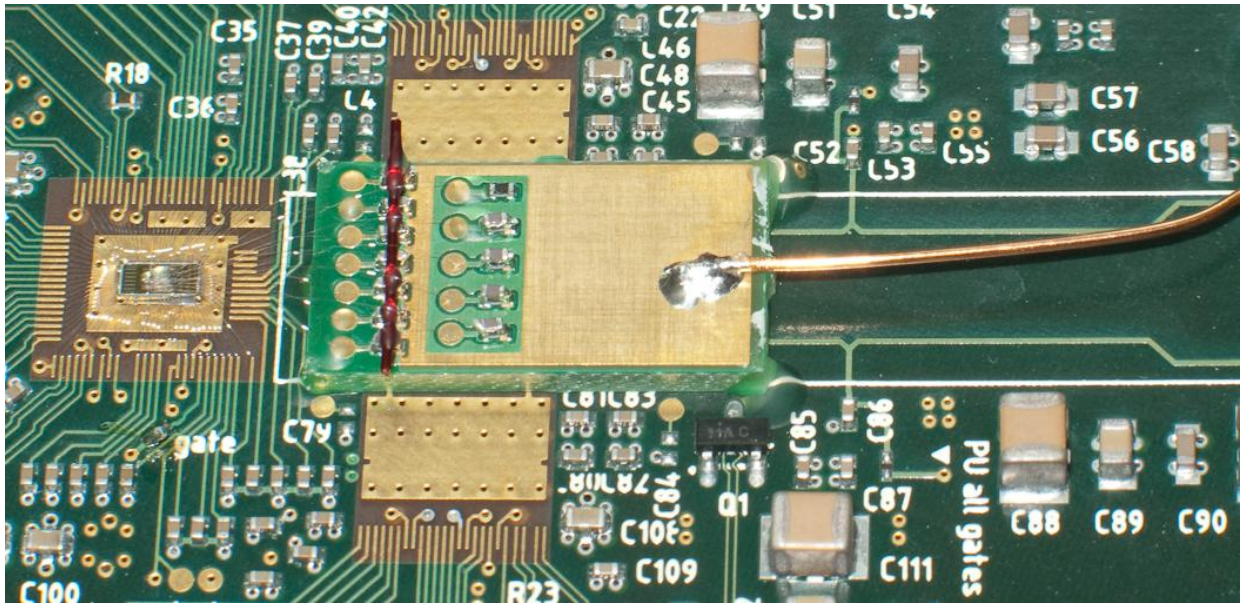
DCD noise vs. direct input capacitance

- previous measurements (Ringberg 05/2009) showed too high noise
- problem due to grounding of capacitors
- easy fix with shorter and more wires



full picture of ‘unfortunate’ setup

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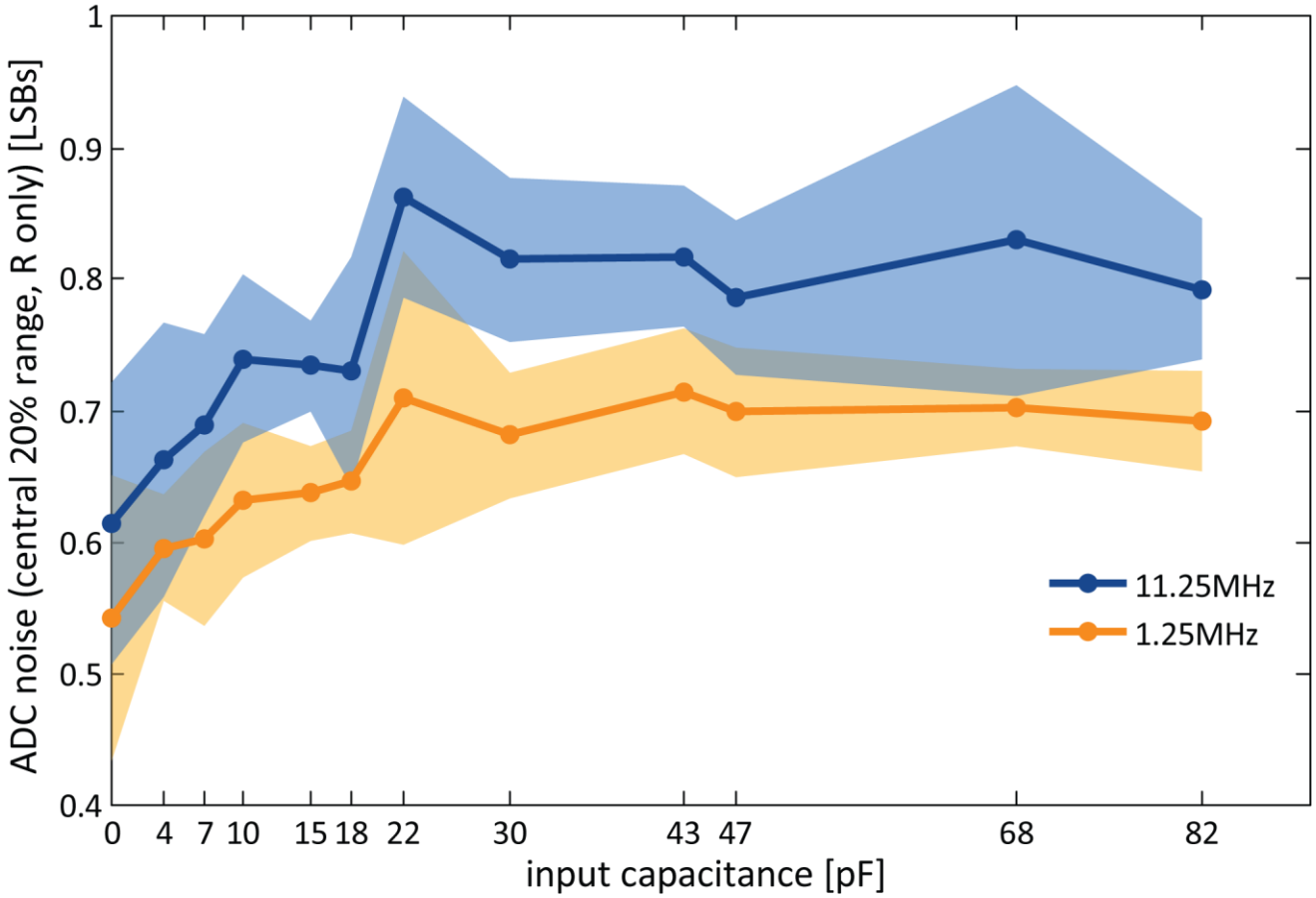
total noise vs. capacitance



- correction to plots shown in Ringberg 05/2009
- not optimized for speed / rise time

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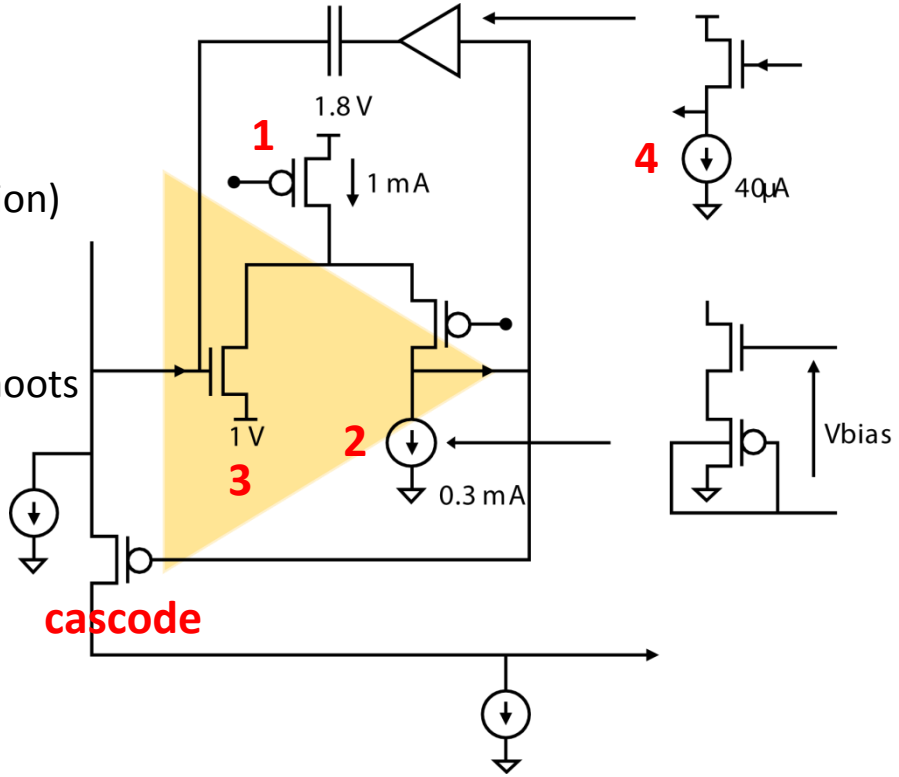
Cascode – schematic

- biasing:
  - 1: VCascAmpBias (main power consumption)
    - more power, more speed
  - 2: VCascAmpLoad
    - DAC < 250: fastest risetimes, overshoots
    - DAC ~ 300: optimal
    - DAC > 350: speed loss
  - 3: VCascVSS (amp ground)
  - 4: VCascAmpSF (compensation)
    - DAC = 250



- total speed also depends on current flowing through cascode transistor
  - good results with minimum 10µA
  - maximum(!) 50µA working range
  - DEPFET has ~50-100µA drain current -> subtract some current in front of cascode

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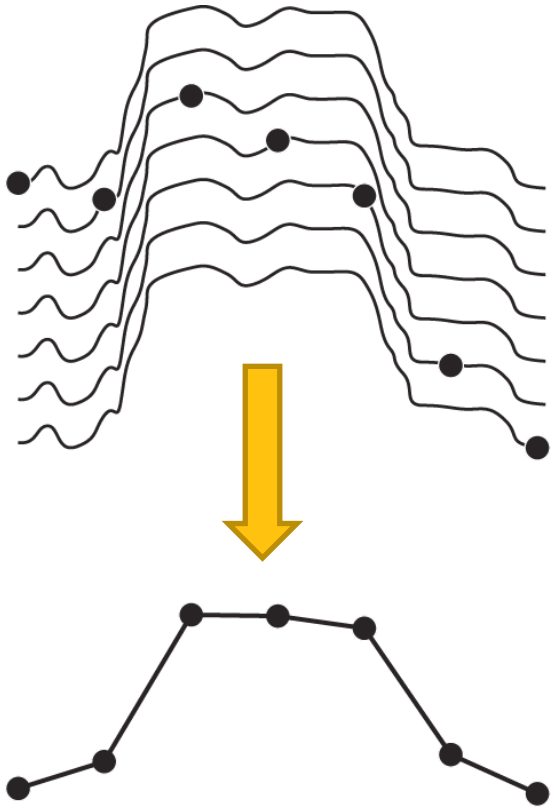
time resolved measurements with the DCD

- DCD can take **one** sample per T_{row}
- use **sequential sampling:**
  - **One sample** is taken from each of a number of similar waveforms.
    - or average over more samples
  - time shift the sampling point
  - The samples are **assembled** to form a composite waveform.
- requires periodic and stable input signals
- current implementation allows 96 samples per T_{row}
- time resolution depends on DCD speed
  - eg. T_{row} = 1500ns : steps of 15.6ns
  - eg. T_{row} = 96ns : steps of 1.0ns
- this technique is used for
  - rise time measurements
  - time resolved DEPFET current output
  - investigation / setting of optimal sampling points
  - …



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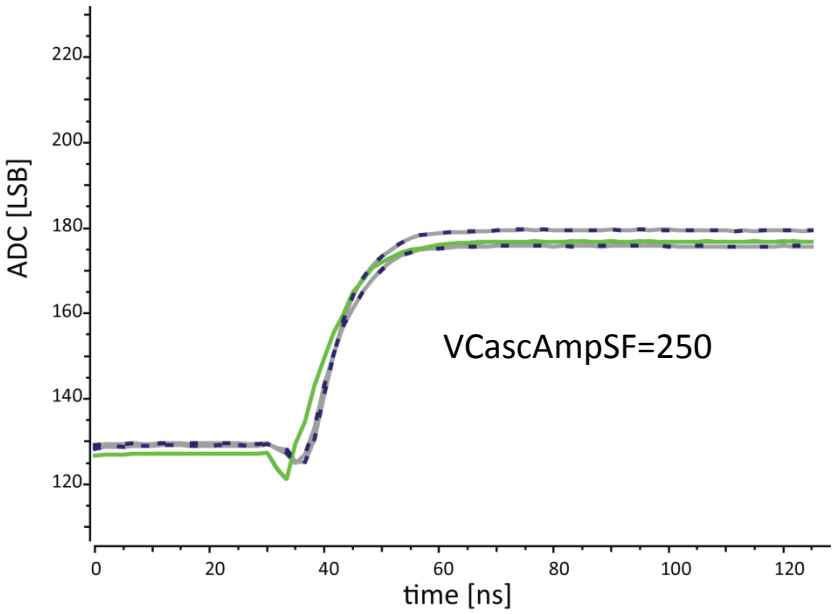
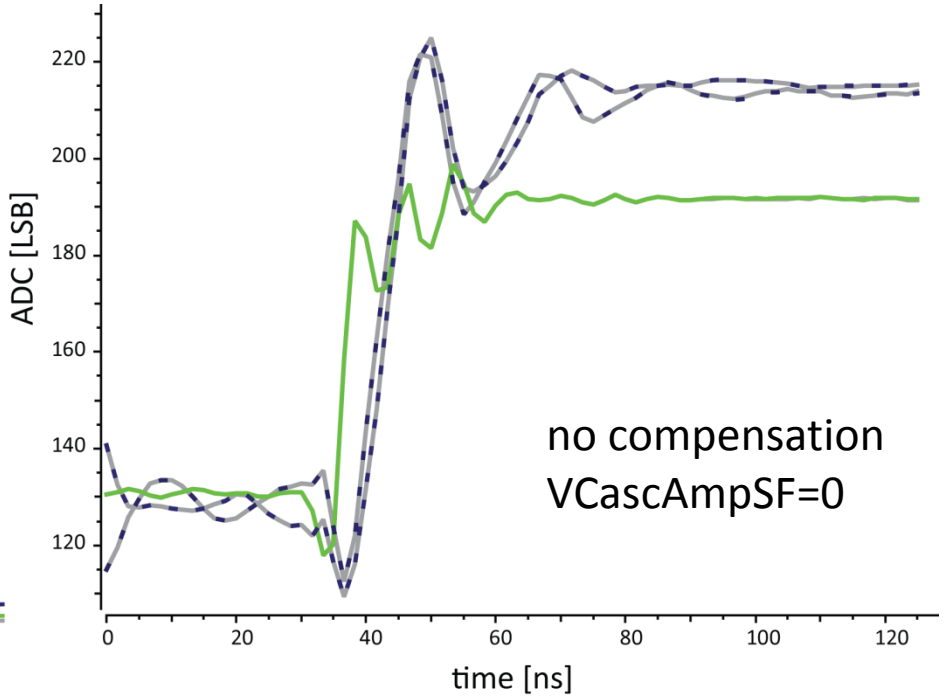
Cascode – compensation / typical output

- for all measurements:
  - generate current step @DCD input
  - sample with ADC
- fast settling based on VCascAmpSF
- can choose critical damping for optimum speed





- vdda 1900, vcavss 1050, CascAmpBias 500 CascAmpLoad 200 CascAmpSF 250 InjBias 200 InjSig 80 “sf compensation.ini”
- DCD runs with 160ns T_{row} to clearly see rise time

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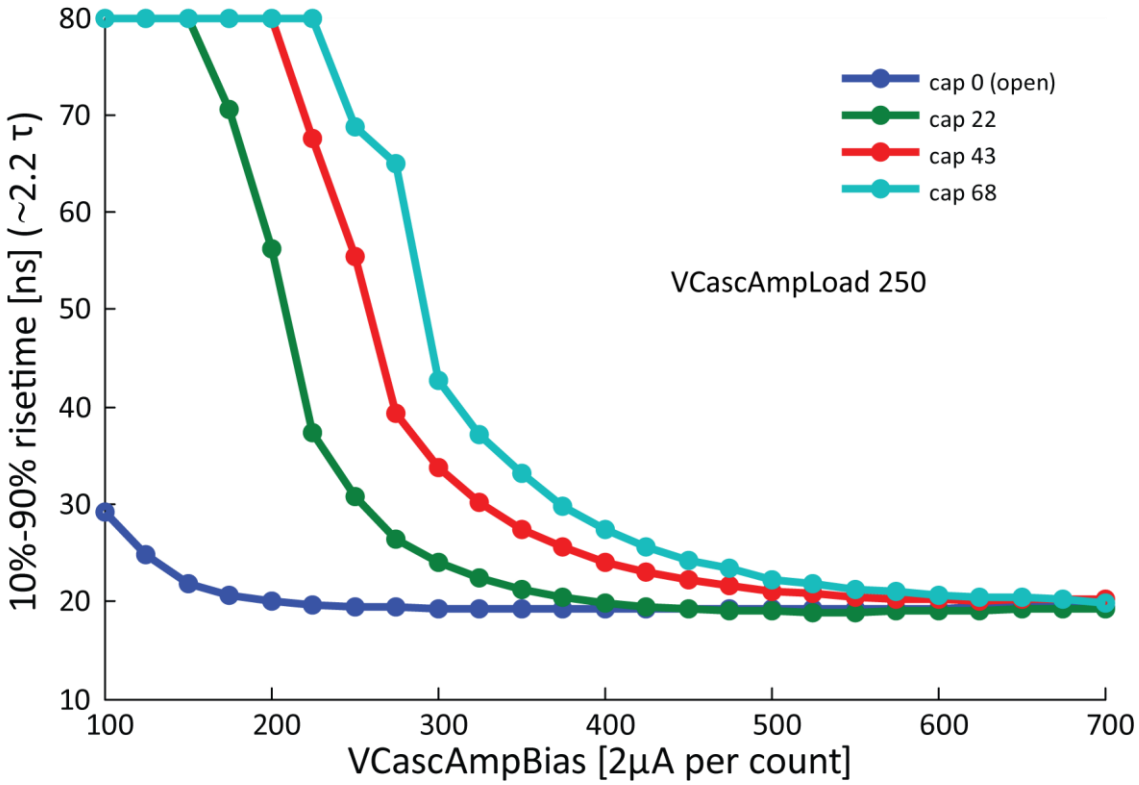
cascode dynamic behavior – speed



- For reference, power based on chip total, per channel:
  - @500: 5.5mW
  - @600: 5.6mW
  - @1000: 6.4mW

- 20ns limit is given by DCD current memory cells

- settings chosen for rise behavior without overshoot
- vdda 1900, vcavss 1050, CascAmpLoad 250 CascAmpSF 250 InjBias 100 InjSig 95
- 300MHz readout speed → 160ns sample-clear-sample

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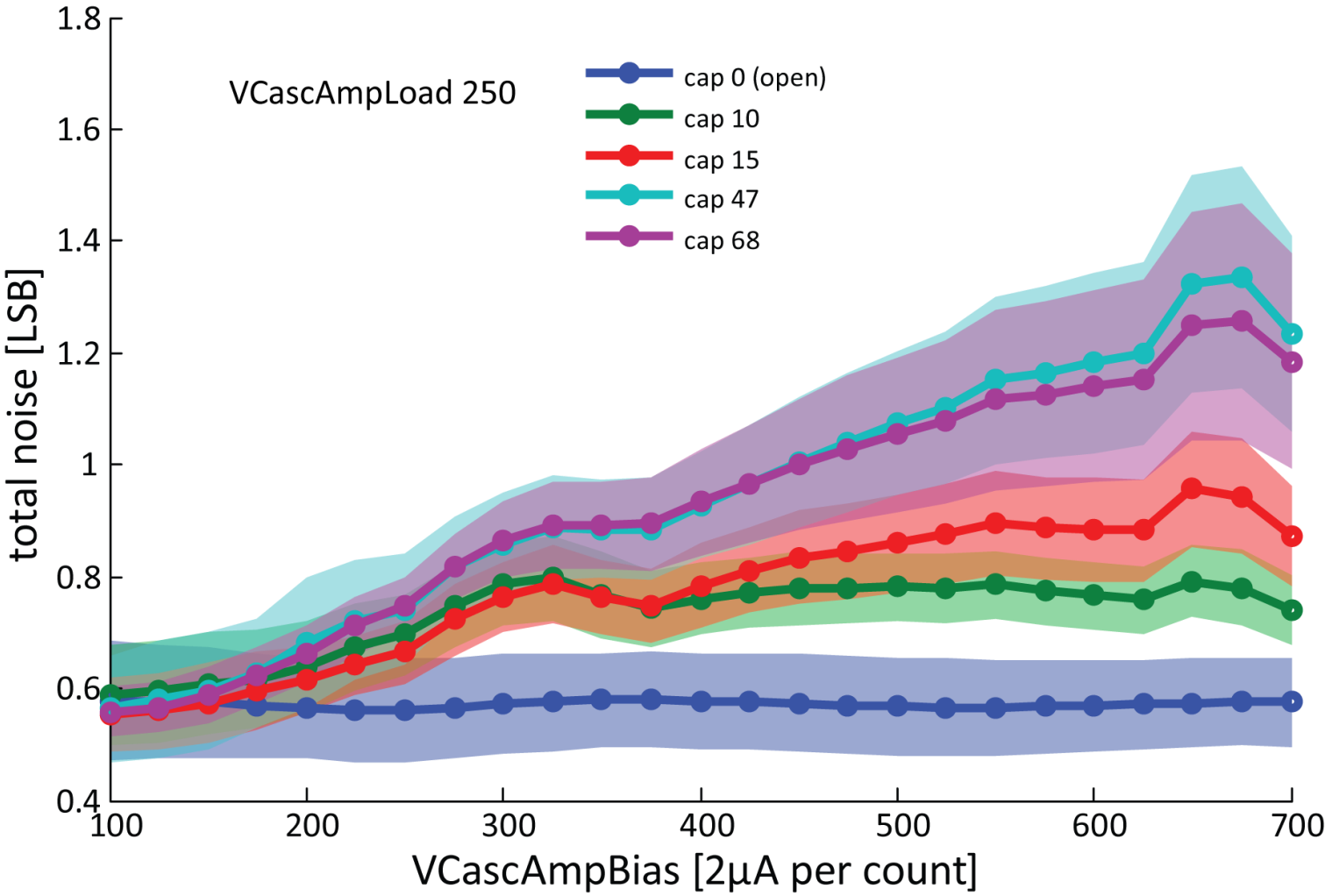
cascode dynamic behavior – noise



➔ @600 VCascAmpBias: for 68pF capacitance, rise time of 20ns with ~ 1.1 LSB noise, 5.6mW/channel total

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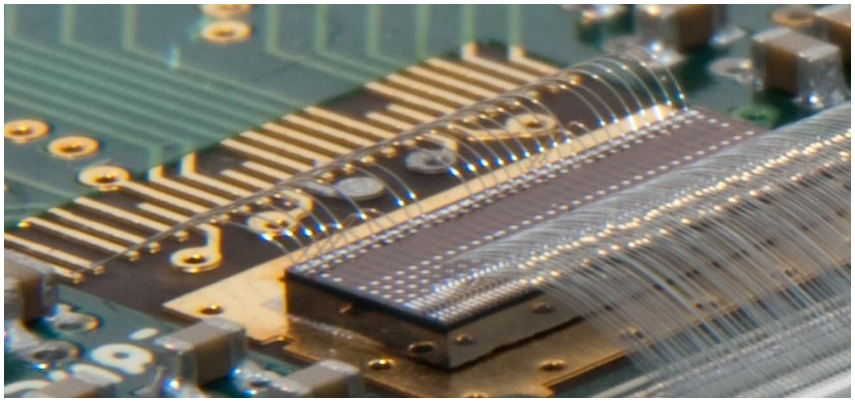
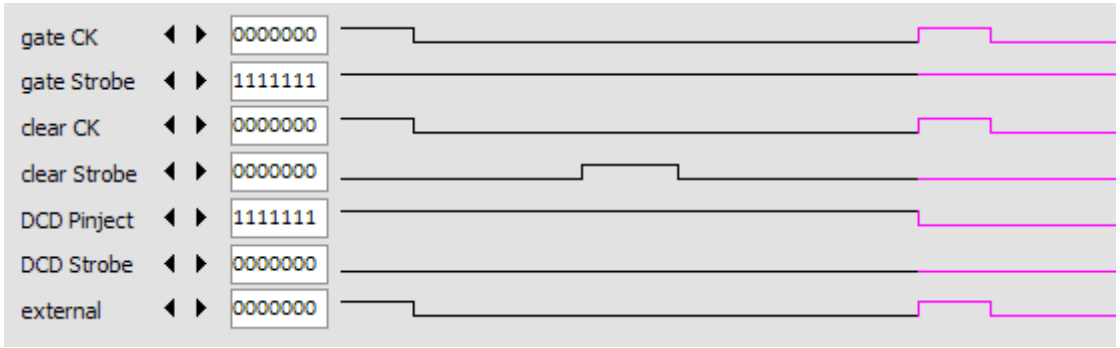
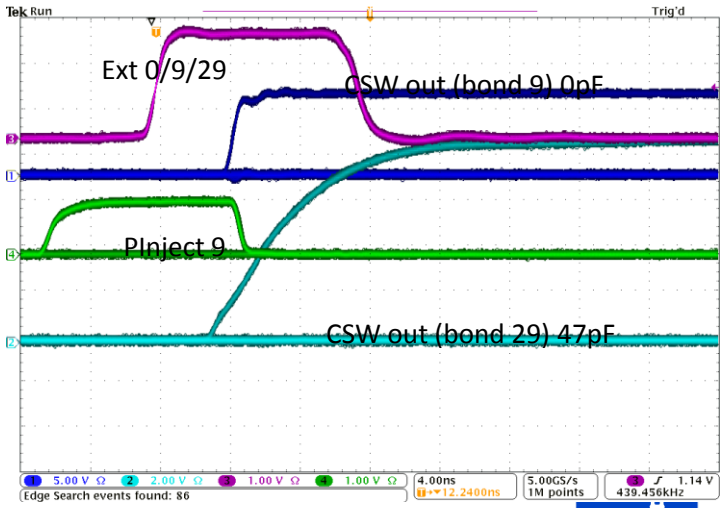
Switcher Integration

- Switcher 3 has been successfully integrated!
  - existing C++ classes / Verilog re-used
- rise times of switcher vs. cap-load confirmed (CK, Mannheim)
- implemented new sequencer
  - allows timing fine adjustment in 96 steps per T_{row}
  - runs synchronized to DCD for repeatable measurements







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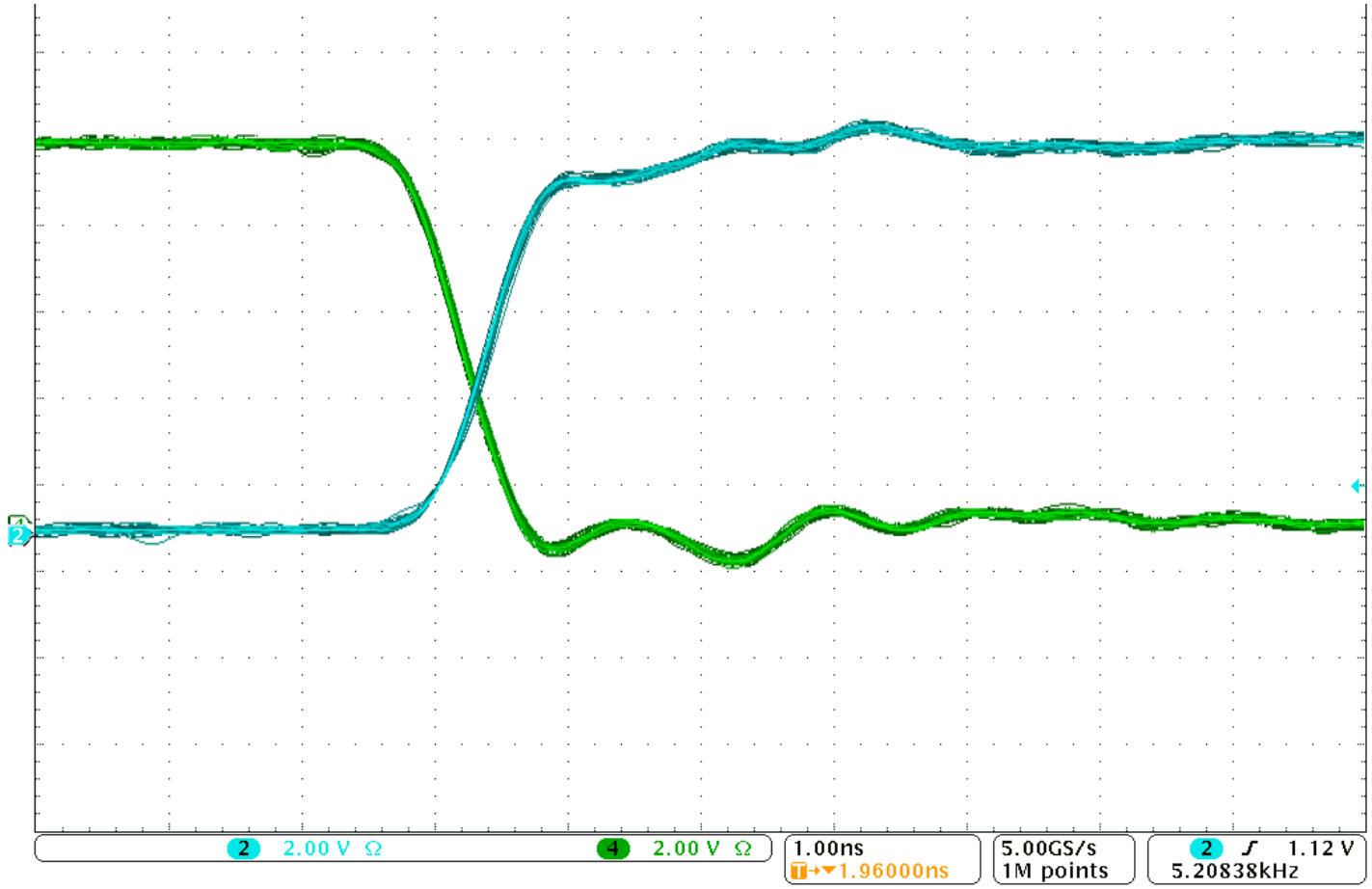
Switcher 3 – output overlap

- two neighboring channels
- no extra capacitive load (Tektronix P6243 <1pF)



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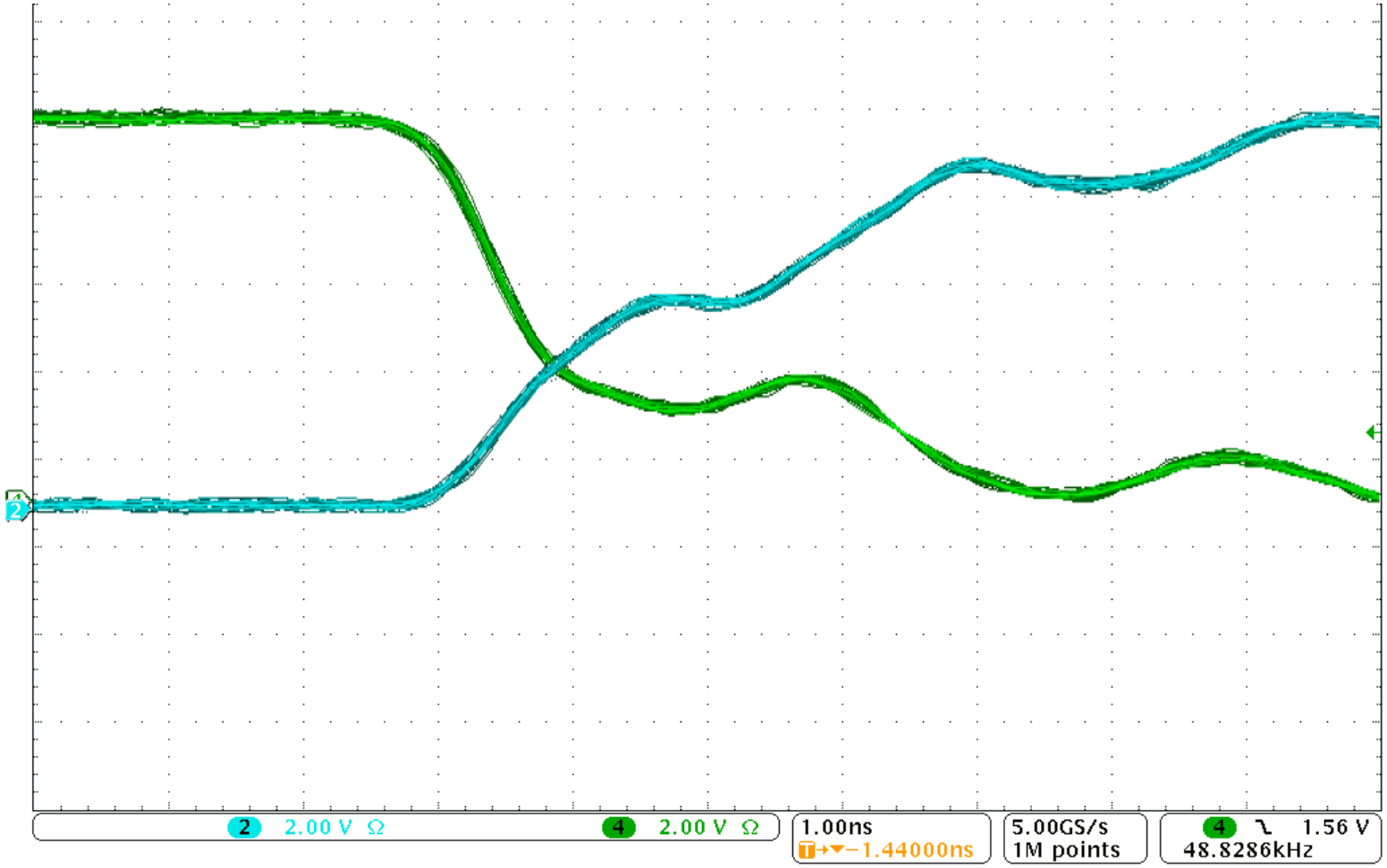
Switcher 3 – output overlap

- two neighboring channels
- extra 22pF capacitive load (+ Tektronix P6243 <1pF)



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DEPFET Matrix Integration

- running with COCG L E device
  - 6 drains (3 pixel columns) connected to DCD fast ADCs
  - 4 drains connected to DCD slow ADCs
- sequencer implementation allows fixed assignment of DEPFET pixels to either DCD's L/R ADC
- for reference, voltages used:
  - Source: 7.0V
  - CCG: 6.4V
  - clear low: 10.5V
  - gate on: 3.2V
  - Switcher Δ: 9V
  - bulk: 17V
  - HV: -180V

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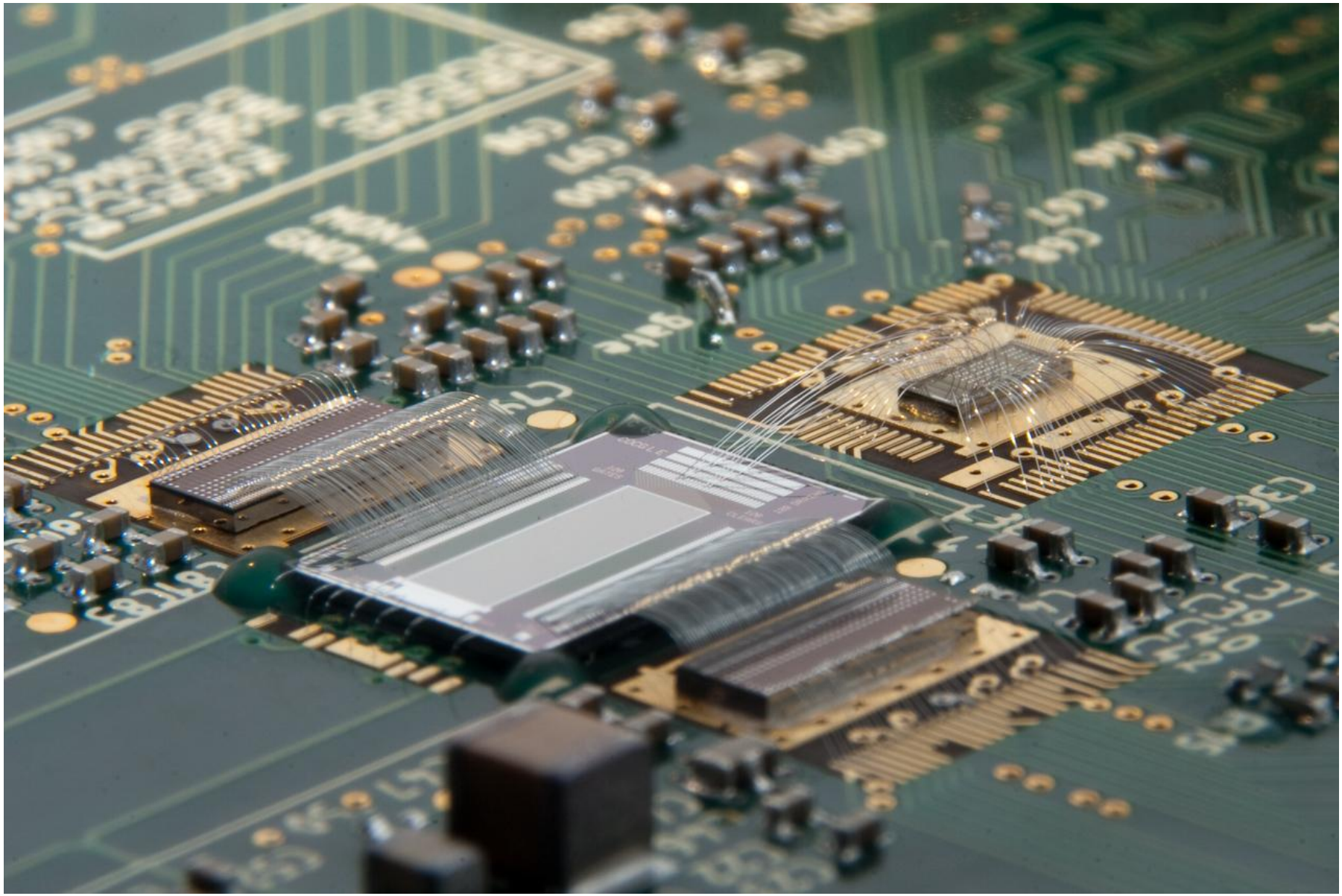
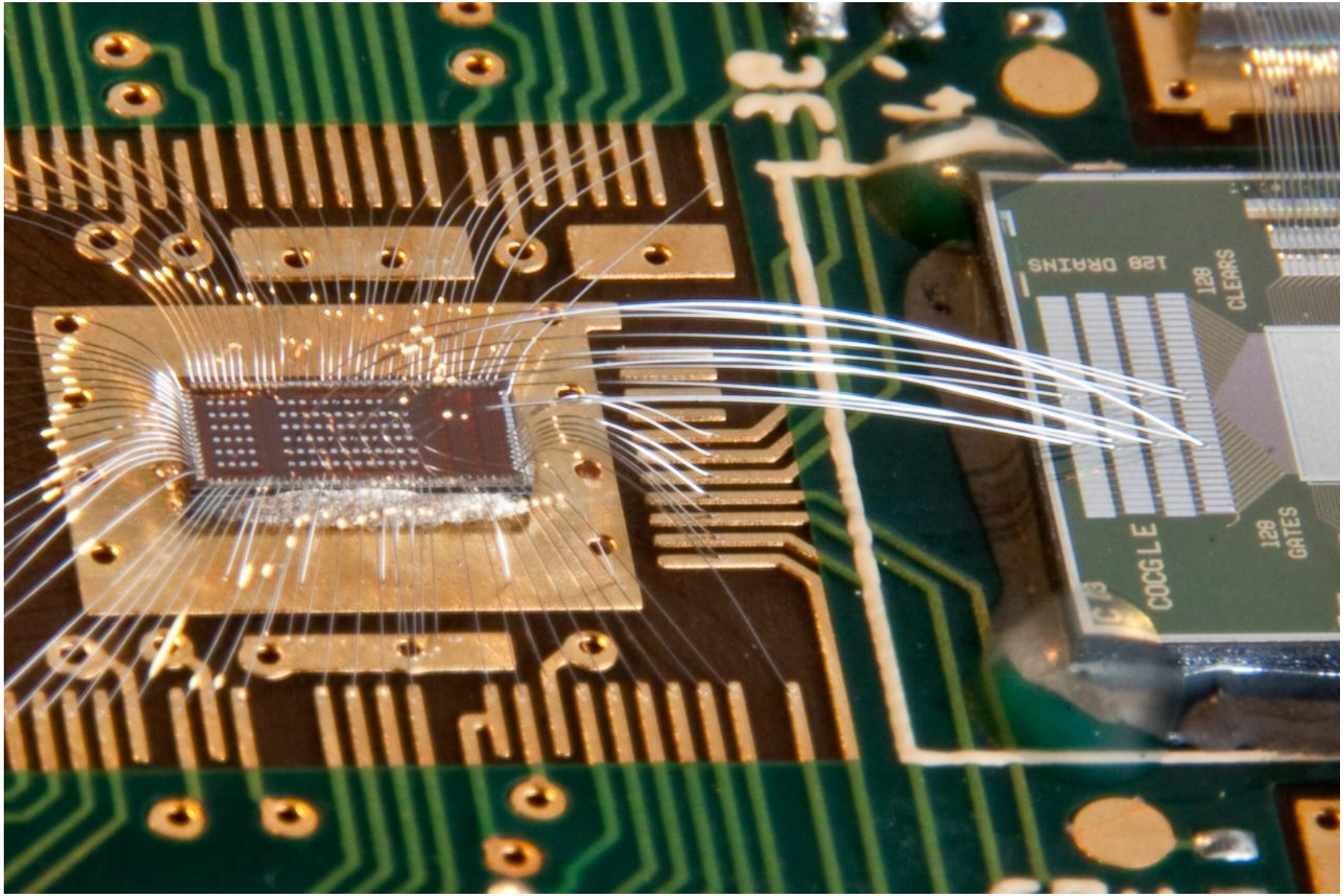
DCD, Matrix and Switchers



DCD bonded to matrix



Summary

- DCD now fully integrated into system with Switchers and DEPFET
  - first source measurements
  - time resolved DEPFET output signals
  - allows detailed studies of single-sampling, clear optimization, …
- DCD measurements
  - cascode:
    - ~20ns settling time can be achieved with reasonable power
    - for 68pF input capacitance, noise of 1.1LSB is possible
  - solution for steps in ADC output found (for next DCD iteration)
    - will improve DNL, INL, noise
  - previous results:
    - 24 µA ADC range possible
    - ADC gain 10.2 ± 0.1 (counts / µA) @12.5MHz
- next steps:
  - compare with large (256x1024) matrix
  - source / laser measurements at higher speed

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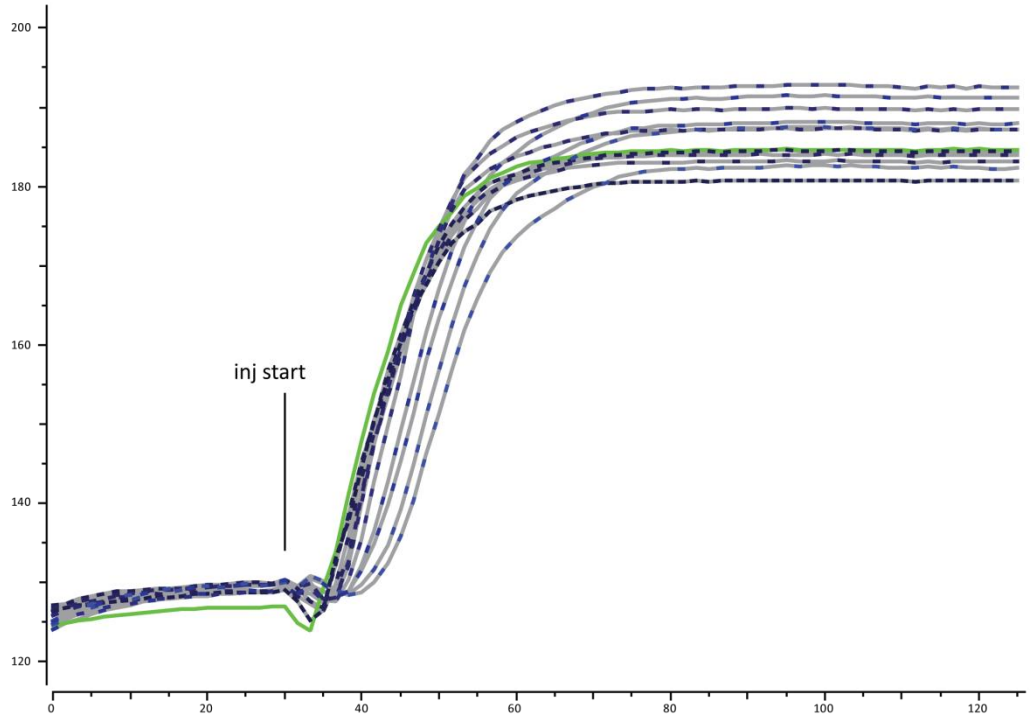
Cascode – measurement issues

- charge injection with current step (see slide)
- overshoots: artificially faster risetimes, longer settling time

- Delays for higher capacitance: (slow settings)
- Possible due to undershoot / charge injection



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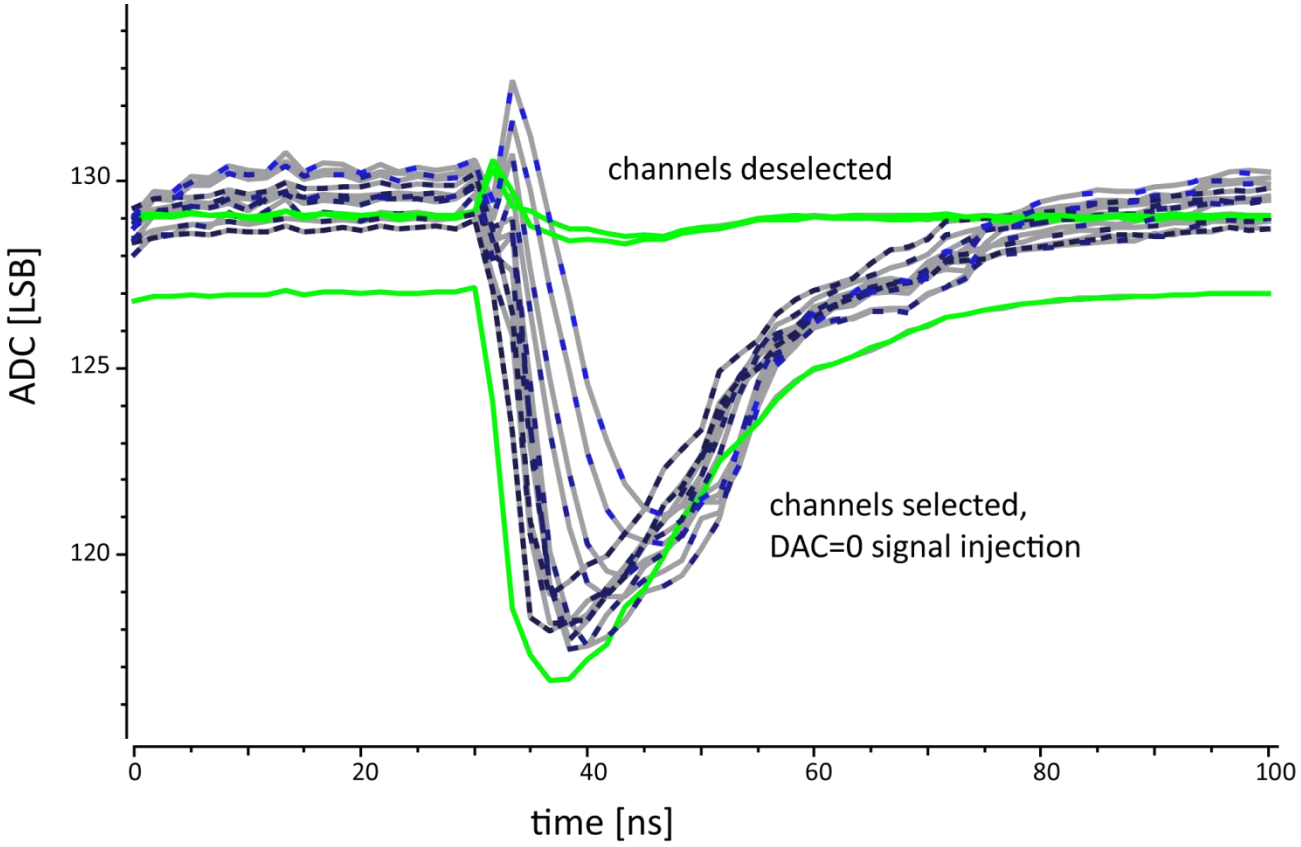
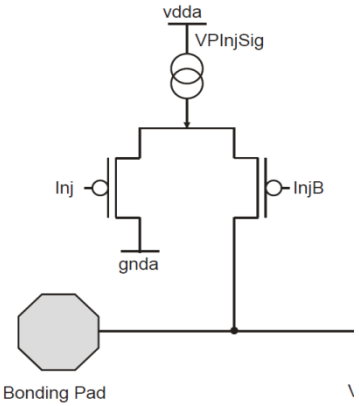
Cascode – charge injection / crosstalk

- Sample input current step, with InjSig=0
- Channels selected (EnInj)
  show undershoot
- deselected ch's quiet
- green channels: no capacitance





- → most likely charge injection due to InjB transistor (InjB goes 1→ 0)

- vdda 1900, vcavss 1050, CascAmpBias 500 CascAmpLoad 150 CascAmpSF 250 InjBias 95 InjSig 0 "casc charge injection.ini"

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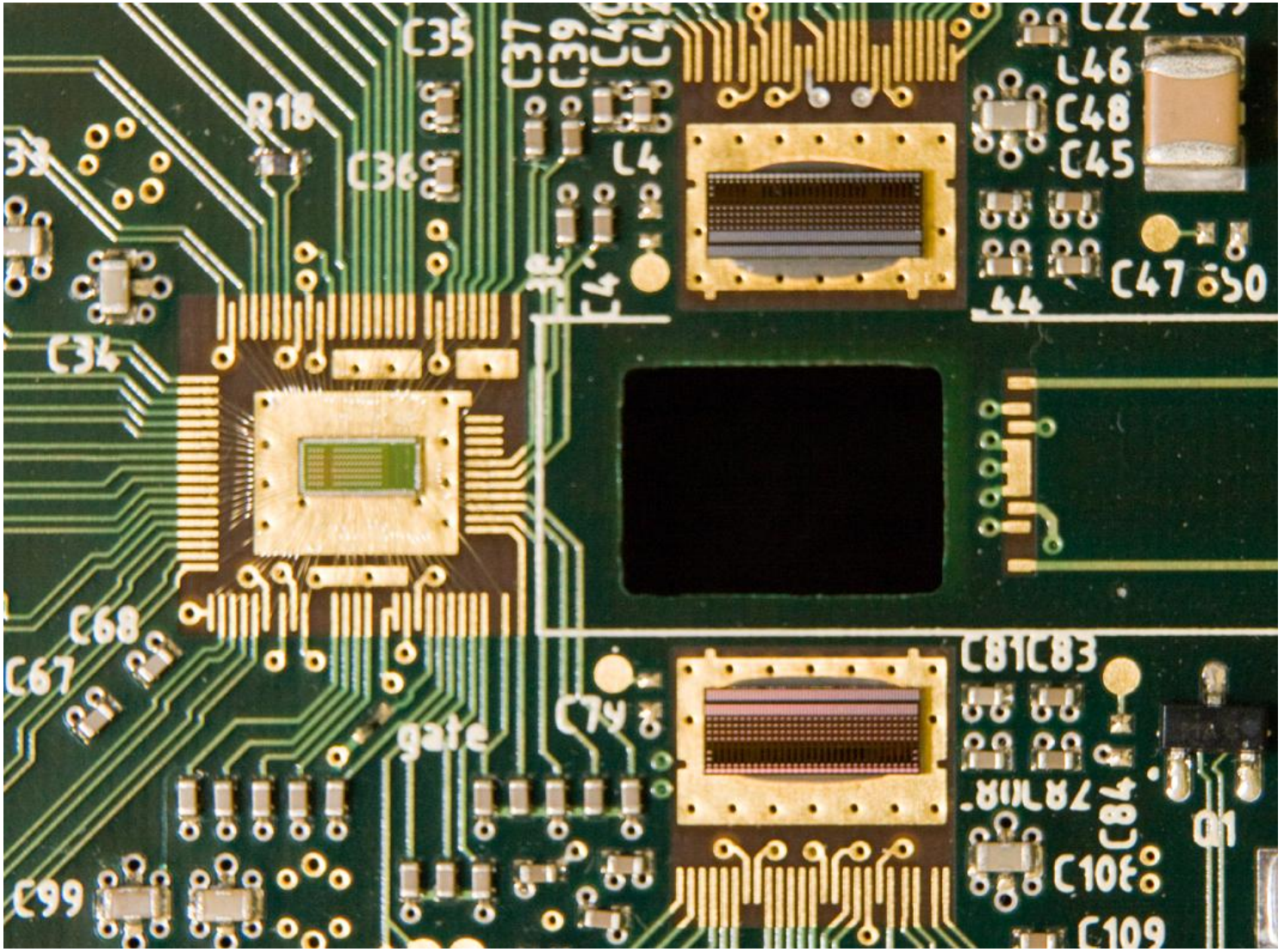
New Hybrid (Bonn v4) - chips



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Summary

- test system working reliable !

- ADC characteristics at 12.5MHz
  - total range of ≈ 24µA
  - gain ≈ 10 ± 0.1 LSBs / µA → LSB ≈ 100nA, small spread
  - DNL ≈ 1 LSB, INL < 4 LSB
  - noise: 0.9 LSB, ≈ 1.2 LSB with L/R ADCs combined
  - noise doubles with 60pF input capacitance

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