- Status of UBM Development (3rd Metal layer in Cu)

- Ladder geometry
  - -: Micro joint for layer 2 (and 1??)
  - -: Geometry
  - -: Plans for dummies

-: Assuming we get bumps on the ASICs - Pactech machine or already bumped by IBM/external bumping services – we still need a solderable pad on the sensor!

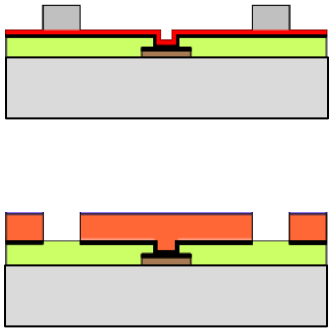
-: two options:

a. coined gold studs directly on Alu
b. Landing pad Cu/Sn by electroplating at HLL

-: for PXD6 we have to use option a.

→ if this works, it can well be used also for the final run

-: but keep option b. open, it is effectively a 3rd metal layer, which we might need at the end

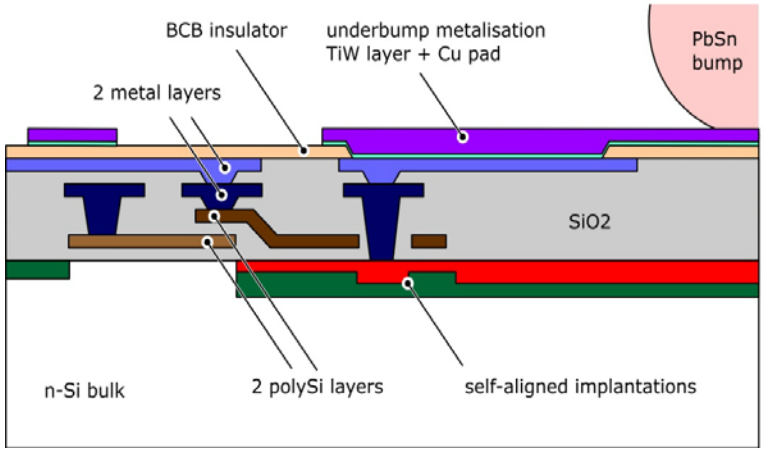


Sputtering
TiW barrier 50nm
Cu seedlayer 100nm

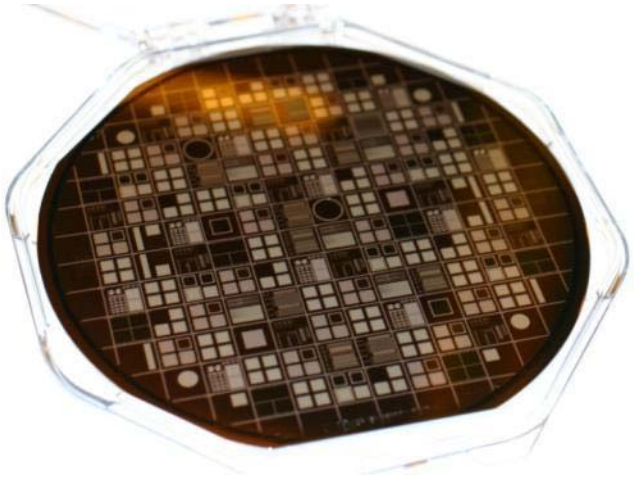
Litho
Insulation trenches

Plating module
Cu 5µm

Resist strip
Wet etch seedlayer & barrier



Small Project with CNM → Cu layer on HLL test diodes



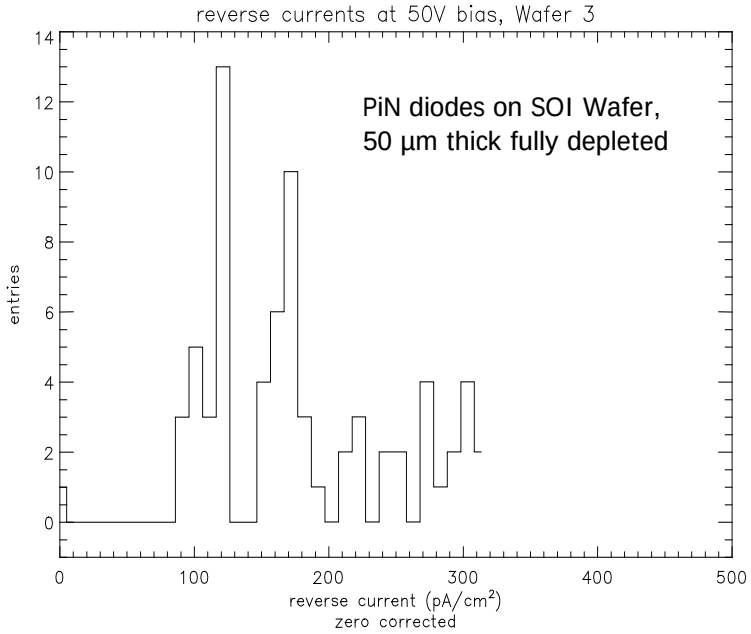
✓ at HLL:

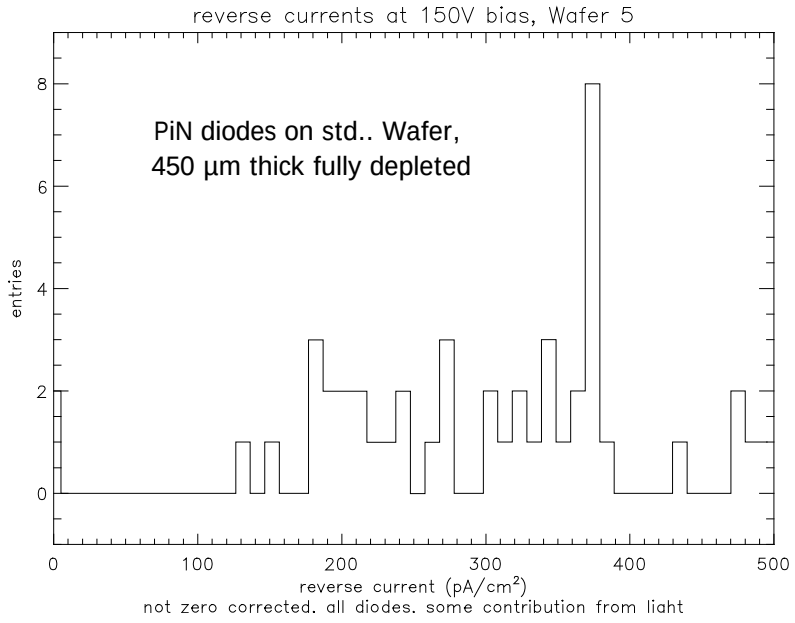
a. Pre-processing of 3 SOI and 3 Std. up to BCB openings
PiN Diodes, MOS Caps. many test structures for:
- design rules
- contact and sheet resistance
- contact "chains"

b. characterization before Cu

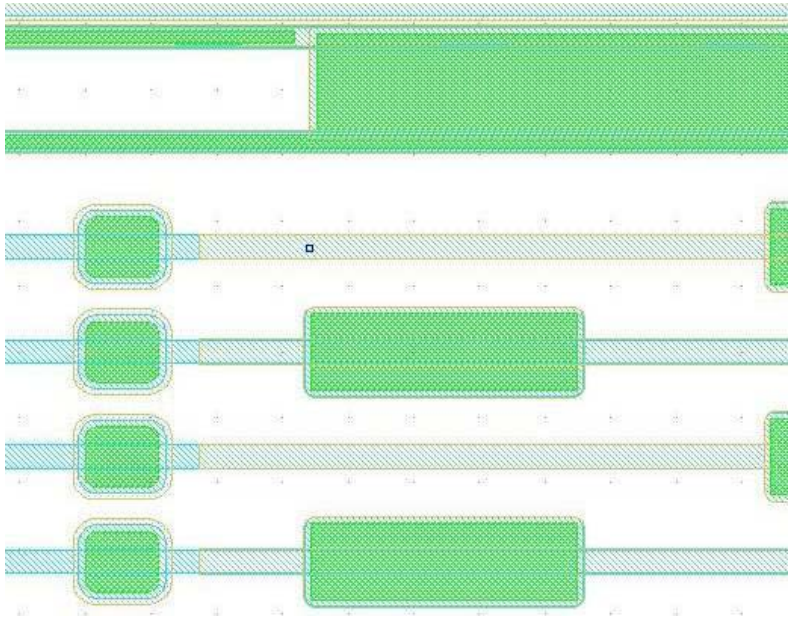
-: at CNM, Barcelona :

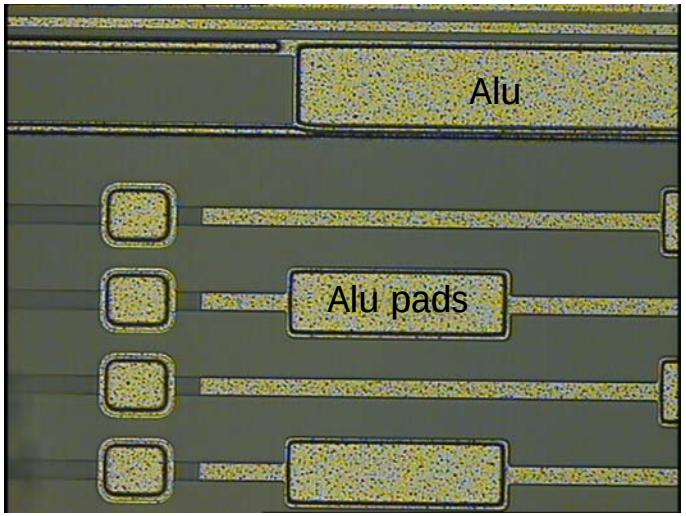
✓
a. sputter barrier and seed layer
b. thru mask electroplating of Cu → **ongoing**

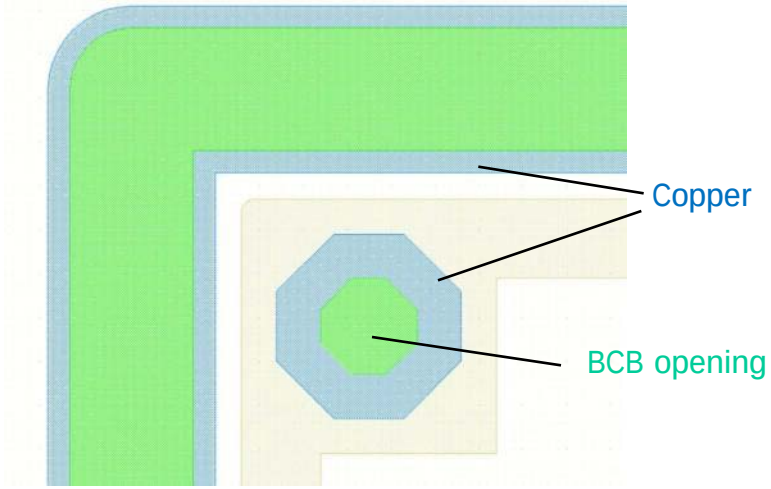


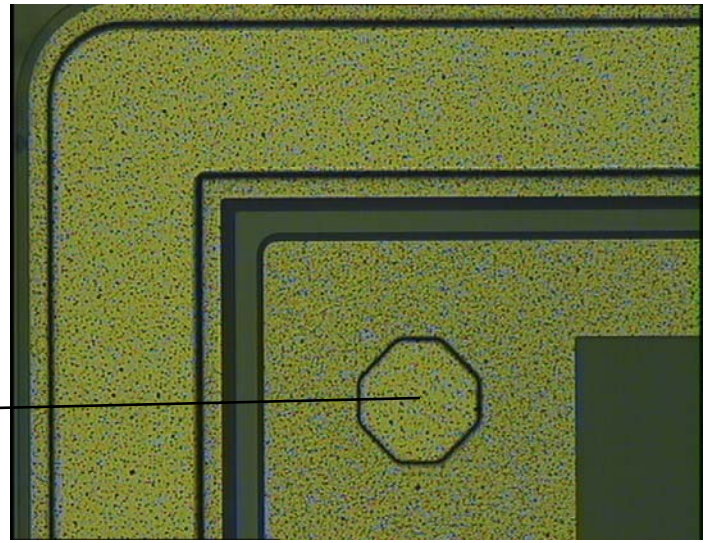


A few details: mask and real world







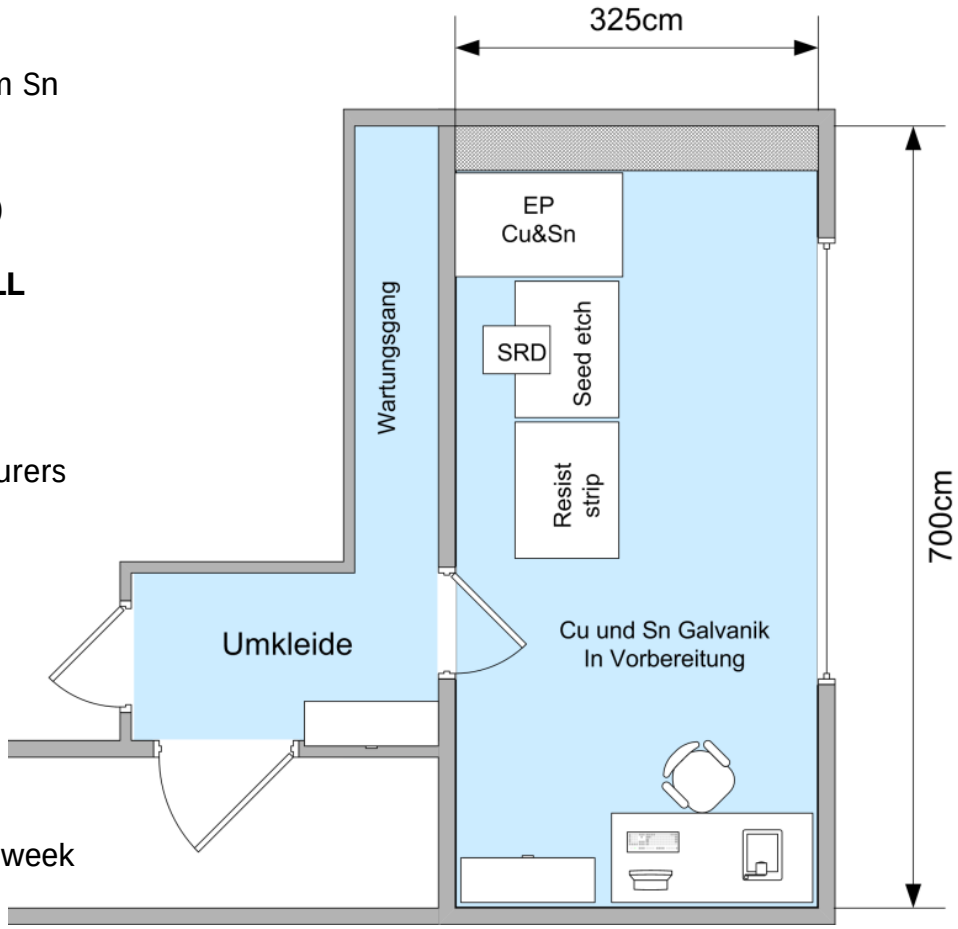


UBM Process

1. Sputter Ti:W und Cu (externally at the beginning)

2. Lithography: thick photo resist
3. Thru mask EP: 3-5 um Cu, ca. 2-3 um Sn
4. Resist strip
5. wet etch Cu
6. Wet etch Ti:W: H2O2 (with additives)

→ install step 2.-6. at HLL



Result after....

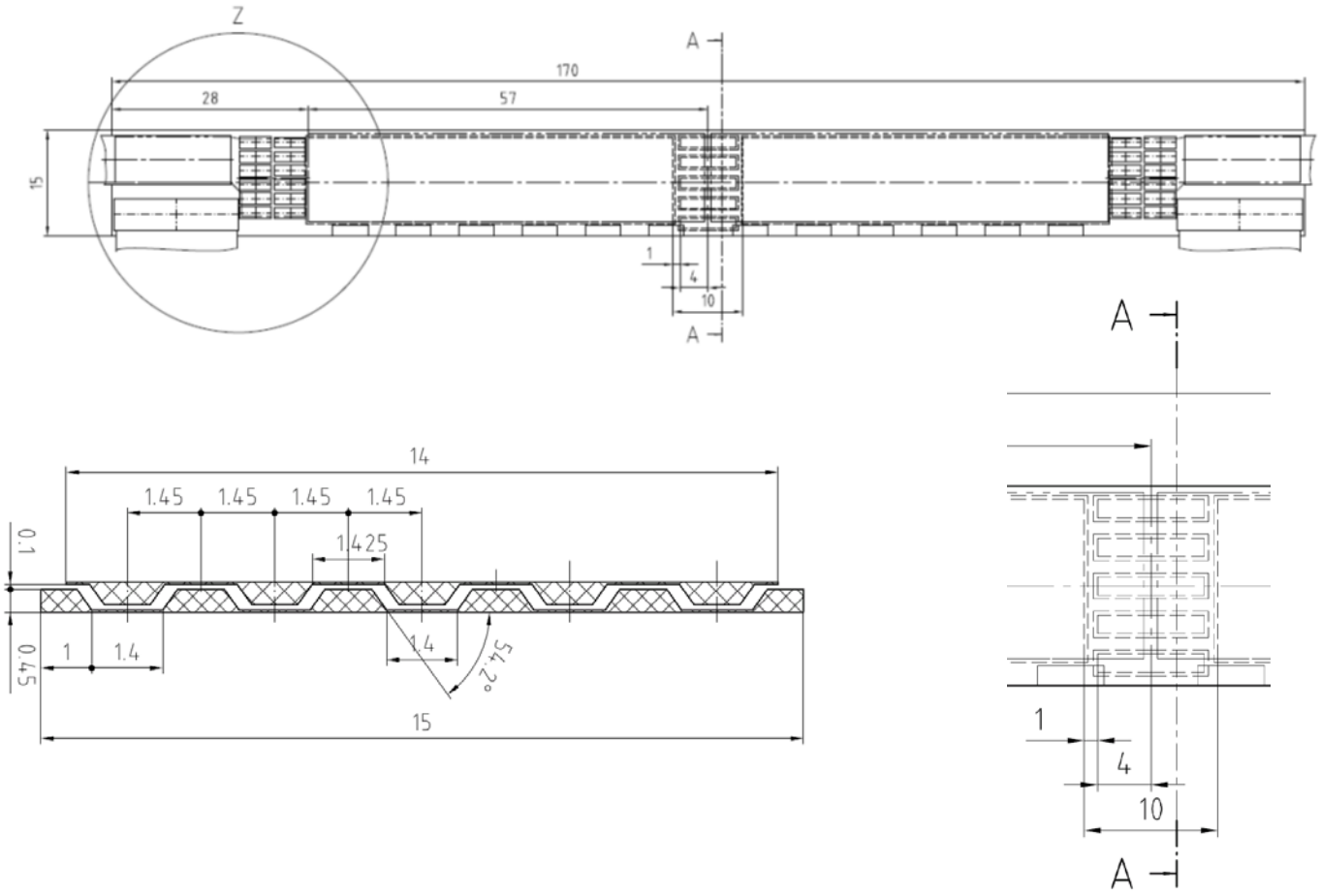
-: a lot of discussions with two equipment manufacturers
-: consultation of process experts and chemical suppliers for electro-plating

→ Fountain plater for Cu and Sn,
→ etch baths for seed layer removal,
→ solvent wet bench

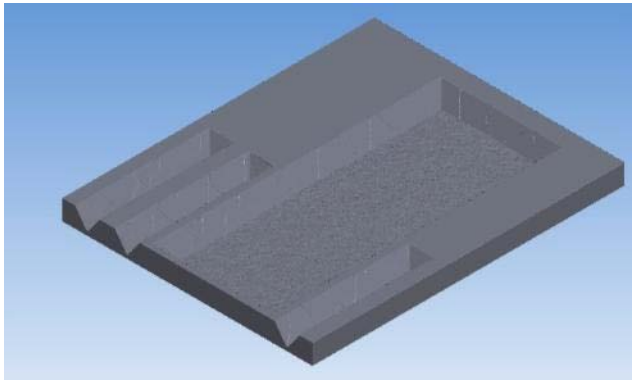
Status: - configuration and negotiations finished
- formal "call for bids" to be sent out next week
- delivery early 2010

Start Process installation Q1 2010

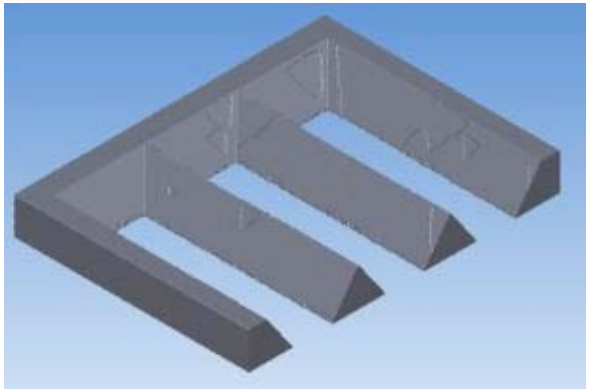
Current ladder design (V06a) → joint in layer 2

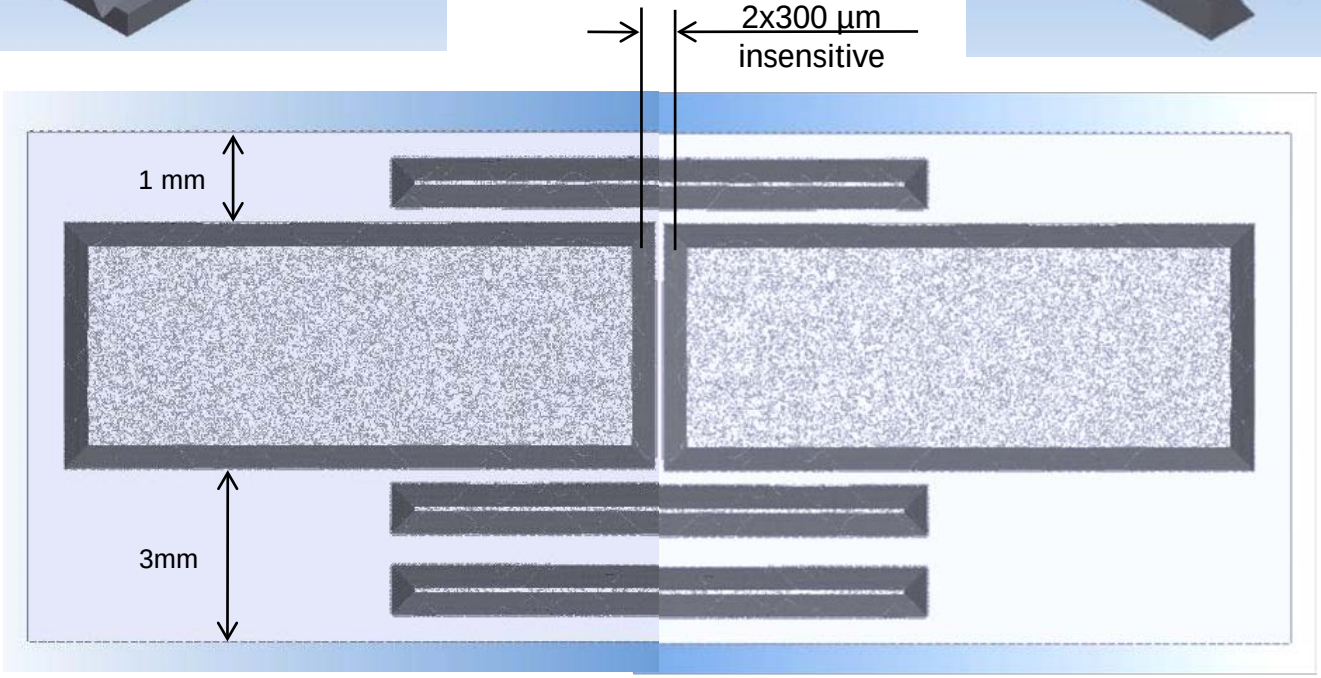


joint in layer 2 → new proposal



Low-mass joint between two Ladders at the second layer of Belle II PXD...



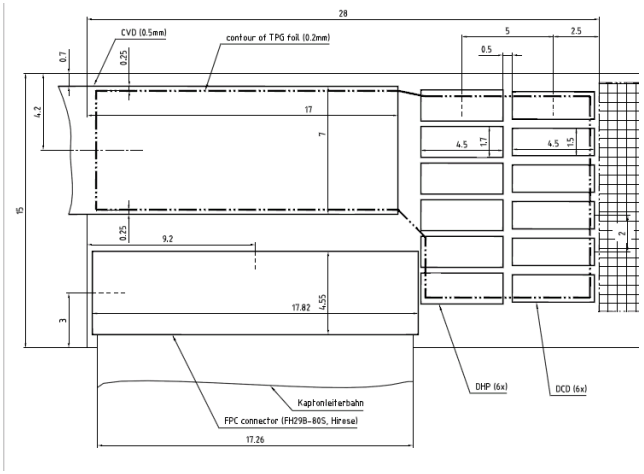


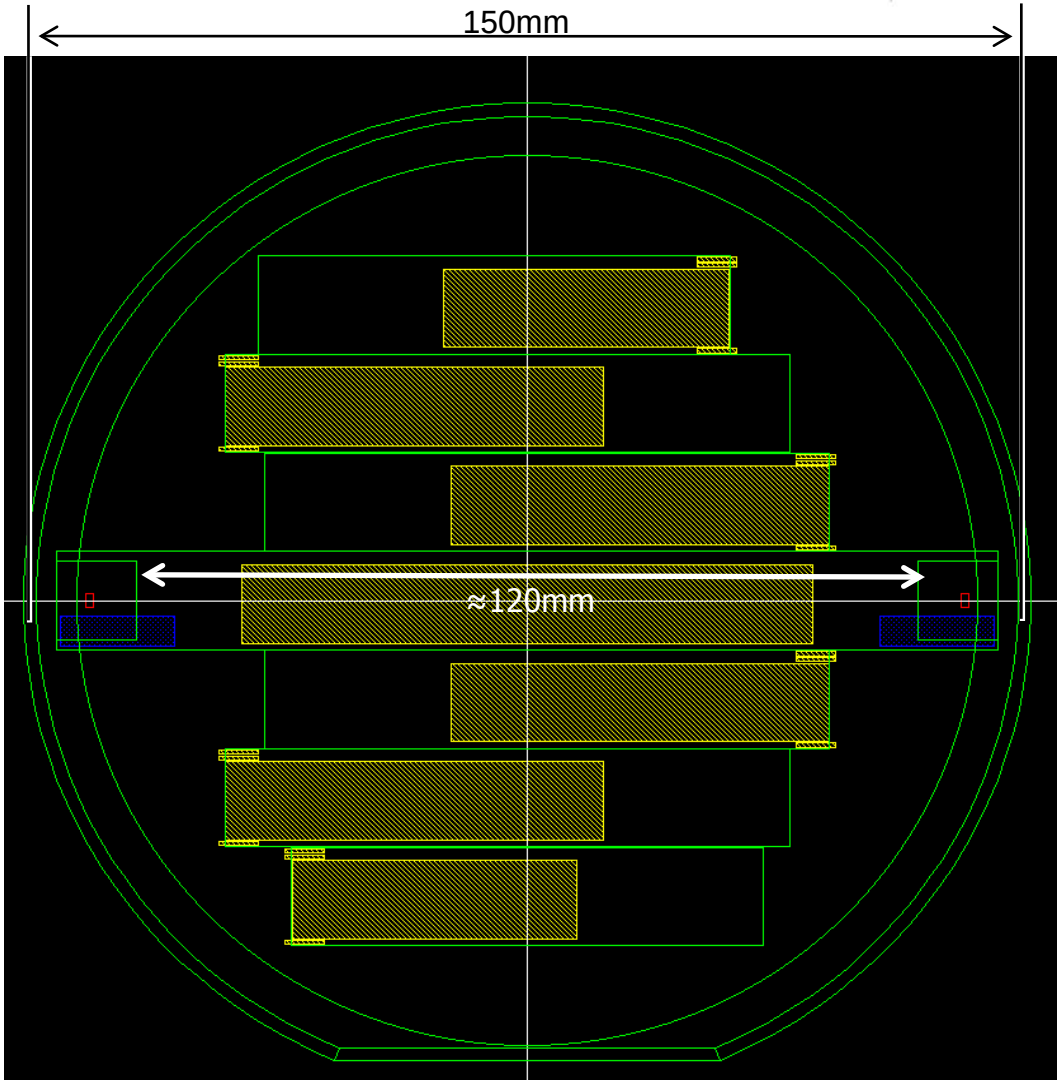
Would this be acceptable in the first layer also???

Current ladder design (V06a)

→ length of layer 1: 142 mm!!!
→ with metal traces for connector

Because of alignment structures metal layers only possible for ≈ 120 mm, Ladder can be longer, but no structured metal beyond ±60 mm from center !





→ Hans: Table of Signals and Supplies

	name	type	voltage [V]	current [mA]	comment	diff.	thin	thic	k
digital signals	GCK	LVDS in				1			
	FCK	LVDS in				1			
	TRG	LVDS in				1			
	RST	LVCMOS in					1		
	TMS	LVCMOS in					1		
	TDI	LVCMOS in					1		
	TCK	LVCMOS in					1		
	TDO	LVCMOS out					1		
	DO[5:0]	CML out				6			
power supplies	VDDA	DCD analog	1,8	600	sense line		1		6
DCD	VDDD	DCD digital	1,8	250	sense line		1		2
	REFIN	DCD analog ref	1,1	100	sense line		1		2
	DGND	common digital ground	0	1000	sense line		1		10
	AGND	analog ground	0	600	sense line		1		6
DHP	VDDIO	DHP IO rail	1,8	100	sense line		1		2
	VDDC	DHP core	1	500	sense line		1		5
SWITCHER	VDDS	digital supply	3,3	10	sense line?				1
	AVDDS	analog supply ?	20	?	sense line?				2
bias voltages	Vclear_on	clear on	~0				1		
	Vclear_off	clear off	~1				1		
	Vgate_on	gate on	~2				1		
	Vgate_off	gate off	~3				1		
	Vsource	source	7	30			1		1
	Vccg	common clear gate	~0				1		
	Vbulk	bulk	10				1		
	Vbias	backplane	-20				1		
					number of signal pins:	18	20	37	
					total sum:				75

23 digital signals

42 Power lines incl. sense lines

10 sensor bias

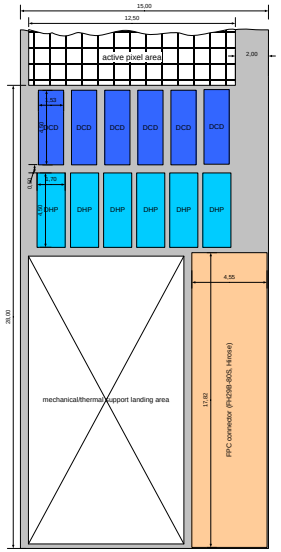
preliminary list, included sense lines

not included yet:

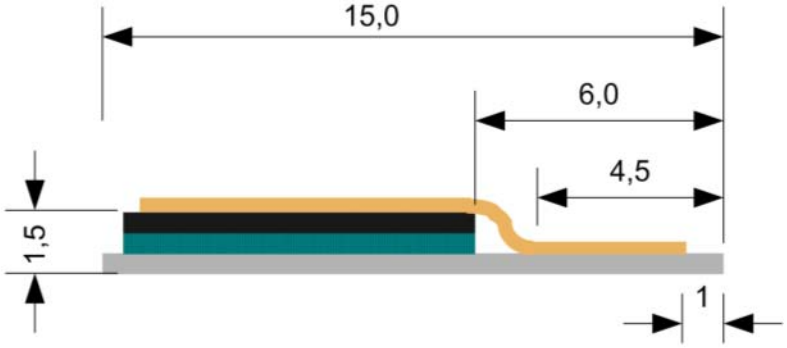
- NTC
- JTAG with LVDS instead of LVCMOS
- Vedge for DEPFET matrix

➔minimum requirement: 75 contacts

➔ Hirose 80 pin conn. with l ≈ 18 mm



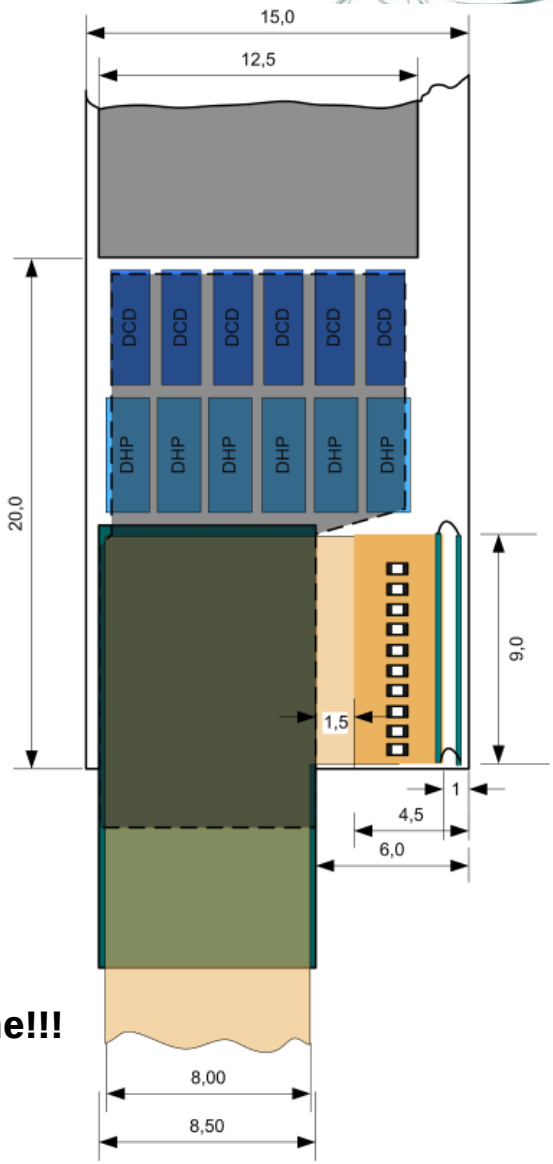
End of Stave: Connector??←→Flex lead??



-: Custom made multi-Layer std. Cu flex cable with
"several" power and ground layers
-: bendable 2x90° over 1.5 mm lateral and
vertical
-: wire bond pads on one end (Au or Ni)
min. pitch 100 µm (staggered??), 80 pins
-: connector (flex-flex??) at the far end
-: solderable pads for passive components

-: what bond wire diameter??? And many more questions …

→ **Contact flex hybrid supplier (Dyconex etc.)**



EOS: 28→20 mm, L: 142 → 126 mm with 86 mm sensitive

If we reduce the sensitive length from 86 to 80 mm ,we are done!!!

Is this possible???

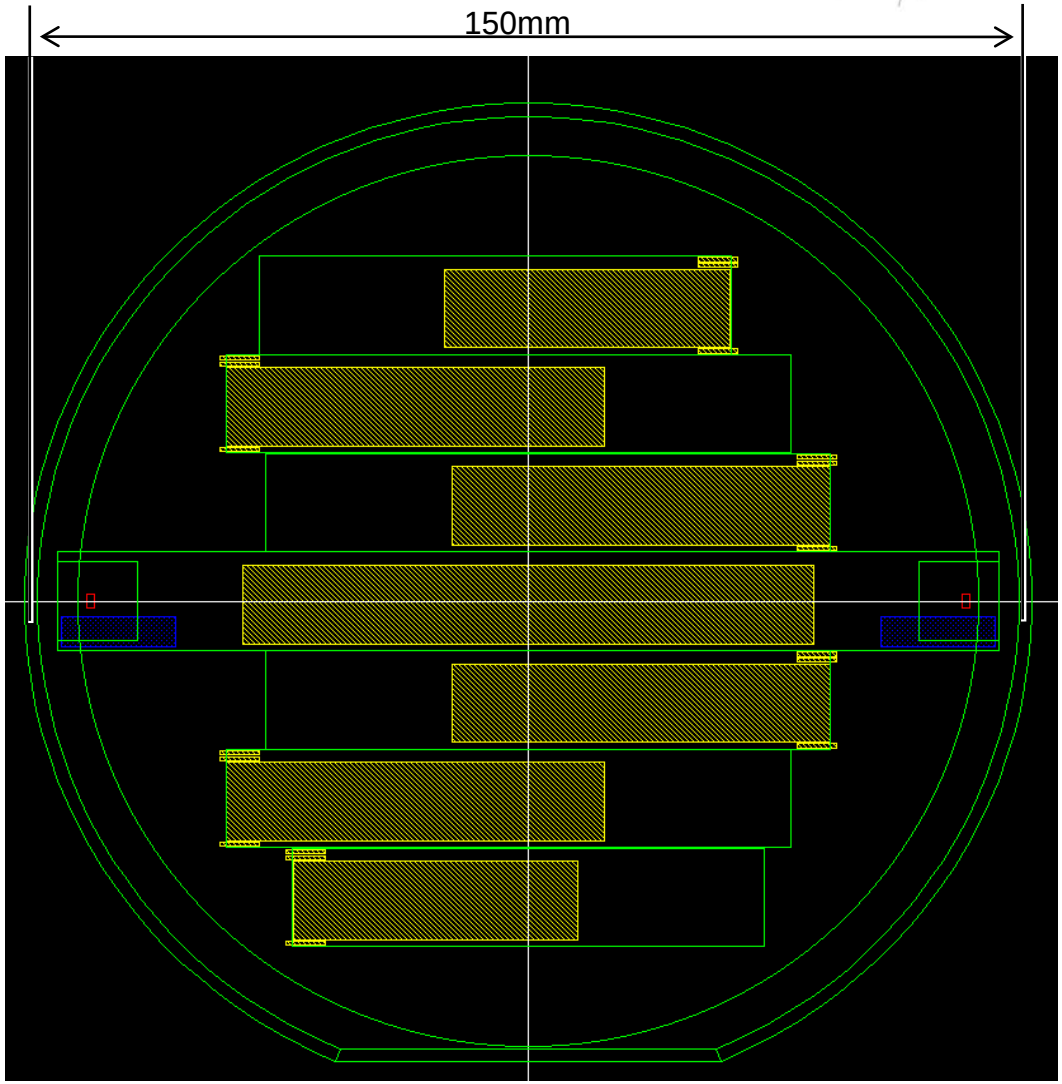
Finally, for the dummies:

We are ready:

-: metalized mechanical grade are in the cup board

-: as soon as we have defined the dimensions, I could start with the masks (together with Christian..)

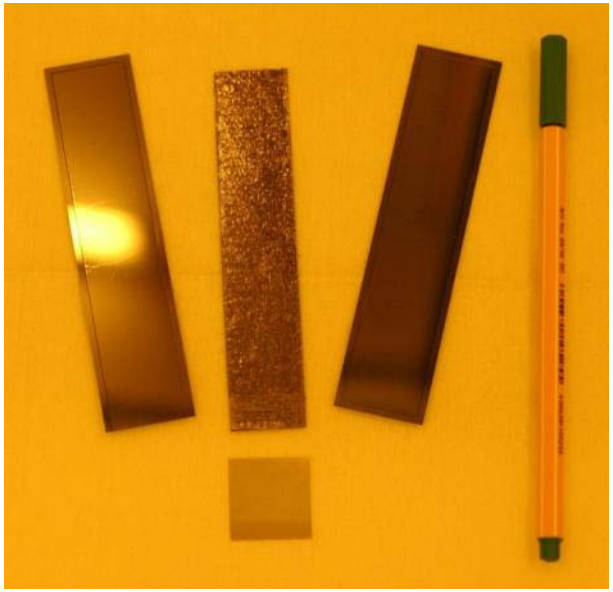
-: By the end of this year we could have dummies, both for electrical and thermo-mechanical tests

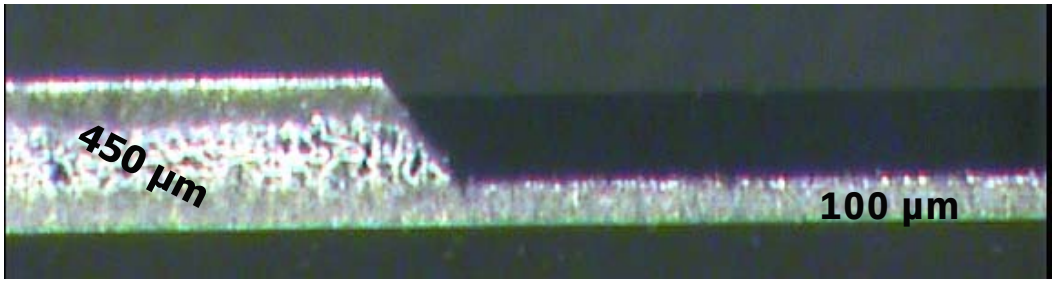


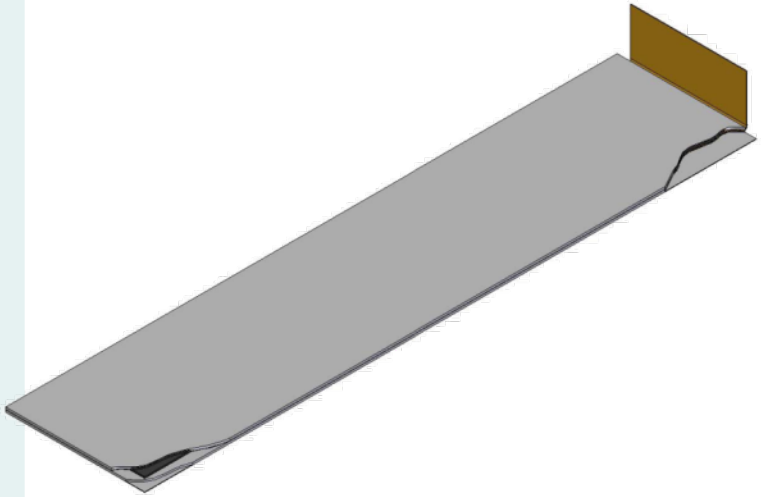
Backup slides follow

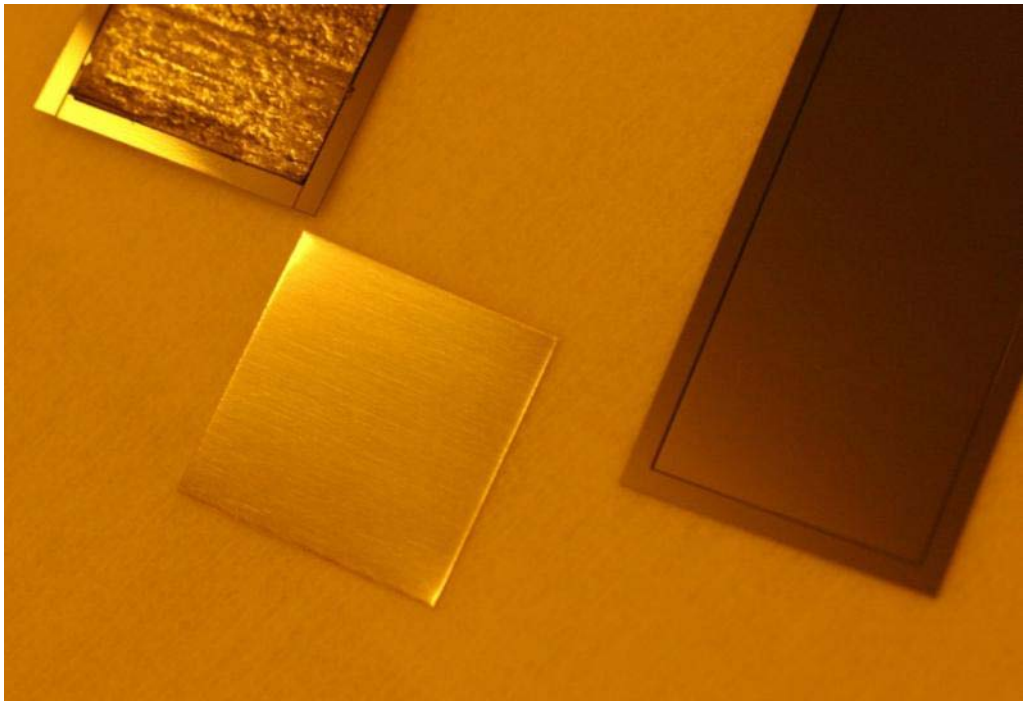

ELECTROPLATING
RENA

Silicon – TCPG Sandwich

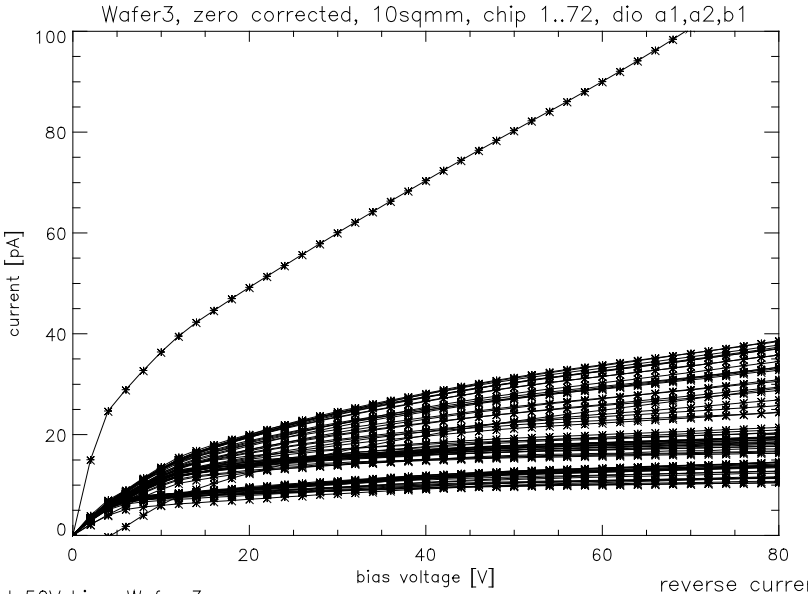








IV before Cu



SOI Wafer,
10mm2 diodes,
50 µm thick,
fully depleted at 50 V