

# Data Handling Hub Readiness for Phase 3

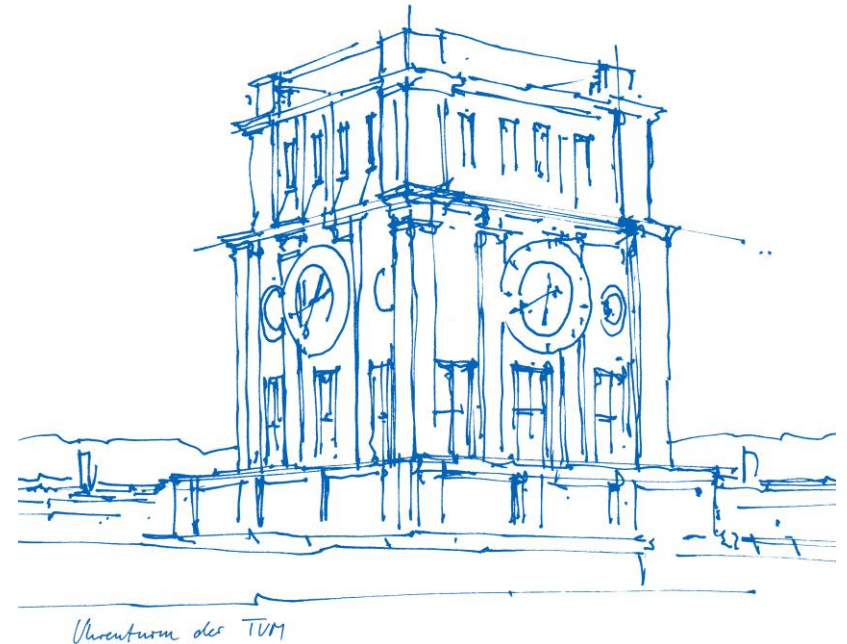
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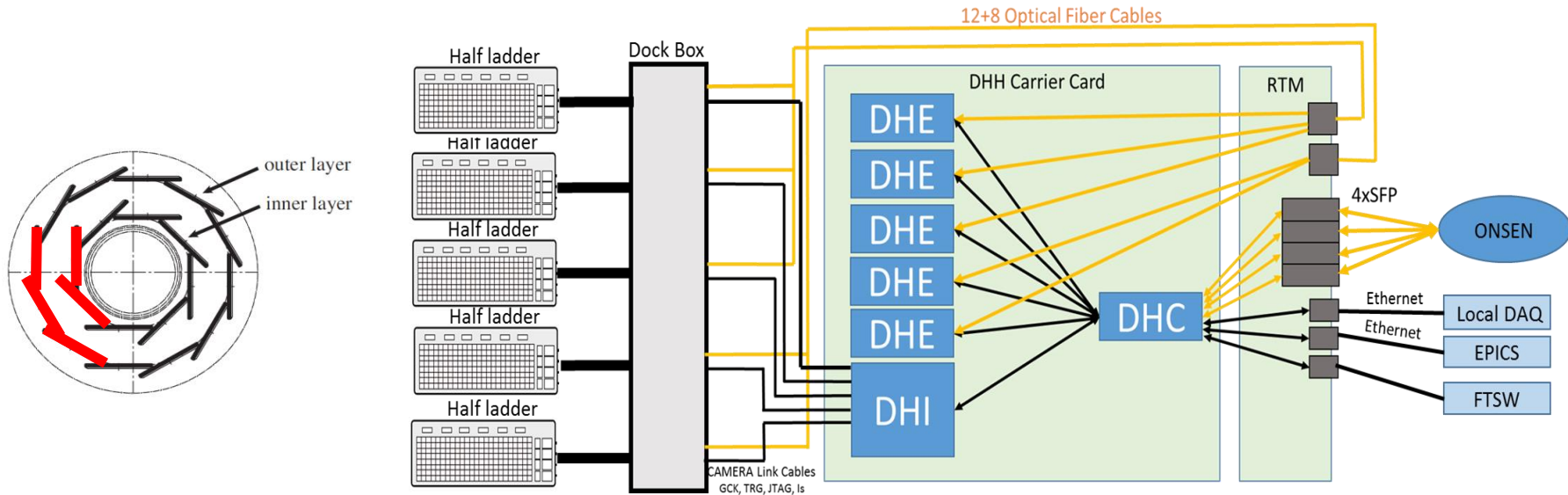
TUM Department of Physics

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# DHH System



DHI – Data Handling Isolator, Module Control JTAG, GCK, FCK, Short Reset

DHE – Data Handling Engine, Data Processing : data buffering in DDR3, event formation, Subevent building

DHC – Data Handling Control, Interface between external and DHE, DHI; Subevent building, Event distribution between four ONSSEN modules

# DHI

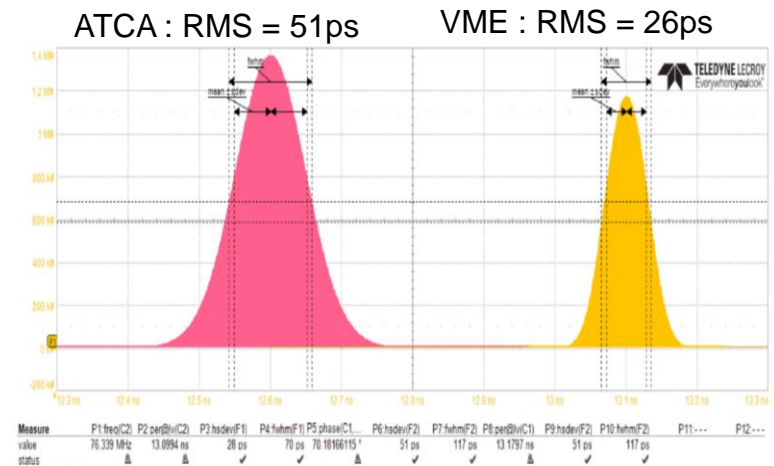
## Hardware issues:

- Performance of SiLab Clock Cleaner chip degraded in ATCA and to compare to DHE;
- Sporadically produces clock signal with too short periods
- Problem originated in switching DC/DC converters

**Cause** : state machines go out of sync

**Solution** : Optimized configuration of blocking capacitors on power lines, implemented in all DHIs at KEK. Still one DHI had to be exchanged to cure the problem

For new production of DHI we will redesign the power section



## Firmware

- Implemented safe logic to produce 76MHz clock out of 127MHz without glitches : DHI\_20181130\_1556 version
- Included new PVs to monitor clock stability : DHI\_20181213\_1621 version
- Change of reset procedure to avoid drop of HS links at start of run, it will be released with Overlapping trigger DHE firmware

## Problems at KEK with latest DHI firmware :

- Some DCD parameters were not correctly written
- problem was not reproduced at DESY

# DHE I

## Hardware

- In December DDR3 SODIMMs were installed and tested in all DHE modules at KEK

## Overlapping trigger firmware:

Firmware test at KEK in December showed following problems:

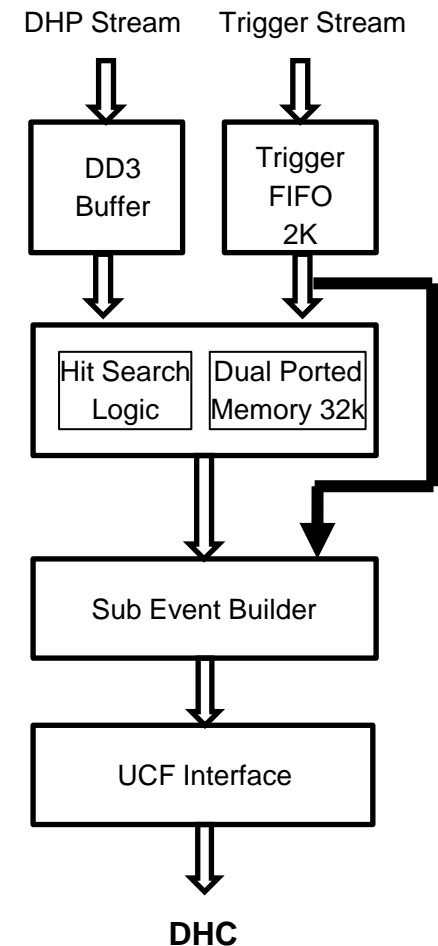
- Unstable synchronization with DHPT phase, for verification requires hit pattern when each gate has a hit;
- DHE32, DHE42, DHE52 and DHE62 were not delivering data in Zero Suppressed mode;
- HS links drop at start of run;
- Statistic information was not working.

Debugging loop procedure :

- Problem reproduced in lab ;
- Reproduced in simulation and fixed;
- System test;

Status :

- Unstable initial synchronization was caused by using not synchronized clock of 76MHz - fixed;
- HS links drop at start of run were caused by additional reset signal issued by DHI during start up procedure. Reset procedure was changed in DHI firmware;
- Problem with Statistic information was also caused by wrong phase of 76 MHz clock;



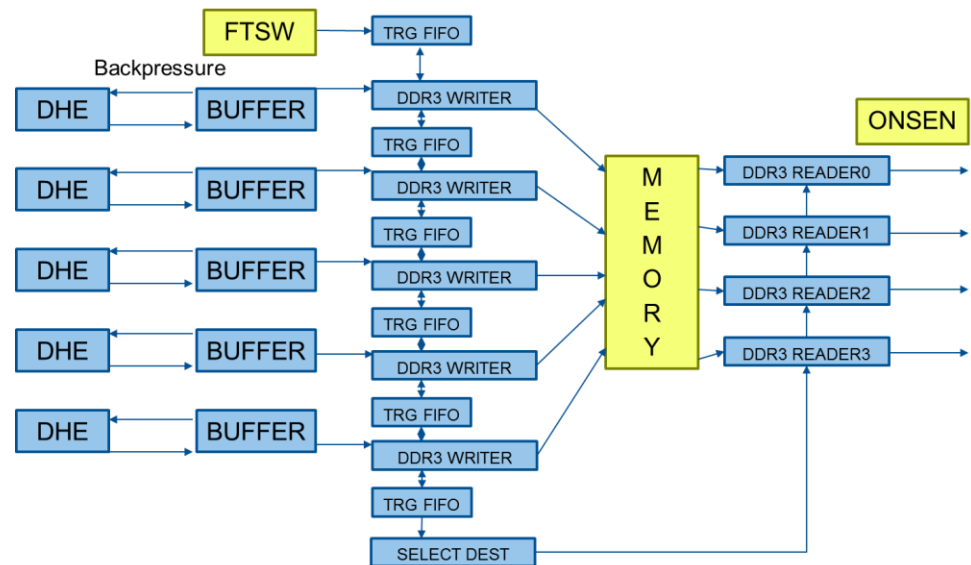
# DHE II

Tests performed so far:

- Propagation of Data flow back pressure (last Friday at DESY).  
Data loss problem observed. It was reproduced in simulation and fixed.
- Propagation of Trigger chain back pressure in DHE.  
Problem observed during long term tests: data flow get stuck . It was reproduced in simulation and caused by lock state of one FSM and fixed

# DHC

- Firmware had problem which were caused by Clock Domain Crossing constrains.
- Problem was fixed by tight timing constrains.
- Stefan developed ONSEN emulator for testing event distribution.
- The test still to be performed.



# Plans

- Complete DHE firmware test at TUM and then at DESY using existing DHC firmware!
- Test to be performed with employed DHC firmware at KEK
- This configuration will be sufficient for phase 3
- Test of final version of DHC firmware with DHE overlapping firmware at DESY
- Commission final DHC and DHE firmware versions at KEK

THANK YOU