# Phase 3 readiness: Software and Scripts

Felix J. Mueller





### Lab Framework

- The framework was already improved a lot during BEAST
- We decided to improve the frame work before phase 3
  - Follow the coding guidelines
  - Use the new abstraction layer with DHE class
  - Merge feature branches for lab setups and Beast into master
- Standard calibration scripts were modified
  - HS-link scan, Pedestal scan, Delay scan, Offset calibration (offset image)
  - Request for offset-delays, sample point, dcd adc and iv-curve
- Parallel processing is used in the measurement, analysis and upload of the data (except delay)
- Tested with lab setup at Munich and DHH setups at DESY, KEK
- GUI for calibration (CalibrationIOC) and data taking (elog\_server)





## **Lab Framework - Problems**

- Time for execution of calibration scripts at DESY with 4 modules and default settings
  - Pedestal scan ~ 2.5 minutes
  - Delay scan ~ 5 minutes
  - Offset calibration ~ 30 minutes
- Analysis of offset data for 20 modules is too much for BonndaqPC
  - Reduce parallelism (one process for every ASIC)
  - Reduce necessary CPU load for each analysis
- Largest problem is the parallel upload of pedestal and offset data
  - Parallelism needed because of long upload time
  - Pedestal upload takes too much CPU load
    - Florian and Michael are working on the problem
    - First implemented fix looks promising but more testing needed

### **IOCs**

- In general the IOCs work fine but problems have been seen only at KEK
- Felix mentioned problems with the utilityIOC, I fixed that yesterday
- Dhh-sequence IOC main problems:
  - Sometimes the sequence gets stuck at initializing JTAG, enabling DCDs, activating switcher outputs
  - Offsets are wrongly uploaded with dhh-sequence
    - We are trying to identify the problem
  - Verification of the switcher sequence does not seem to work properly
    - The switcher sequence is uploaded and read back for verification
    - If the check fails the switcher sequence is uploaded again
    - Apparently the switcher sequence is verified but is still not correct
      - Maybe a problem of the input data from DB?
      - Observed None values in PV dump and wrong offsets on/off values in PV readings
    - Severe problem since potentially harmful for switcher and DEPFET matrix
    - Unknown if same problem exist for gated mode sequence

## **Alarm System**

- We had a short meeting discussing the task
- Everybody should be aware of the alarm system
- For details https://indico.mpp.mpg.de/event/6182/contribution/2/material/slides/0.pdf
- Needs input from every expert and operator
- List of alarms:
  - https://confluence.desy.de/display/BI/PXD+Alarms+in+CS-Studio