Efficiency Measurements of final PXD9 Half-Ladders in Test Beams

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Belle II

DEPFET

Active Pixel Detector

1 7 3 7

Bundesministerium
für Bildung
und Forschung

Introduction

- What is the efficiency (charged track generating a hit) of final PXD9 half-ladders?
  - optimal efficiency of well working pixels
  - overall efficiency including dead/hot/inefficient pixels
- How to optimize the DHP zero-suppression threshold?
- In-pixel homogeneity of charge collection (drift paths, biasing) and efficiency?
- Effects of non-optimal biasing?
  - biasing optimization strategy
  - sensitivity to bulk damage, etc. $\rightarrow$ stability of biasing condition

Devices under test

Beam Test 2018 (DESY)

- W11_OF2
  - several dead drain lines
  - grade C: 97.4 % alive
- W40_IF
  - "Göttingen guinea pig" cut ladder
  - 2 dead gates
  - grade A: 99.1 % alive
- W05_OB1
  - instable/faulty ASIC pair 3
  - grade A: 99.2 % alive

Beam Test 2019 (DESY)

- W05_OB1
  - γ-irradiated to 21 Mrad
  - re-optimized
  - 73.1 % alive
- W37_OF1
  - Phase2 module
  - re-optimized
  - grade A: 99.8 % alive

Track reconstruction

- using TBSW[1] framework by Benjamin
- Kalman filter based track fitting (telescope and front-end hits)
  - tracks require hit on each telescope and front-end plane
- extrapolate hit position to DUT plane
- match DUT cluster hits in 200 μm radius
- efficiency $\epsilon = \frac{\#\text{ tracks with matched cluster hit}}{\#\text{ tracks total}}$

[1] https://bitbucket.org/BenjaminSchwenker/tbsw/

Reconstruction: PXD specific remarks

- active link pixels
  - during TB18 observed instable HS-links on all 3 DUTs
  - "activate"[2] test pixel in each ASIC pair
  - neglect events with missing "link pixels"

  $\rightarrow$ remove in-efficiency due to dropped links
- good event flag
  - flag events without any format error[3] reported by BonnDAQ
  - skip events without good event flag
- DHP bug
  - last gate fully masked (pedestals = 255)

[2] setting pedestal value 0 $\rightarrow$ artificial hot pixel
[3] details by Florian

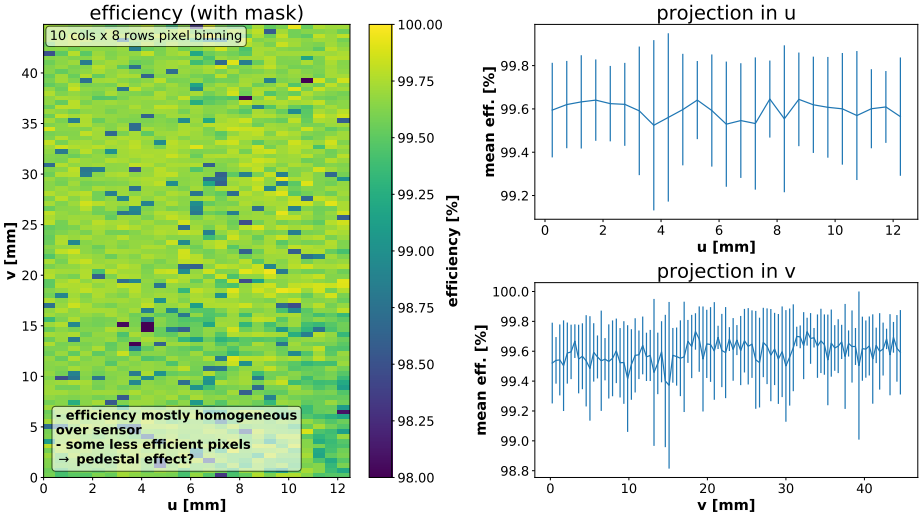
Efficiencies summary

- mass testing optimized configuration
- *real* efficiency: average efficiency of all (illuminated) pixels[4]
- *optimal* efficiency: excluding dead and hot pixels and nearest neighbours

half-ladder	optimal efficiency [%]	real efficiency [%]	comment
W11_OF2	99.612 ± 0.003	96.267 ± 0.007	several dead drain lines
W40_IF	99.580 ± 0.002	97.942 ± 0.004	2 dead gates
W05_OB1	99.655 ± 0.002	99.610 ± 0.003	dead ASIC pair 3
W05_OB1 irrad.	99.636 ± 0.002	92.835 ± 0.008	*see Harrisons talk*
W37_OF1 phase2	99.584 ± 0.002	99.560 ± 0.002	phase2 configuration
W37_OF1 re-opt.	99.551 ± 0.001	99.453 ± 0.001	2 half-dead drain lines

[4] up to 0.5 % in-efficiency due to masked last gate

Efficiency details: W40_IF optimal efficiency



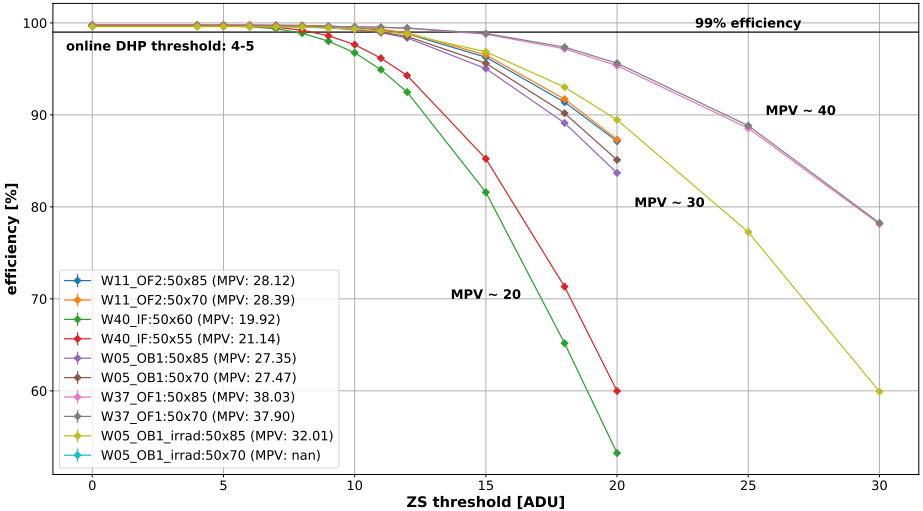
DHP zero-suppression threshold optimization

- higher zero-suppression threshold: cutting Landau charge distribution $\rightarrow$ efficiency loss

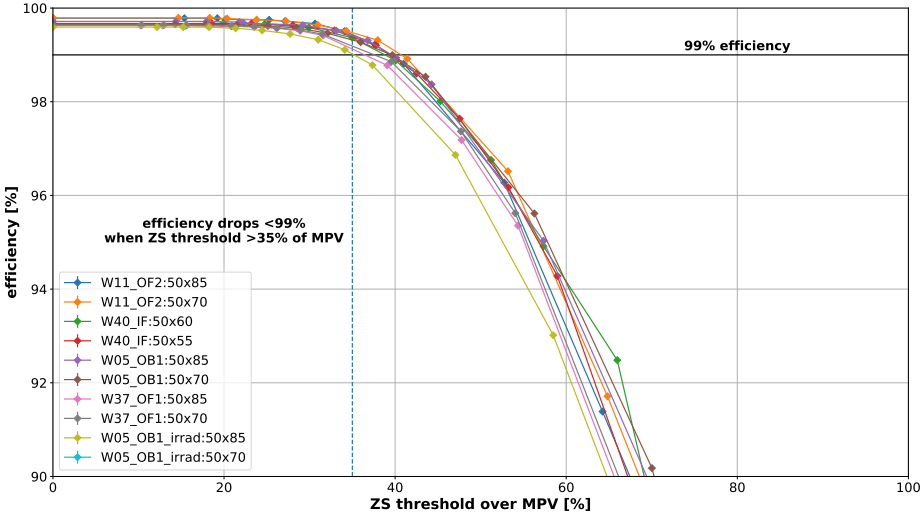
$\rightarrow$ What threshold leads to significant efficiency loss?

- offline pre-clustering zero-suppression (ZS) cut equivalent to higher online DHP threshold
- more relevant f.o.m. is threshold over Landau MPV ratio

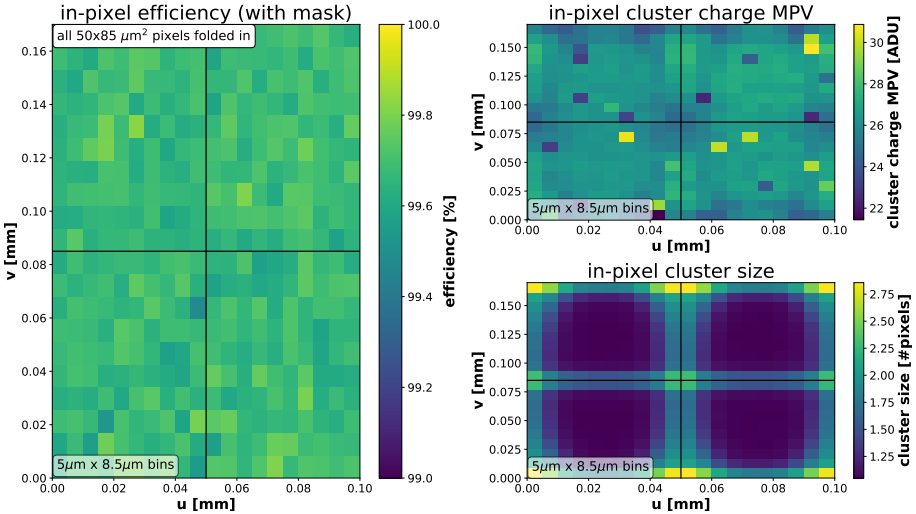
Efficiency vs ZS threshold



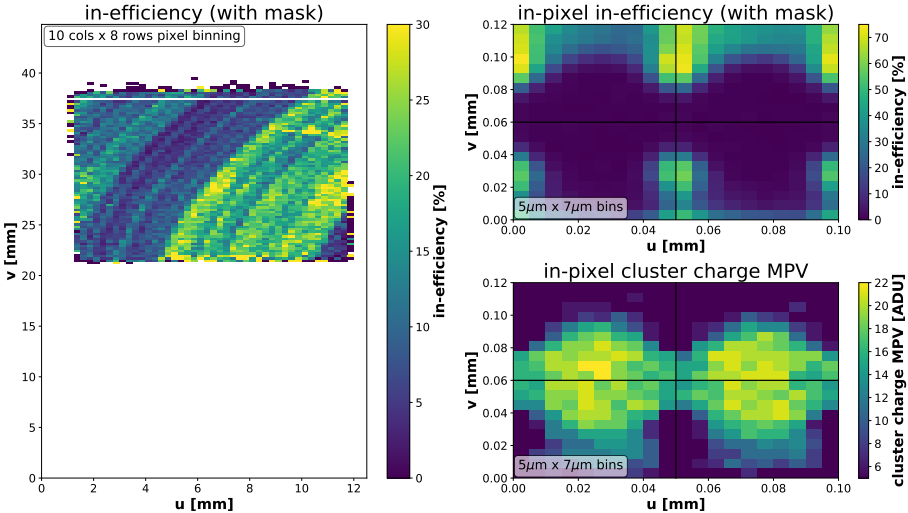
Efficiency vs threshold/MPV ratio



In-pixel homogeneity (W05_OB1 non-irrad., $50 \times 85\,\mu m^2$ pixels, 2×2 grid)



Non-optimal biasing effects (W40_IF, HV −66 V, drift −4 V, clear-off 5 V)

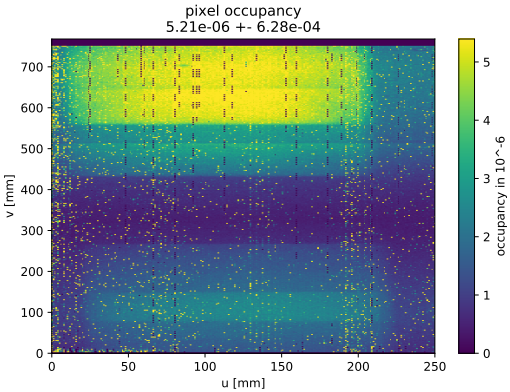


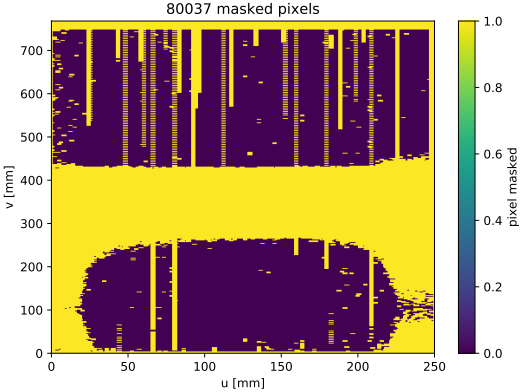
Conclusion & Outlook

- optimal efficiency about 99.6 % consistent for 4 different modules
  - no significant degradation due to γ-irradiation observed
  - up to 1 % in-efficiency due to dead pixels for grade A modules
  - up to 0.5 % in-efficiency due to last gate masked (DHP bug)
- source of ≈ 0.4 % inefficiency:
  - "optimal efficiency" $\rightarrow$ dead and hot pixels already excluded
  - track reconstruction? $\rightarrow$ study not-matched tracks in detail
  - intrinsic dead time due to clear: $t_{\text{clear}} \approx \frac{1}{4} t_{\text{gate}} \rightarrow 0.13$ % efficiency loss expected
  - low efficiency pixels? $\rightarrow$ bad pedestals? bad ADC curve region? charge collection?
- biasing stability
  - understanding in-pixel inefficient areas $\rightarrow$ layout of DEPFET structures
  - biasing variation $\rightarrow$ where does significant efficiency loss occur?

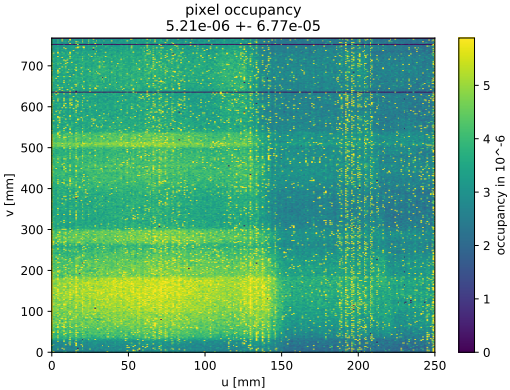
Backup

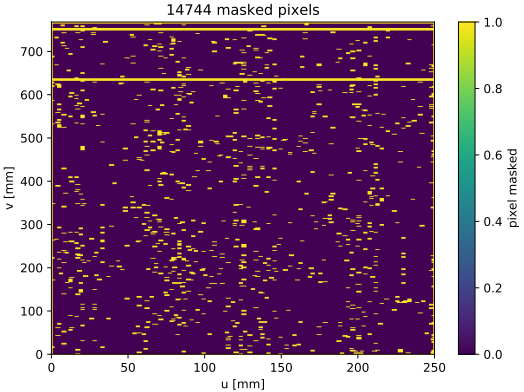
W11_OF2 occupancy and mask



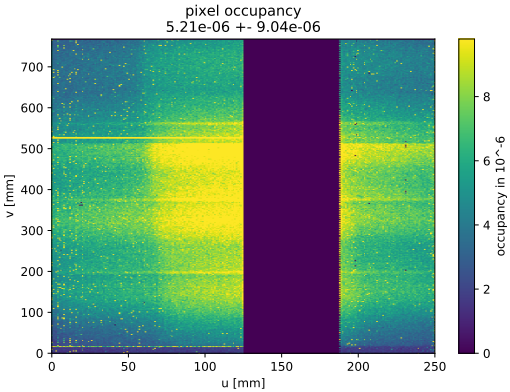


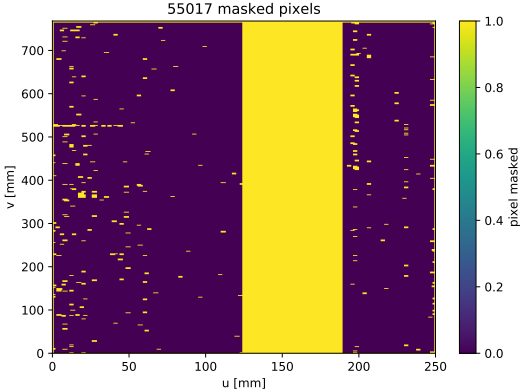
W40_IF occupancy and mask



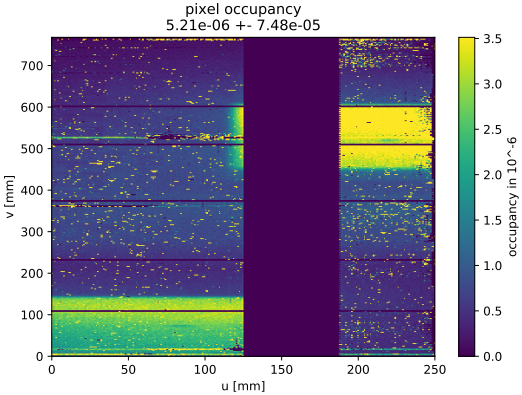


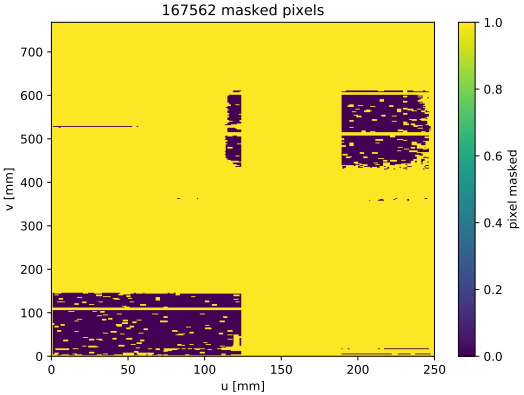
W05_OB1 (pre-irrad.) occupancy and mask



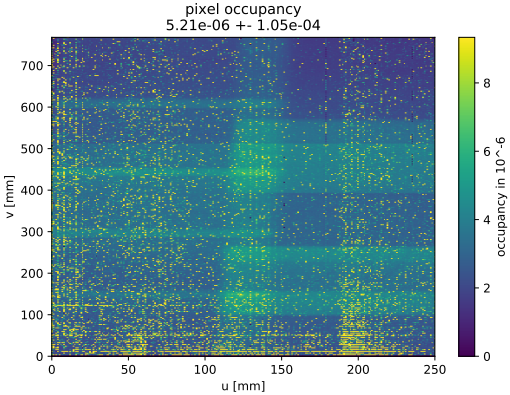


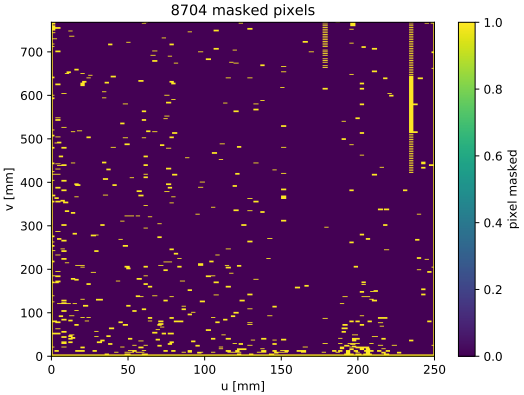
W05_OB1 (post-irrad.) occupancy and mask



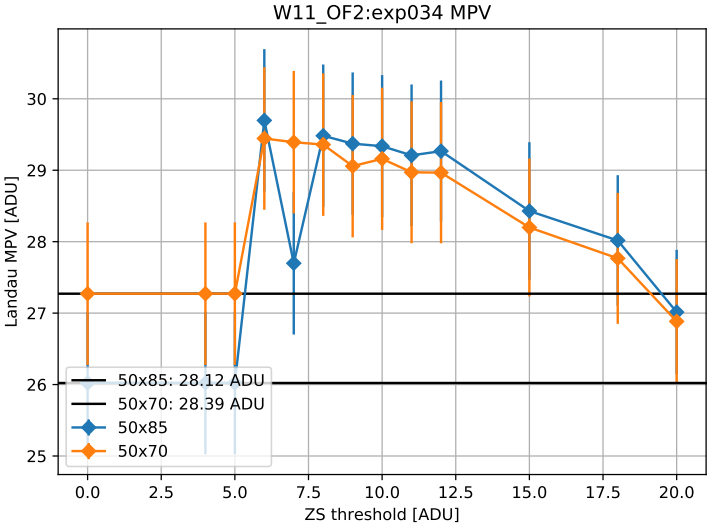


W37_OF1 occupancy and mask

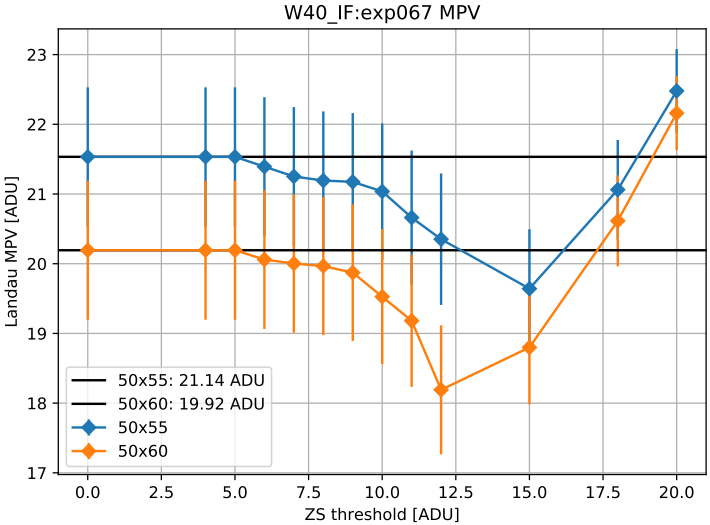
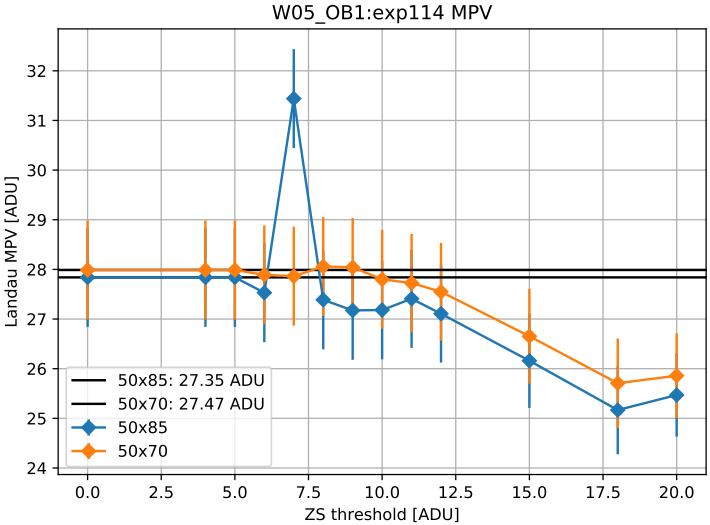




W11_OF2 cluster charge MPV



W40_IF cluster charge MPV



W05_OB1 cluster charge MPV