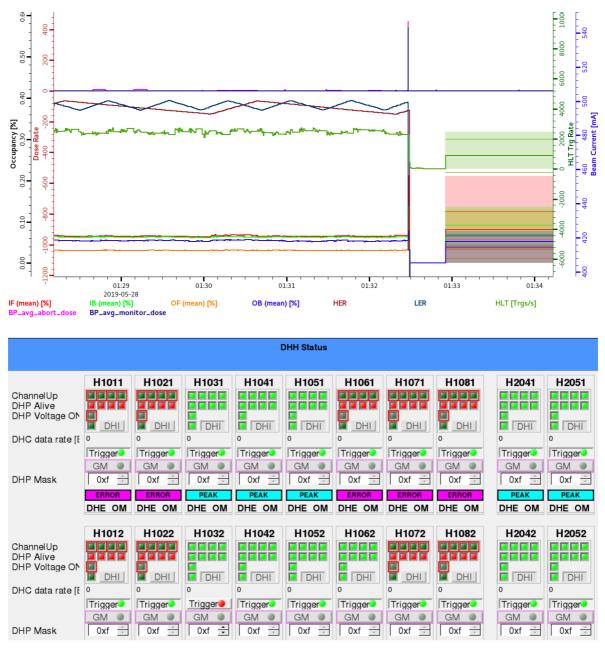
Note 2019.05.28

Owl shift,

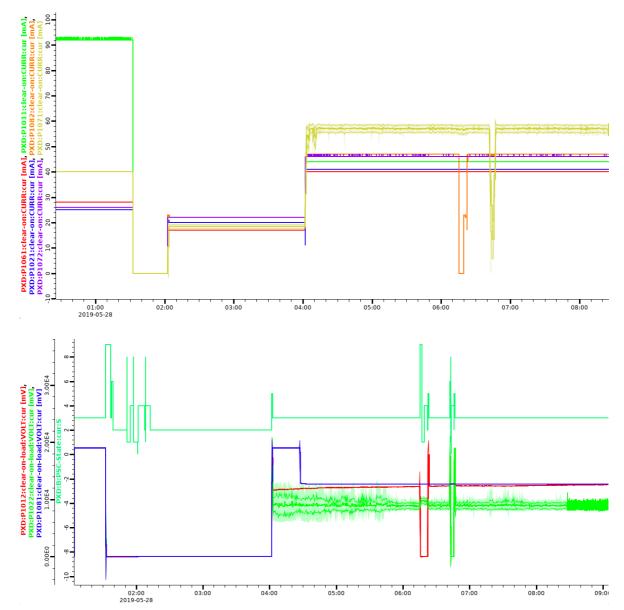
1:32am beam aborted, PXD emergency shutdown



3:50am BCG announced QCS power supply trouble need vendor's investigation, so no beam until today's evening at fastest.

Then H1012,1022,1081 high clear-on current, voltage does not reach the requested.

H1071 clear-on current at limit.



H1071,1022 were masked in data taking.

## Abnormal clear-on currents on:

H1082,1072,1022,1012,1081,1071, 1061,1021,1011

At 10:00

Reading Switcher IDCODE:

fine: 1011, 1081, 1031, 1021, 2042, 1071, 1051, 1061, 1041, 2052. (Sw -> ASIC4) not fine, reading fill pattern back (AAAAAAAA or 55555555): 2041, 1012, 1082, 1022, 1032, 2051, 1062, 1072, 1042, 1052 (Sw -> ASIC1). After enable dcd stag en in ASIC1, all sw IDCODE are correct.

## The sw-seq in DHP memory are correct.

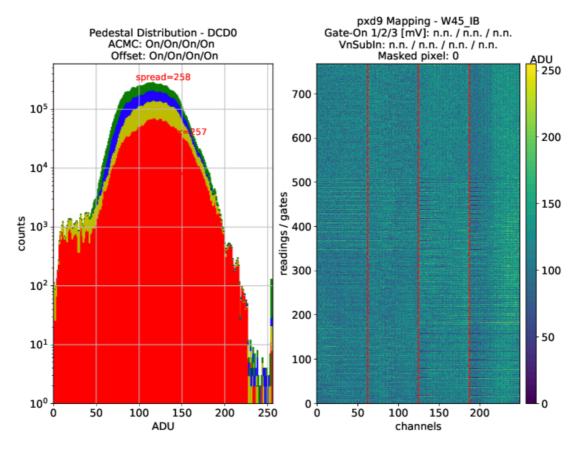
Adjust the clear-on/off current limits for several modules:

Set limits: clear-on 90, clear-off to 80mA, current reaches 83mA, -59mA, source 94mA. P1012 Limit: clear-on 80mA, currents reach 70mA, -49mA, source 69mA. P1081 Limit: clear-on100mA, currents reach 95mA, -26mA, source 83mA. P1071 Limit:clear-on 70mA, currents reach 60mA,-35mA, source 94mA.

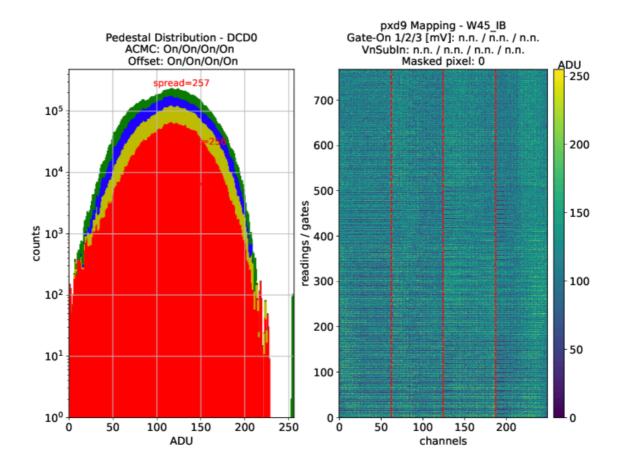
Taking pedestals, all works except H1071. https://elog.belle2.org/elog/PXD-Commissioning-KEK/4654 - 4672

## Pedestal changes, e.g. H1022:

Before



After



H1071

					PS Channel C	verview				P1072	P1081
PXD PS P1071 - Sensor 07 IF								P2071	P1061		
	. [			CY	Current State:	PEAK				Unit II Temp	D: 34 p: 27 degC
THERMAL				_							
UPS software reset											
DHI power 10	min.	Set Current	max.	min.	Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
sw-sub	0 mA	50 m A	50 m.A	-7100 mV	-7000 mV	0 mV		-7099 m V	-7009 m V	-22 mA	sw-sub
sw-dvdd	0 m.A	30 m A	40 m.A	0 mV	1800 mV	2000 mV		3046 m V	1801 m V	22 mA	sw-dvdd
sw-refin	0 m.A	30 mA	30 m.A	-7100 mV	-5200 mV	0 mV		-5237 mV	-5202 mV	0 m A	sw-refin
cd-amplow	0 mA	1300 mA	1400 mA	0 mV	300 mV	500 mV		1007 mV	299 m V	-696 mA	dcd-amplow
dcd-avdd	0 m A	3000 mA	3000 m.A	0 mV	1800 mV	2000 mV		5139 mV	1800 m V	2613 mA	dcd-avdd
dcd-dvdd	0 m A	940 mA	1000 mA	0 mV	1800 mV	2000 mV		3776 m V	1802 mV	846 m A	dcd-dvdd
dcd-refin	0 mA	1000 mA	1000 mA	0 mV	700 mV	1300 mV		2616 m V	701 m V	260 m A	dcd-refin
dhp-core	0 m.A	730 mA	800 m.A	0 mV	1200 mV	1640 mV		3255 mV	1198 mV	694 mA	dhp-core
dhp-io	0 m A	550 mA	550 m.A	0 mV	1800 mV	2000 mV		3595 mV	1802 mV	334 mA	dhp-io
buk	0 mA	10 mA	10 mA	0 mV	10000 mV	10000 mV		10005 mV	10004 mV	0 m A	buk
clear-on	0 mA	70 mA	100 m.A	0 mV	19000 mV	22000 mV		19177 mV	19022 mV	60 mA	clear-on
clear-off	0 mA	60 m A	100 mA	0 mV	4000 mV	20000 mV		3828 mV	3990 m V	-38 mA	clear-off
gate-on1	0 m.A	15 mA	30 m.A	-4000 mV	-3090 mV	5000 mV		-3165 mV	-3090 mV	-7 mA	gate-on1
gate-on2	0 m A	15 mA	30 m.A	-4000 mV	-3090 mV	5000 mV		-3160 mV	-3093 mV	-6 m A	gate-on2
gate-on3	0 mA	15 mA	30 m.A	-4000 mV	-3090 mV	5000 mV		-3169 mV	-3087 m V	-7 mA	gate-on3
gate-off	0 mA	40 mA	40 m.A	0 mV	5000 mV	6000 mV		5107 mV	5006 mV	26 m A	gate-off
source	0 m.A	120 mA	150 m.A	0 mV	6000 mV	7000 mV		7478 mV	6003 mV	93 mA	source
ccg1	0 mA	10 mA	10 mA	-5000 mV	0 mV	0 mV		-3 m V	-8 mV	0 m A	ccg1
ccg2	0 m A	10 mA	10 mA	-5000 mV	0 mV	0 mV	_	3 m V	3 m V	0 mA	ccg2
ccg3	0 mA	10 mA	10 m.A	-5000 mV	0 mV	0 mV	_	-3 mV	2 mV	0 m A	ccg3
hv	0 uA	600 uA	10000 uA	-80000 mV	-66000 mV	0 mV		-65955 mV	-65970 mV	-114 uA	hv
drift	0 mA	10 mA	10 mA	-6000 mV	-4000 mV	0 mV	_	-3996 mV	-4005 mV	0 mA	drift
guard	0 mA	. 10 mA	30 m.A	-6000 mV	-5000 mV	0 mV		-5003 mV	-5001 mV	0 m A	guard

The clear-on/off current is not stable, jumping from  $\,$  54 to 60mA / -38 to -34mA

Pedestals: https://elog.belle2.org/elog/PXD-Commissioning-KEK/4653.

Pedestal Calibration always failed using calibrationIOC, After manually upload the pedestals, high occupancy observed.

