

# PXD9-20: results from probe station measurements

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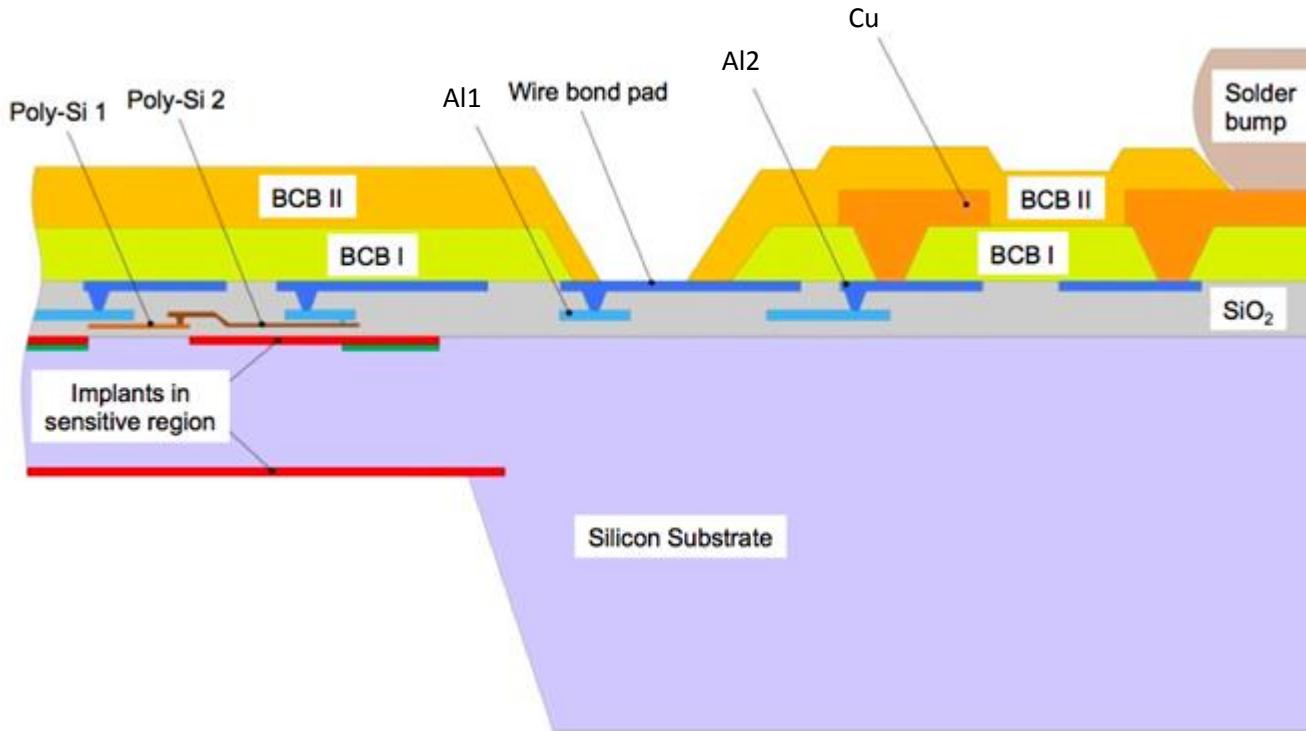
# Outline & Motivation

1. Short introduction to the device testing
2. Results
  - Global tests on the modules to get info on:
    1. Diode integrity (n+ & p+ region)
    2. Shorts in the polylines (Gate & ClearGate)
  - Tests of DEPFET transfer characteristics at one gate row to get info on:
    1. Opens (Drainlines)
    2. Shorts (Drainlines)
    3. Pedestal Currents and other Transistor characteristics

→ precise localisation of faulty drainlines  
→ possibility of rework in faulty areas



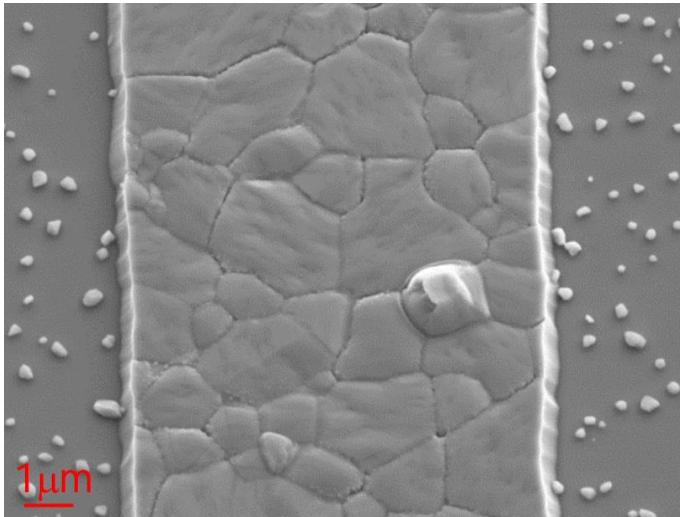
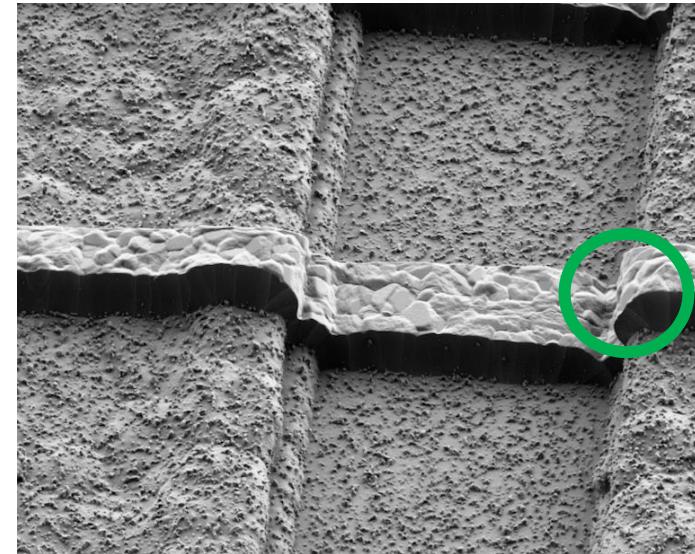
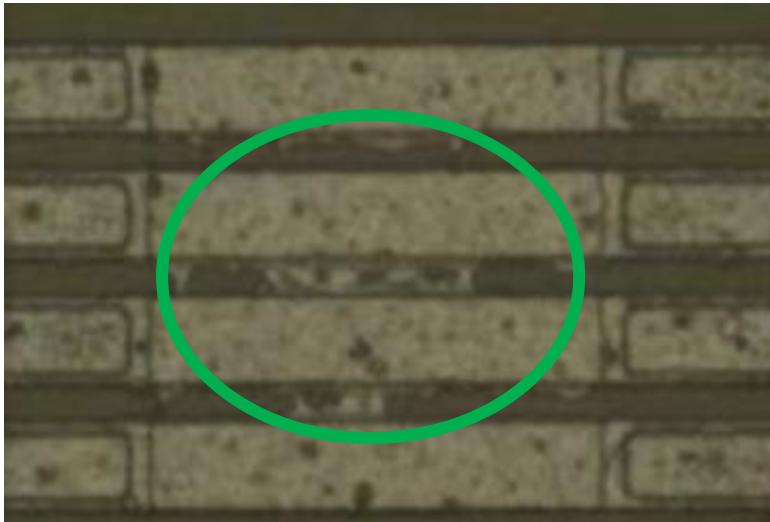
# Metallization



- Metallization done layer by layer with alternating of dielectric and routing material (Al1, Al2 and Cu)
- $\text{SiO}_2$  & BCB (BenzoCycloButene) as dielectrics between the layers
- Connection between the layers done per vias



# Defects



- Lateral shorts (Stringers)
- Discontinuities (Topographie)
- Hillocks
- Etching of contacts might lead to missing contacts
- Breakdown of the dielectric



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# AllClear (n+) vs Source (p+)



Test of all p-regions vs n-regions => Test of the Diode Integrity  
Criteria: breakdown starts around  $V_{Clear} \approx 15$  V

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	ok	bad	ok	bad	ok							
OF1	ok	bad	ok	ok	ok							
OF2	ok	ok	ok	ok	ok	bad	ok	ok	ok	ok	ok	bad
OB1	ok	bad										
OB2	bad	ok	bad	ok	bad	bad						
IB	bad	ok										

Ok marked in yellow have higher currents (~ 1-3  $\mu$ A, not nA).  
If needed, the modules should be tested further.



# PXD9 – Clear vs Source

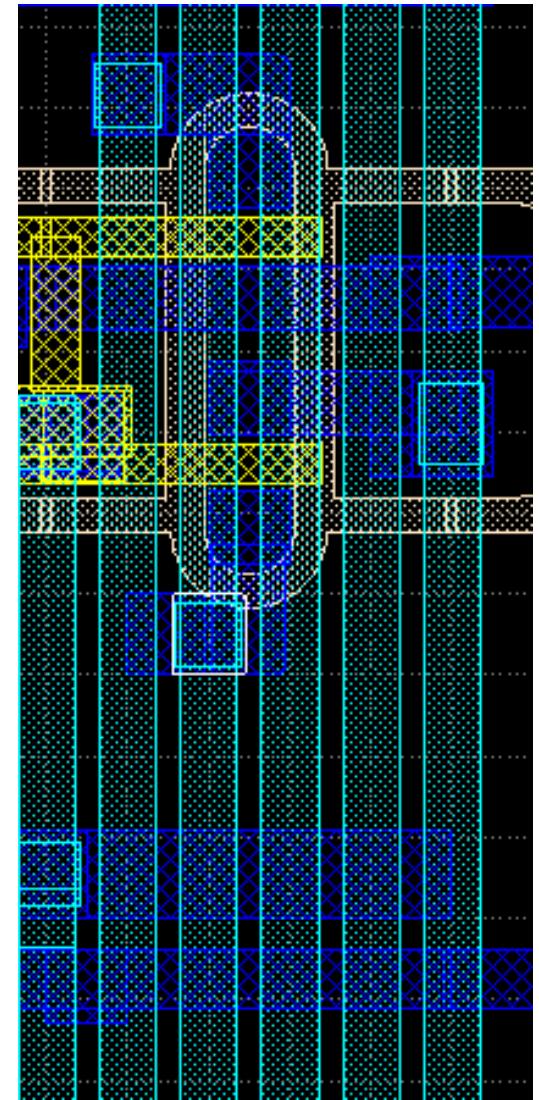
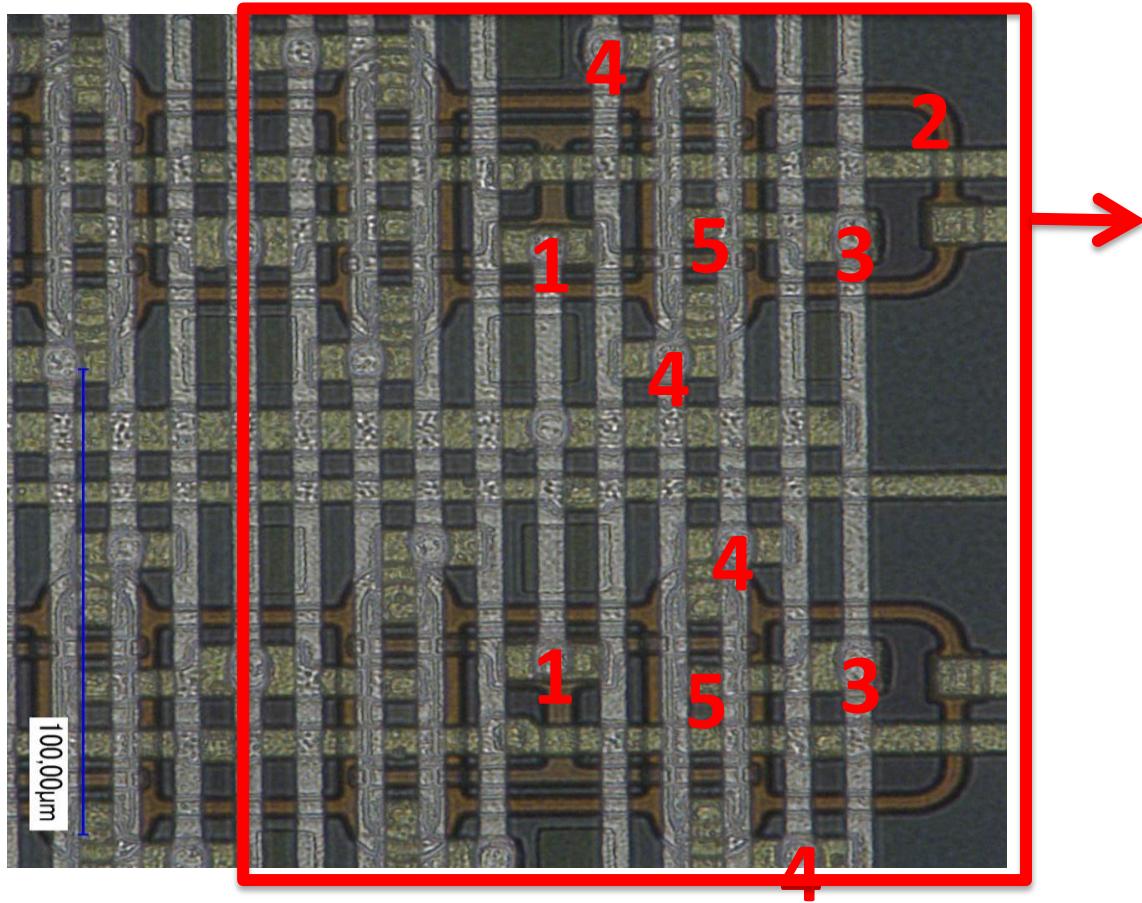
	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	bad	ok	ok	ok	ok	ok	dead	ok	ok	ok	ok	bad	ok	ok	ok
OF1	ok	ok	bad	ok	ok	ok	dead	bad	ok						
OF2	bad	bad	ok	bad	ok	ok	dead	ok	ok	ok	ok	med	bad	ok	ok
OB1	ok	bad	ok	med	ok	ok	dead	ok	ok	ok	bad	ok	bad	ok	ok
OB2	bad	bad	bad	bad	bad	bad	dead	ok	med	bad	bad	ok	ok	ok	ok
IB	ok	med	ok	med	ok	med	dead	bad	ok	bad	med	bad	ok	ok	ok

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	ok	bad	ok	ok	ok	bad	ok	ok	ok	ok	ok	med	ok	ok
OF1	ok	ok	ok	ok	ok	bad	ok	ok	bad	ok	ok	ok	ok	ok
OF2	ok	ok	med	ok	bad	bad	med	bad	med	bad	ok	ok	ok	bad
OB1	bad	ok	ok	bad	ok	ok	med	bad	ok	bad	ok	bad	ok	bad
OB2	ok	bad	bad	ok	ok	bad	ok	bad	ok	med	ok	ok	ok	bad
IB	ok	bad	med	ok										

- Test of all p-regions vs n-regions => Test of the Diode Integrity
- In case of just one short => module is considered bad
- Shorts are not specified => further tests would be required

IF	23	1	5
OF1	24	0	5
OF2	15	4	10
OB1	17	2	10
OB2	13	2	14
IB	19	5	5

# Pixelstructure

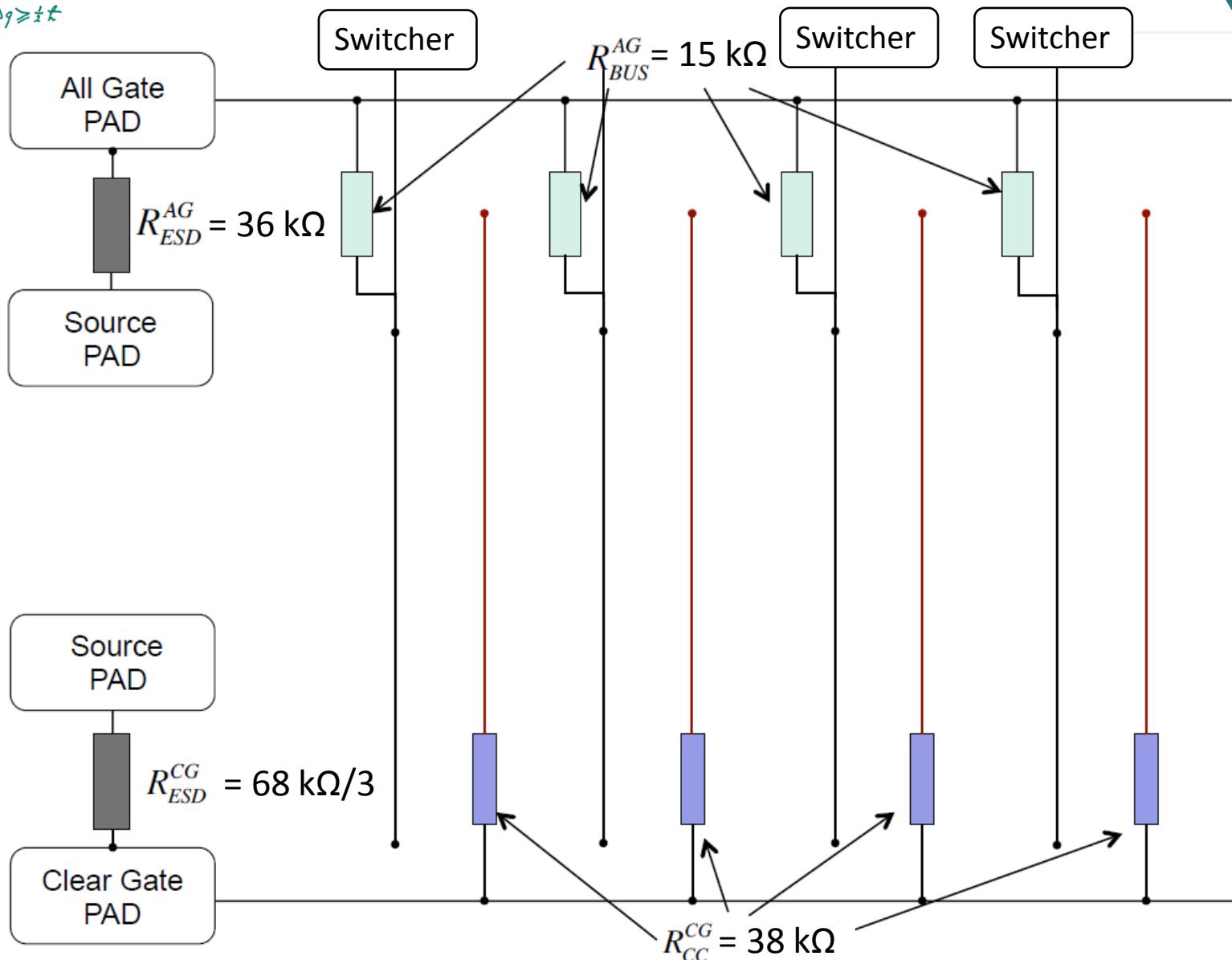


Top view of **12** DEPFET pixels.

1: external gate (poly-Si2), 2: clear gate (poly-Si1),  
3: clear (n+), 4: drain (p+), 5: source (p+).

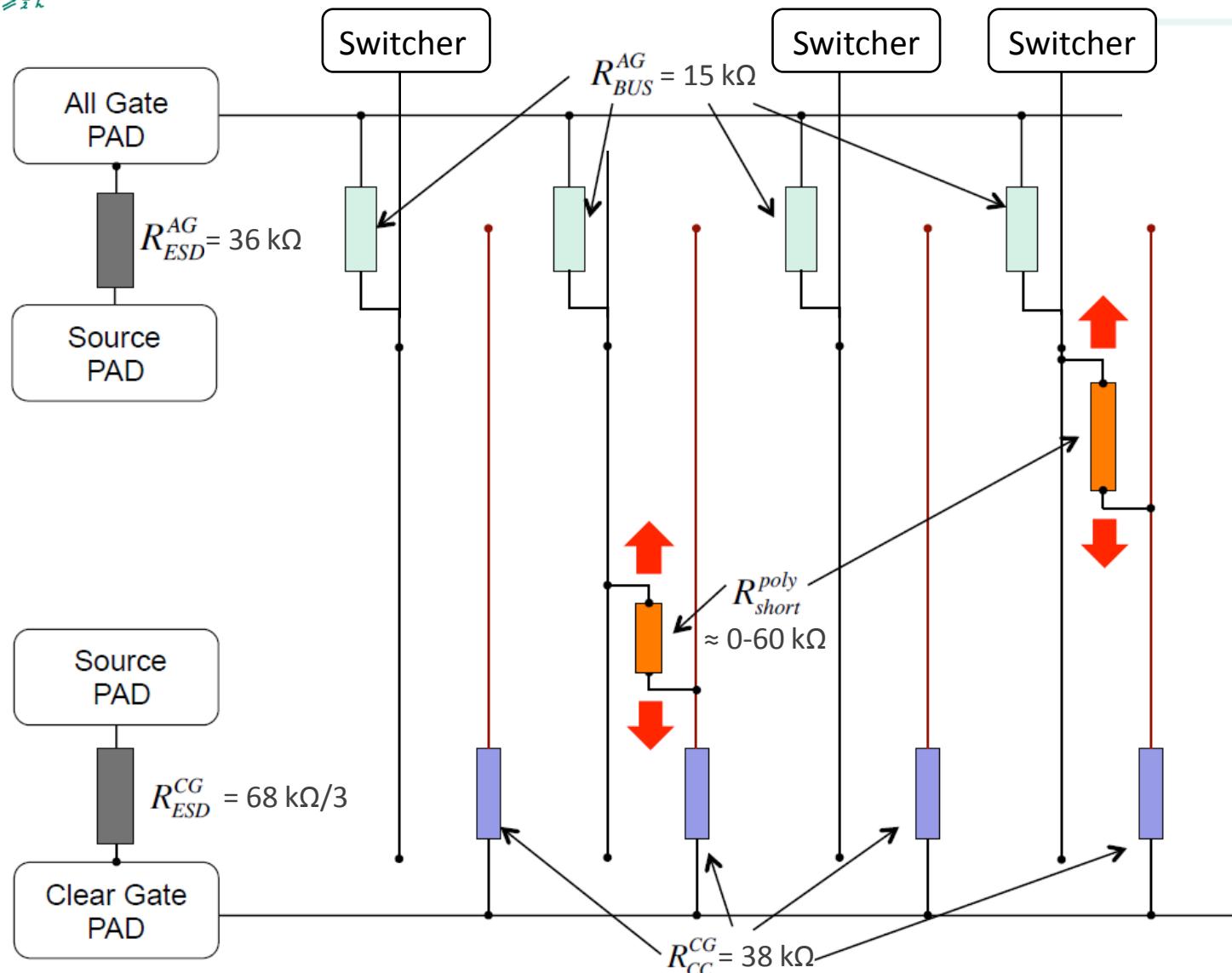


# The poly1/poly2 electrical net





# The poly1/poly2 electrical net

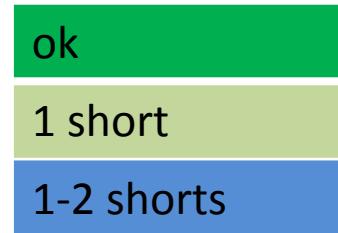




# AllClearGate vs All Gate

But Clear vs Source  
short anyway

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	61,9	67,8	60,3	58,5	58,6	59,3	59	59,8	58,6	58,5	bad	59,4
OF1	49,6	70,4	62,1	59,7	59,6	60,9	60,3	60,8	58	59,8	60,3	52,2
OF2	64,6	72,5	63,7	61,1	44,4	62	61,7	62,5	61,6	61,4	61,8	29
OB1	61,2	68,7	45,2	58,4	58,8	59,4	59,1	59,9	39,9	58,8	59,3	36
OB2	31	68,5	61,2	59	38,6	59,9	41,6	43,4	59,8	59,3	59,6	47
IB	35	67,1	60,7	44,3	58,3	59,5	58,5	59,5	48,6	58,5	59	40,4





# PXD9 – Shorts between Poly1 and Poly2



	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	3+	1-2	2	2	1	1	bad	1	1	1-2	1	0	1	2-3	1-2
OF1	0	1-2	1	1	1	2	bad	1-2	2	2+	2	2	3	0-1	1-3
OF2	2+	2	0	2+	1	3+	bad	1	1	2+	2	2	2+	1	1-2
OB1	0	2	1	1-2	2	2	0*	2	1-2	2+	3+**	1	2+	2+	1
OB2	1	2	1	1	2	2	bad	1-2	1	2+	2	2	2+	1	1
IB	0	2	0	1	2+	1	bad	1	0	1-2	2	1	1-2	2+	0

\*Increased resistance in the AllClearGate\_vs\_Source and AllGate\_vs\_AllClearGate tests

\*\*very low resistance in AllGate vs Source test

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	0	2+	2-3	1-2	2+	1-2	0	1	1	0	1-2	1	1	1
OF1	1	0	2-3	1-2	2+	2+	1	1	0	0	0	1	0	2-3
OF2	0	0	1-2	1	2+	2+	1	1	0	1	0	0	0	2+
OB1	1-2	1	0	1-2	2+	2+	0	2+	1	2+	1-2	1	1	2+
OB2	0	1-2	2+	1-2	1	2+	0	2+	0	0	0	0	0	2+
IB	0	2-3	0	1	1-3	1-3	0	0	0	0	0	0	1	1



# Summary global tests

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	0 shorts	bad	0 shorts									
OF1	0 shorts	1 short	0 shorts	0 shorts	0 shorts							
OF2	0 shorts	0 shorts	0 shorts	0 shorts	1 short	0 shorts	1-2 short					
OB1	0 shorts	0 shorts	1 short	0 shorts	1 short	0 shorts	0 shorts	1 short				
OB2	1 short	0 shorts	0 shorts	0 shorts	1 short	0 shorts	1 short	1 short	0 shorts	0 shorts	0 shorts	1 short
IB	1 short	0 shorts	0 shorts	1 short	0 shorts	0 shorts	0 shorts	0 shorts	1 short	0 shorts	0 shorts	1 short



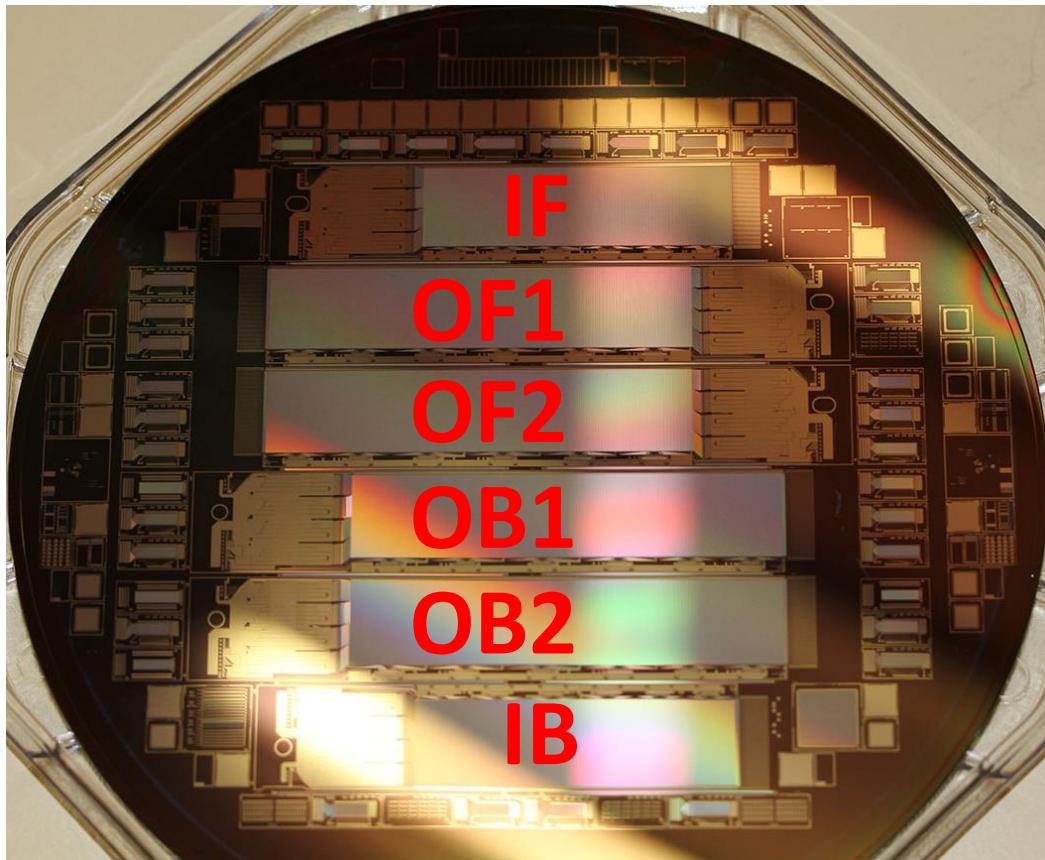


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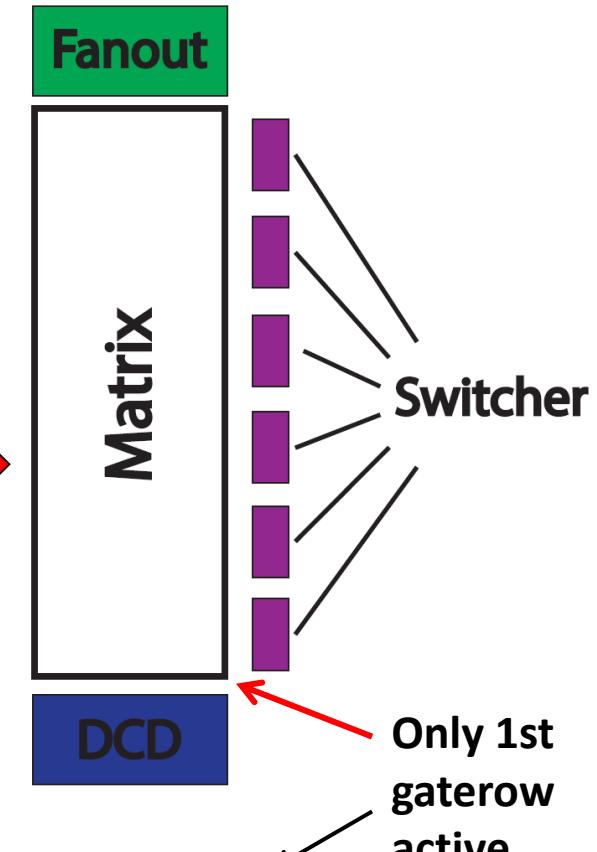
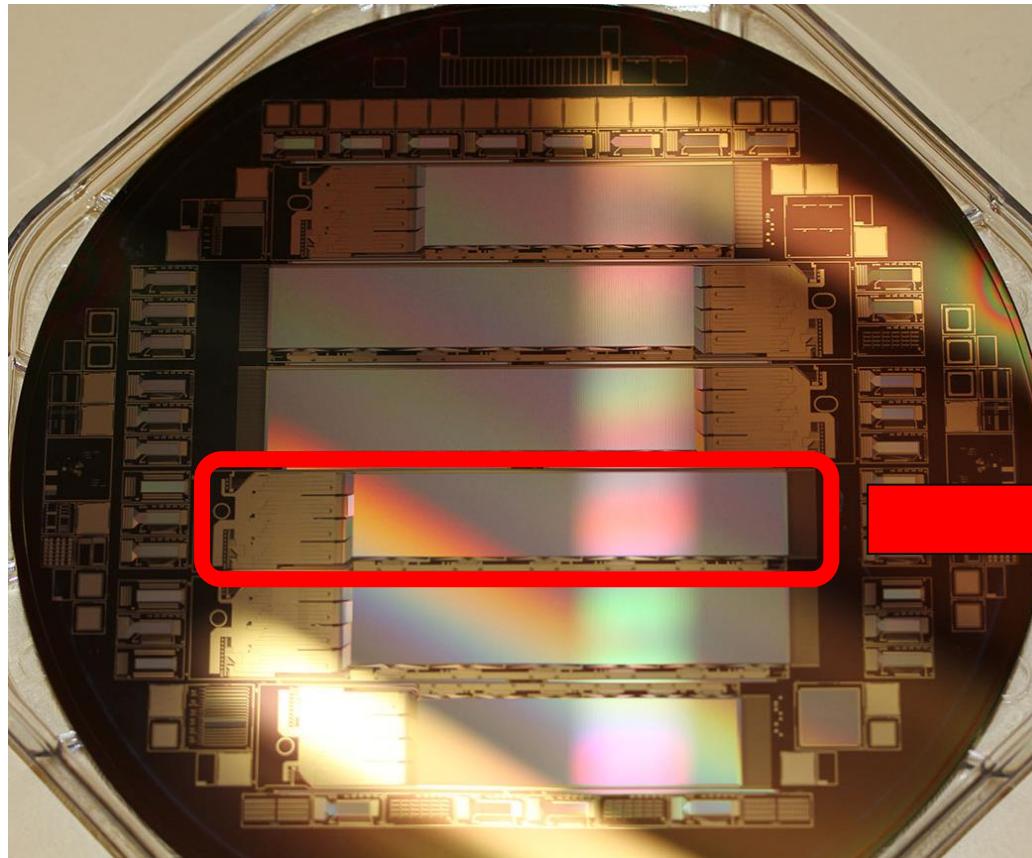
# Wafer and chip layout



Each wafer has 6 modules/chips:

- Inner forward (IF)
- Outer forward (OF1)
- Outer forward (OF2)
- Outer backward (OB1)
- Outer backward (OB2)
- Inner backward (IB)

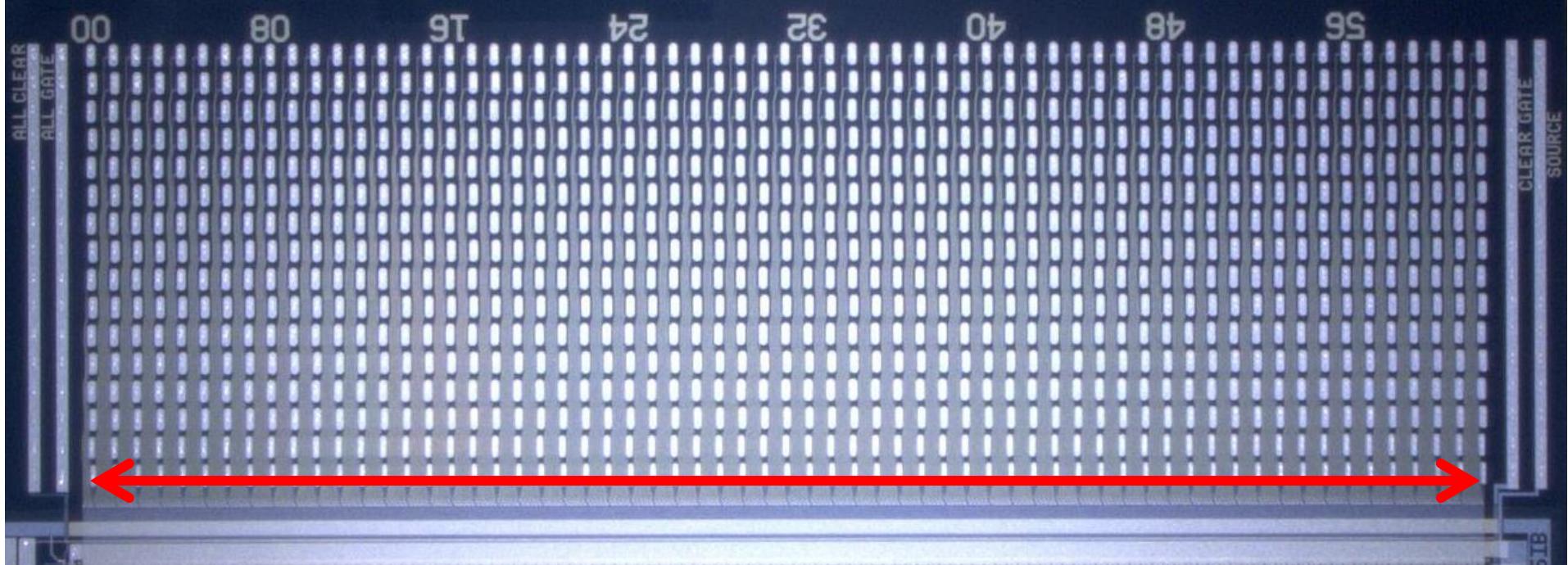
# Wafer and chip layout



Test of the full drainlines



# Probecardtest



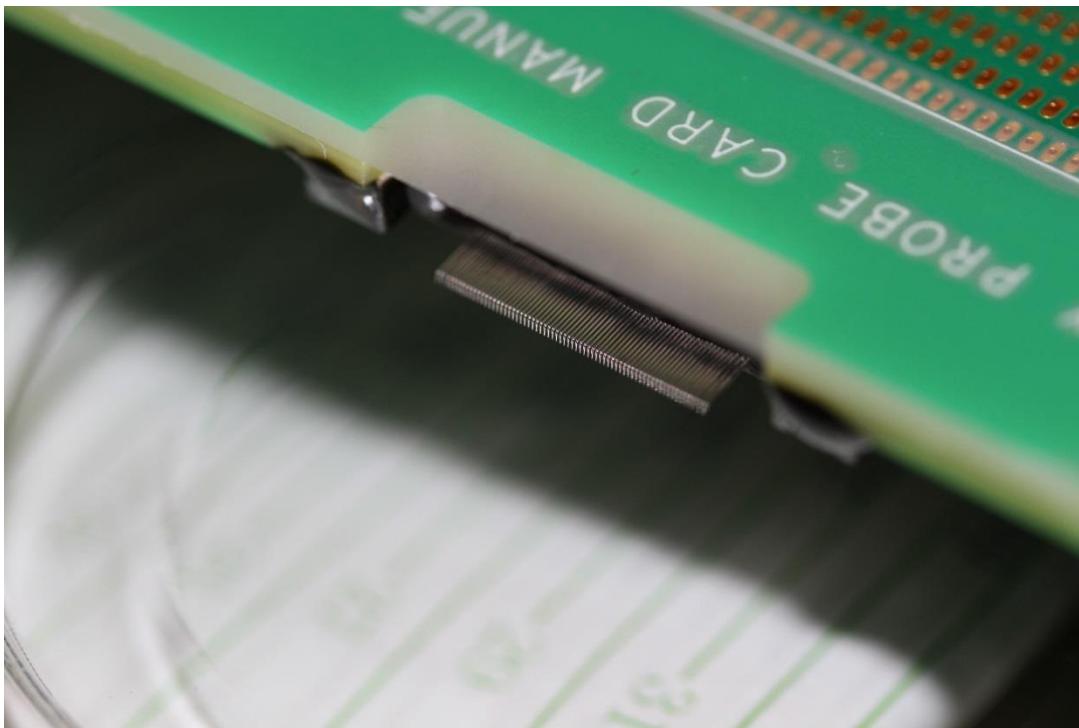
1000 Drain Pads

All Clear  
All Gate

Clear Gate  
Source



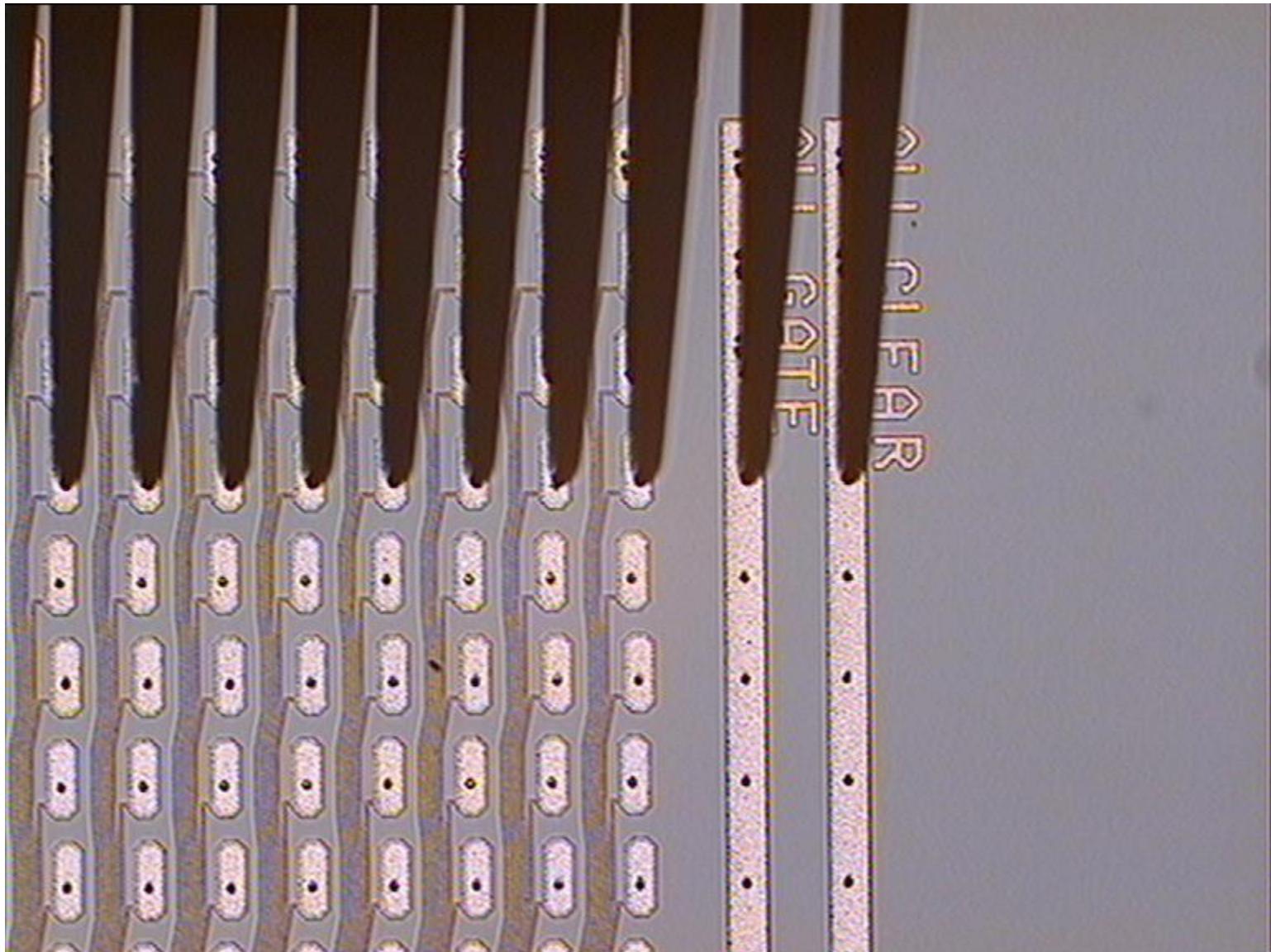
# System description



- Probecard with 134 needles in total, arranged in two rows. 126 needles for the drain lines and 4 needles per row for the static voltages.
- Probecard is connected via two ribbon cables to a conversion board
- Conversion board distributes the currents to the SMUs and the voltages to the probecard
- The 126 drain lines are connected to 7 SMUs → 18 drain lines per SMU
- The 4 static voltages are connected to 1 SMU each
- 1 SMU is used for the single needle for the gate rows.
- → 12 SMUs in total

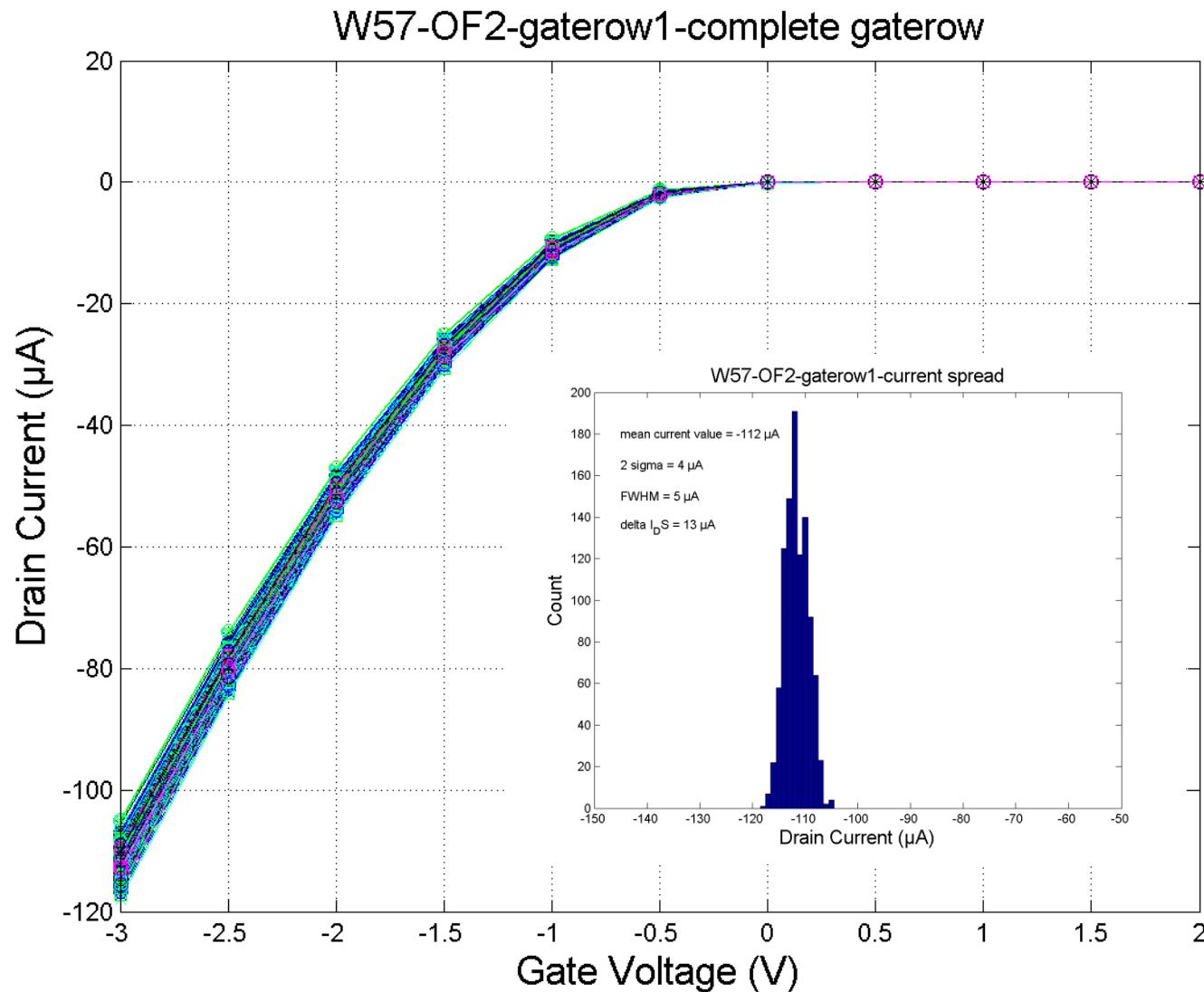


# Probecardtest





# Drain Currents – Transfer characteristics





Please remember:

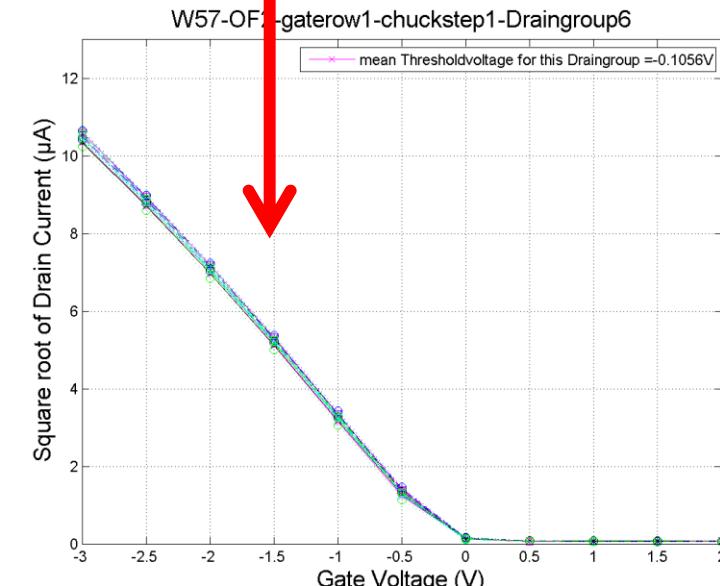
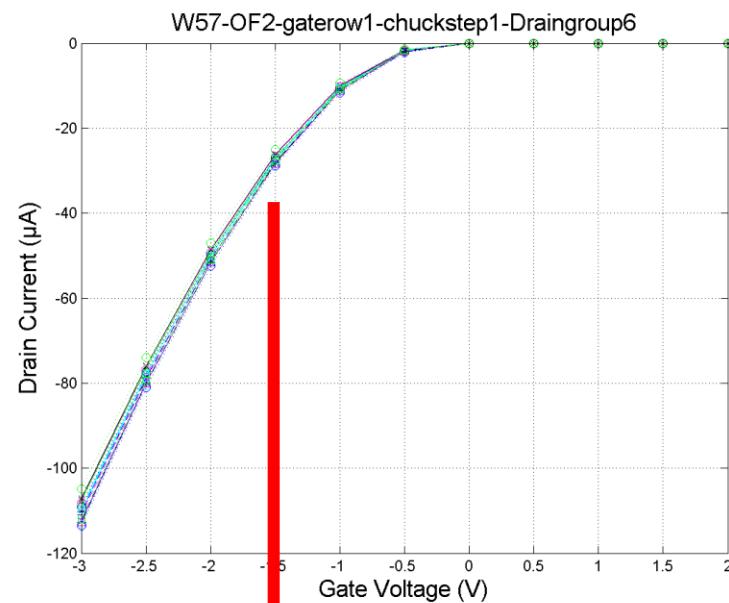
- Main measurement goal: To locate and repair possible faults
- All the values (Threshold, Drain currents and pedestal spread) are just from the first gaterow and from static measurements!



# Threshold voltage – Saturation ( $V_{DS} = -5$ V)

Threshold calculation according to:  
Dieter K. Schroder: Semiconductor  
material and device characterisation.  
Arizona State University (2006),  
p.225.

- Take the square root of the absolute values
- Fit for Gate voltages of -3 V to -1 V
- Get the value of the gate voltage at  $I_{DS} = 0 \mu A$



Threshold voltage mostly around -0.1V



# Mean threshold voltage

All values in V

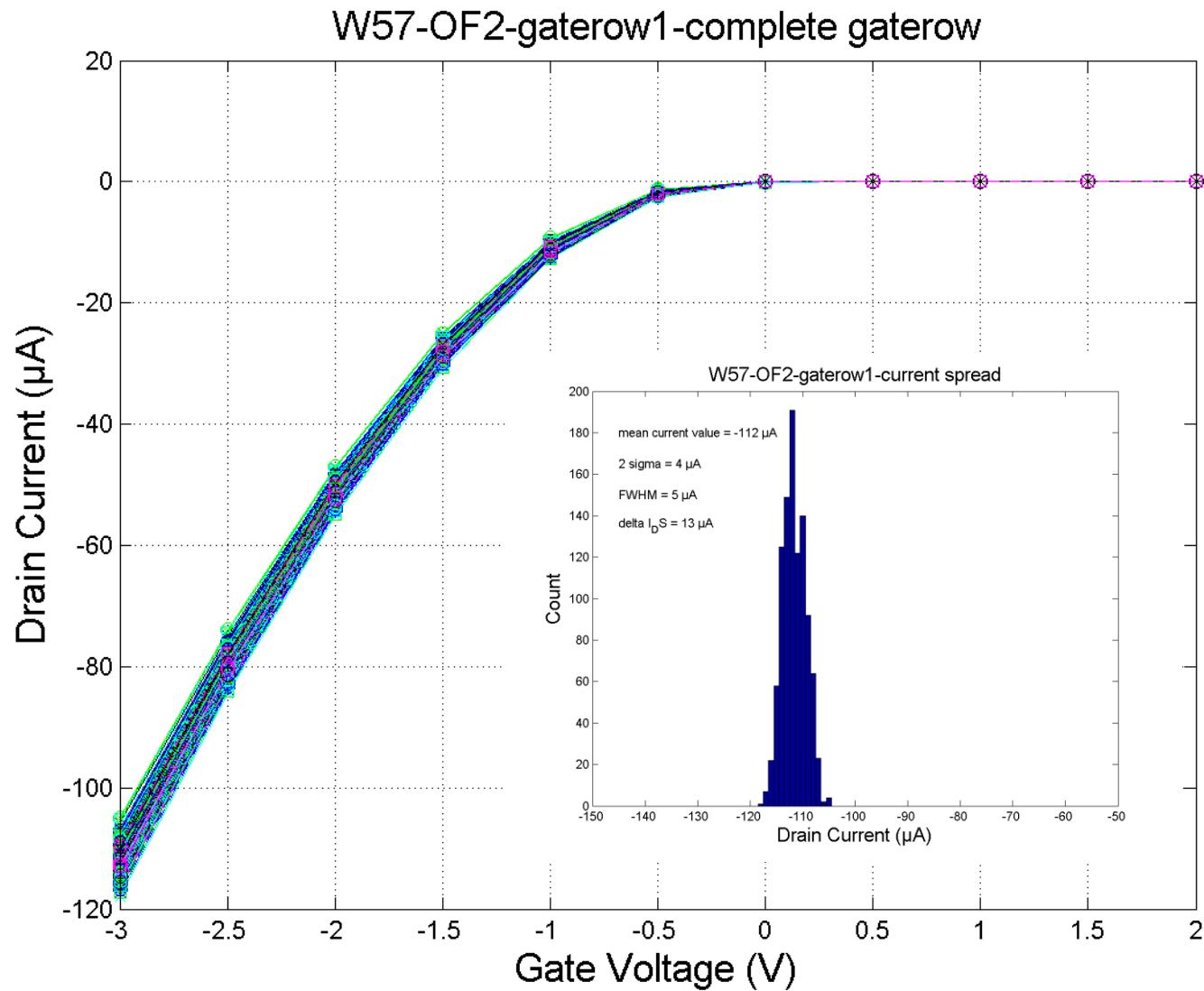
$$V_{DS} = -5 \text{ V}, V_{GS} = -3 \text{ V} \nearrow +2 \text{ V}$$

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	not tested	not tested	-0,06	-0,11	-0,09	-0,1	-0,06	-0,05	-0,13	-0,12	not testable	-0,07
OF1				-0,09		-0,08	-0,1	-0,06	-0,11	-0,08	-0,06	-0,06
OF2						-0,07	-0,06	-0,09	-0,11	-0,1	-0,09	-0,08
OB1	-0,1	0,02	-0,09	-0,14	-0,12	-0,14	-0,15	-0,11	-0,13	-0,13	-0,11	-0,12
OB2	-0,07	0,01	-0,08	-0,14	-0,13	-0,14	-0,12	-0,08	-0,15	-0,13	not testable	-0,12
IB	-0,24	-0,03	-0,23	-0,26	-0,24	-0,26	-0,2	-0,22	-0,26	-0,25	-0,27	-0,21

Mean threshold voltage in previous productions  
was about ~-0,08 V → comparable



# Drain Currents – Transfer characteristics



All values in  $\mu\text{A}$

$V_{DS} = -5 \text{ V}$ ,  $V_{GS} = -3 \text{ V}$

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	not tested	not tested	-117	-110	-111	-110	-117	-119	-109	-109	not testable	-114
OF1				-110		-109	-110	-114	-109	-111	-113	-112
OF2						-106	-112	-112	-108	-110	-111	-112
OB1	-112	-136	-112	-105	-108	-105	-106	-111	-107	-108	-109	-106
OB2	-117	-141	-115	-108	-108	-106	-110	-116	-107	-109	not testable	-109
IB	-99	-129	-100	-95	-96	-94	-103	-101	-95	-94	-94	-102

Mean Drain currents in previous productions was  
about  $\sim 108 \mu\text{A} \rightarrow$  comparable



# Pedestal spread

All values in  $\mu\text{A}$

$V_{DS} = -5 \text{ V}$ ,  $V_{GS} = -3 \text{ V}$

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	not tested	not tested	24	25	25	24	24	25	25	24	not testable	32
OF1				22		19	14	13	12	20	15	20
OF2						19	20	13	16	12	14	18
OB1	26	32	23	25	25	21	21	19	18	21	20	16
OB2	22	28	23	20	22	27	26	23	17	20	not testable	20
IB	31	33	33	31	30	27	31	28	27	30	31	36

The pedestal spreads here are the upper limit(!!), since a less good contact with a needle leads to lower currents => bigger spreads

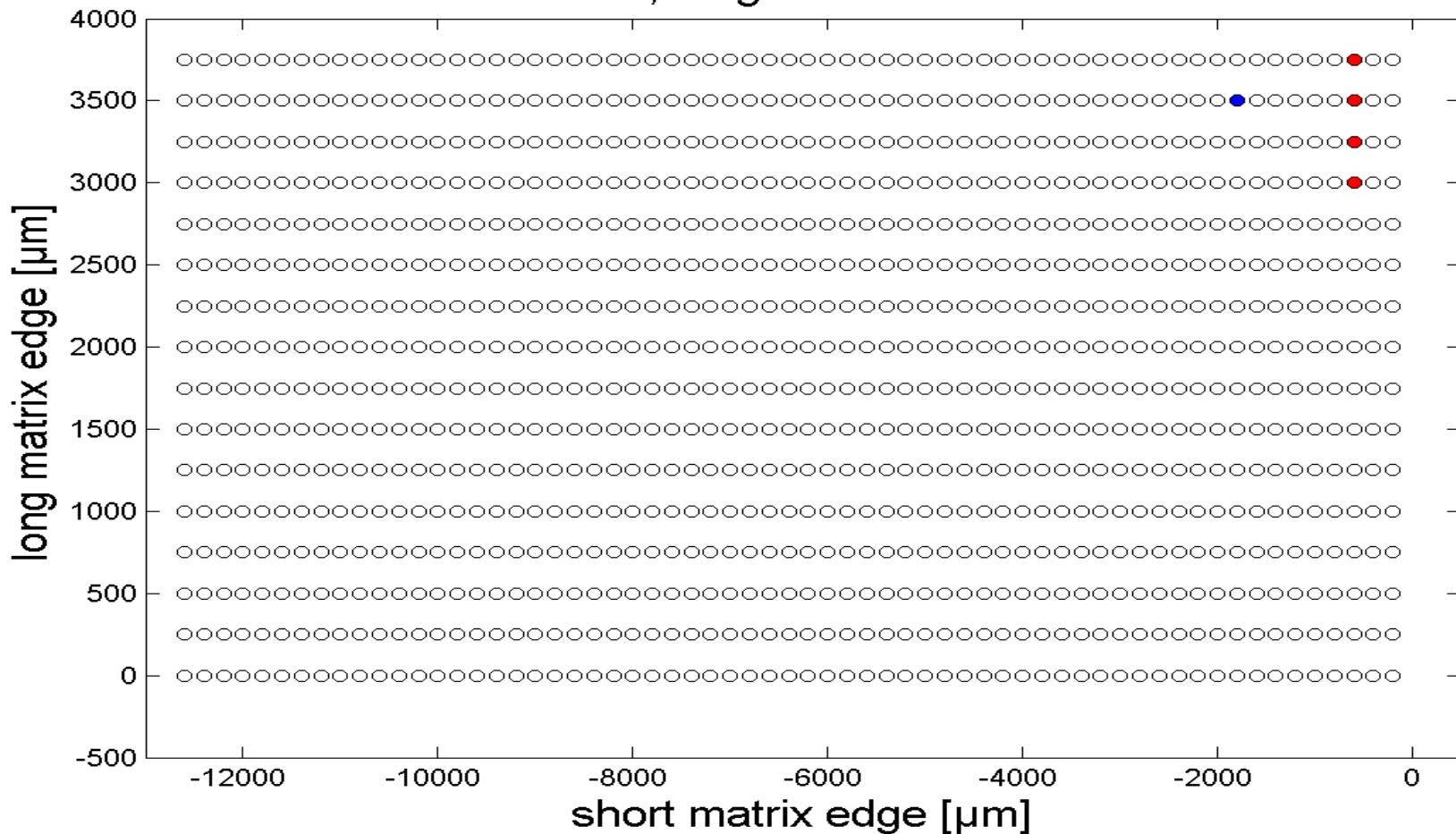
Mean pedestal spreads in previous productions was about  $\sim 18 \mu\text{A} \rightarrow$  comparable



# Example of the mapping from PXD9-6

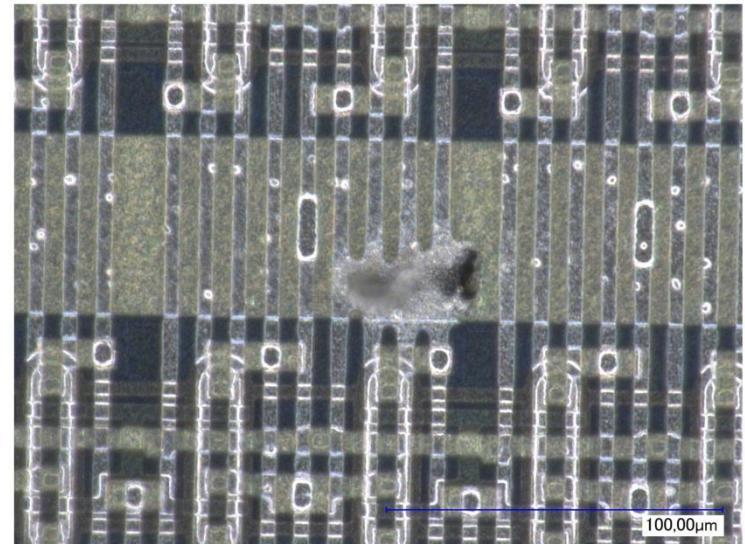
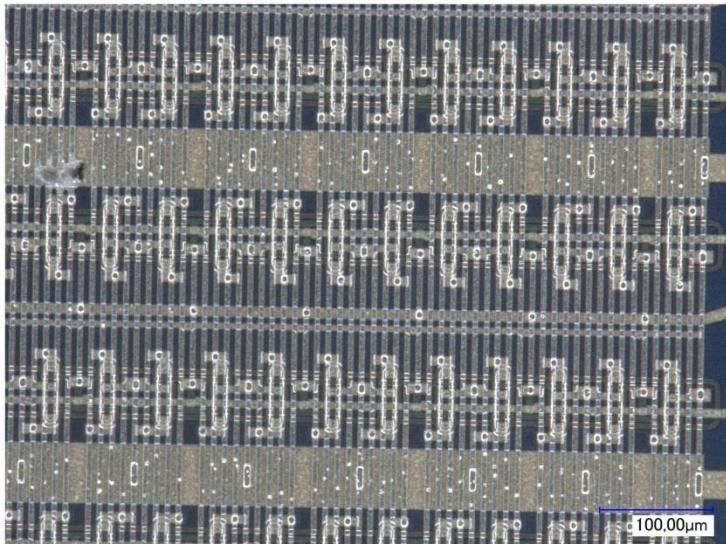
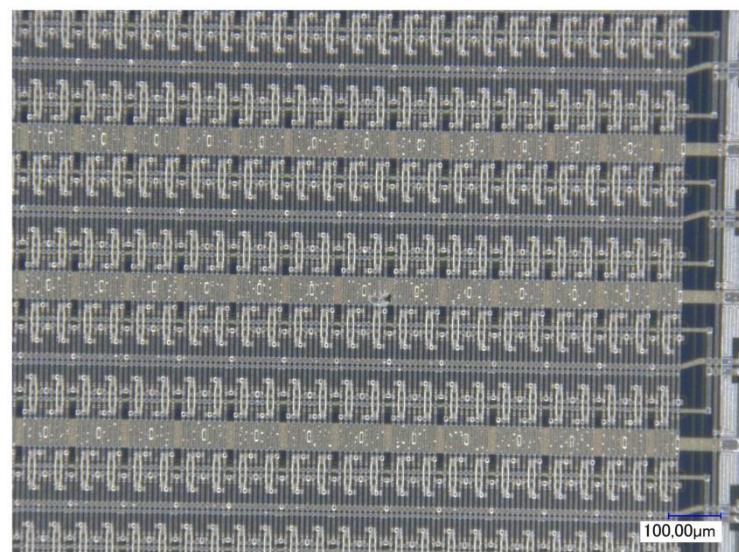
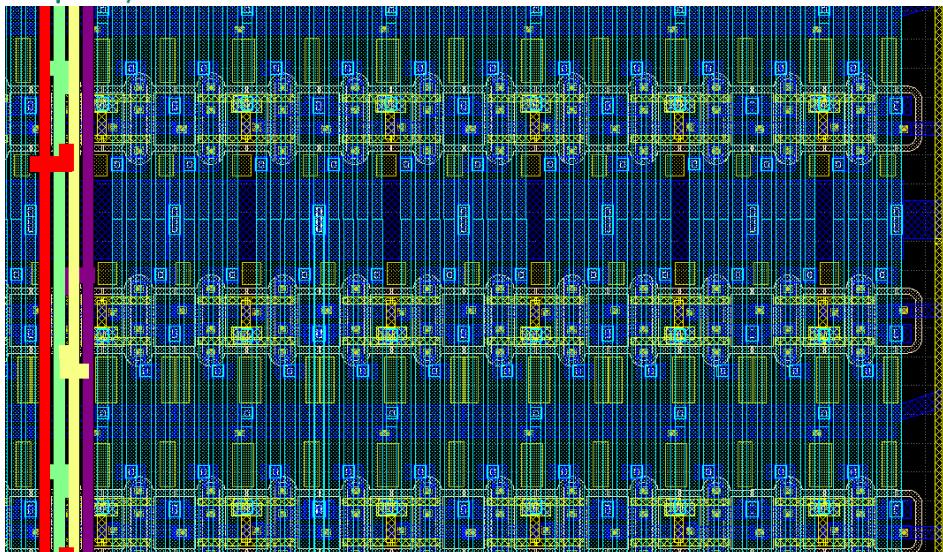
W30-OB2-faulty pads

blue = opens, white = ok, black = 2 drains, cyan = 3 drains  
red = 4 drains, magenta = 5 or more drains





# W30 (PXD9-6)– short in OB2





# Opens

Scrapped in the test fan-out  
by me. No damage to the  
module! But untestable?

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	not tested	not tested	0	0	0	0	0	0	0	0	not testable	0
OF1				1		0	0	0	0	0	0	0
OF2	0	0	0	0	0	0	0	0	0	0	0	0
OB1	0	0	0	0	0	0	0	0	0	0	0	0
OB2	0	0	0	0	0	0	0	0	0	0	not testable	0
IB	1	0	0	0	0	0	0	0	0	0	0	0

Not tested in order to not delay  
processing & enough OF  
modules already



# Shorts

	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	not tested	not tested	0	0	0	2 Drains	2 Drains	0	0	0	not testable	0
OF1				0		0	0	0	1 D-S 4 Drains	0	0	0
OF2					4 weak D-G?	0	0	0	0	2 D-S	0	0
OB1	0	0	0	0	2 Drains	0	0	0	0	6 Drains	0	
OB2	0	0	0	0	0	0	0	3 G-D	1 D-G?	0	not testable	0
IB	0	0	2 Drains	0	0	0	0	0	1 weak D-G	0	0	0

G-D = Gate-Drain short = inverts Drain & Source

D-S = Drain-Source short = too much current to the DCD

=> Repaired by removing the drain lines



# Final yield PXD9-20: prober measurements



	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
IF	NA	0	100	100	100	98.8	99.8	100	100	100	0	100
OF1	NA	NA	NA	99.9	NA	100	100	100	0	100	100	100
OF2	NA	NA	NA	NA	NA	0	100	100	100	99.8	100	0
OB1	100	100	99.5	100	99.8	100	100	100	99.5	100	99.4	0
OB2	0	100	100	100	99.5	100	99.5	99.2	0	100	0	0
IB	0	100	99.8	99.5	100	100	100	100	99.3	100	100	99.5

Only the results of the global tests. No tests  
on the opens, shorts or critical shorts!



# Final results PXD9-20: prober measurements



	Total	defect	Not tested	<95%	95%	98%	$\geq 99\%$	PXD complete
Inner Forward	12	2	1	0	0	0	9-10	8
Outer Forward	24	3	9	0	0	0	12+	12
Outer Backward	24	5	0	0	0	0	19	12
Inner Backward	12	1	0	0	0	0	11	8

Enough good modules to form one complete PXD detector. And there is an additional backup production coming!



Thanks for your attention!

Question?



# PXD9 – Clear vs Source

	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	bad	ok	ok	ok	ok	ok	dead	ok	ok	ok	ok	bad	ok	ok	ok
OF1	ok	ok	bad	ok	ok	ok	dead	bad	ok						
OF2	bad	bad	ok	bad	ok	ok	dead	ok	ok	ok	ok	med	bad	ok	ok
OB1	ok	bad	ok	med	ok	ok	dead	ok	ok	ok	bad	ok	bad	ok	ok
OB2	bad	bad	bad	bad	bad	bad	dead	ok	med	bad	bad	ok	ok	ok	ok
IB	ok	med	ok	med	ok	med	dead	bad	ok	bad	med	bad	ok	ok	ok

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	ok	bad	ok	ok	ok	bad	ok	ok	ok	ok	ok	med	ok	ok
OF1	ok	ok	ok	ok	ok	bad	ok	ok	bad	ok	ok	ok	ok	ok
OF2	ok	ok	med	ok	bad	bad	med	bad	med	bad	ok	ok	ok	bad
OB1	bad	ok	ok	bad	ok	ok	med	bad	ok	bad	ok	bad	ok	bad
OB2	ok	bad	bad	ok	ok	bad	ok	bad	ok	med	ok	ok	ok	bad
IB	ok	bad	med	ok										

- Test of all p-regions vs n-regions => Test of the Diode Integrity
- In case of just one short => module is considered bad
- Shorts are not specified => further tests would be required

IF	23	1	5
OF1	24	0	5
OF2	15	4	10
OB1	17	2	10
OB2	13	2	14
IB	19	5	5



# PXD9 – Clear vs Source

	PXD9-6				PXD9-7				PXD9-8				PXD9-9				PXD9-10		
	IF	OF1	OF2	OB1	OB2	IB		IF	OF1	OF2	OB1	OB2	IB		IF	OF1	OB1	OB2	IB
IF	3	0	0	3	0	1	7	1	1	5	0	1	5	0	0	1	5	0	2
OF1	3	0	0	3	0	1	8	0	1	5	0	1	5	0	0	1	5	0	2
OF2	2	1	0	1	1	2	5	1	3	3	0	3	4	0	1	3	4	1	2
OB1	2	0	1	3	1	0	4	0	5	4	1	1	4	0	0	1	4	0	3
OB2	2	0	1	3	0	1	5	1	3	0	0	6	3	1	1	3	1	3	1
IB	2	1	0	4	0	0	8	0	1	3	3	0	2	1	1	3	1	4	1

With  
PXD9-6

IF	23	1	5
OF1	24	0	5
OF2	15	4	10
OB1	17	2	10
OB2	13	2	14
IB	19	5	5

Without  
PXD9-6

IF	20	1	5
OF1	21	0	5
OF2	13	3	10
OB1	15	2	9
OB2	11	2	13
IB	17	4	5

- Test of all p-regions vs n-regions => Test of the Diode Integrity
- In case of just one short => module is considered bad
- Shorts are not specified => further tests would be required

IF	20	1	5
OF	34	3	15
OB	26	4	22
IB	17	4	4



# PXD9 – Shorts between Poly1 and Poly2



	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	3+	1-2	2	2	1	1	bad	1	1	1-2	1	0	1	2-3	1-2
OF1	0	1-2	1	1	1	2	bad	1-2	2	2+	2	2	3	0-1	1-3
OF2	2+	2	0	2+	1	3+	bad	1	1	2+	2	2	2+	1	1-2
OB1	0	2	1	1-2	2	2	0*	2	1-2	2+	3+**	1	2+	2+	1
OB2	1	2	1	1	2	2	bad	1-2	1	2+	2	2	2+	1	1
IB	0	2	0	1	2+	1	bad	1	0	1-2	2	1	1-2	2+	0

\*Increased resistance in the AllClearGate\_vs\_Source and AllGate\_vs\_AllClearGate tests

\*\*very low resistance in AllGate vs Source test

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	0	2+	2-3	1-2	2+	1-2	0	1	1	0	1-2	1	1	1
OF1	1	0	2-3	1-2	2+	2+	1	1	0	0	0	1	0	2-3
OF2	0	0	1-2	1	2+	2+	1	1	0	1	0	0	0	2+
OB1	1-2	1	0	1-2	2+	2+	0	2+	1	2+	1-2	1	1	2+
OB2	0	1-2	2+	1-2	1	2+	0	2+	0	0	0	0	0	2+
IB	0	2-3	0	1	1-3	1-3	0	0	0	0	0	0	1	1



## PXD9 – Opens



	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	29	0	0	0	2	0	bad	0	1	0	0	0	0	0	0
OF1	4	0	3	2	0	1	bad	0	0	0	0	0	0	1	0
OF2	2	0	6	4	2	0	bad	0	0	0	0	1	0	0	0
OB1	0	0	0	0	0	0	bad	0	0	0	0	0	0	0	0
OB2	5	1	0	0	1	0	bad	0	0	8	2	0	0	1	0
IB	56	0	0	0	0	0	bad	0	0	0	3	0	0	---	---

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	0	0	0	0	0	0	0	0	2	0	0	0	0	0
OF1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
OF2	0	0	0	0	0	0	0	0	0	0	0	1	0	0
OB1	0	0	0	0	0	1	0	0	0	bad	0	0	0	0
OB2	0	0	0	0	0	3	1	0	0	1	0	0	0	0
IB	0	0	---	---	---	---	---	0	0	0	0	0	0	0



# PXD9 – Shorts

	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	0	0	0	0	0	7 D-S + 2	bad	0	0	2	2 G-D	0	2	83*	1+1 D-S
OF1	0	0	2	0	0	0	bad	0	0	0	0	0	0	0	0
OF2	0	0	0	2	0	2	bad	0	0	2	2	0	2 D-S	0	0
OB1	0	1 D-S	0	0	0	0	bad	0	0	0	12	2	2 D-S	2	1 G-D
OB2	0	0	1 D-S	0	0	0	bad	0	0	0	2	3	0	4	0
IB	0	0	0	0	0	0	bad	0	0	0	5	0	0	---	---

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	0	0	0	0	0	2	0	0	2	0	0	2	0	0
OF1	0	0	0	0	2	0	0	0	0	0	0	0	0	3 G-D
OF2	0	0	0	0	0	0	2	2	0	0	0	0	0	0
OB1	0	0	6*	0	0	4 D-S	0	0	0	bad	2	0	0	0
OB2	0	0	5	2	0	0	0	0	0	1	0	0	0	0
IB	0	0	---	---	---	---	---	0	0	0	0	0	0	0

\*Scratched during testing, had been 0 before

Normal short: repairable by 2nd etch after Me2

D-S: Drain to Source (Me2-Me2) short, affecting one drain line -> repairable by 2nd etch after Me2

G-D: Gate to Drain (Me1-Me2) short, affecting one drain line -> repaired by removing the drainline



# PXD9 – mean Pedestal currents of one gaterow

	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	-102	-104	-110	-103	-103	-109	bad	-101	-116	-104	-111	-112	-106	-95	-110
OF1	-105	-103	-110	-106	-105	-113	bad	-102	-113	-107	-117	-115	-113	-106	-111
OF2	-94	-100	-99	-96	-103	-102	bad	-97	-108	-95	-107	-110	-99	-102	-106
OB1	-95	-98	-97	-98	-97	-100	bad	-95	-113	-95	-105	-105	-96	-99	-100
OB2	-95	-96	-103	-96	-105	-105	bad	-100	-106	-96	-107	-107	-104	-104	-99
IB	-86	-88	-94	-89	-103	-98	bad	-92	-97	-87	-101	-101	-97	---	---

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	-120	-124	-129	-122	-122	-125	-125	-129	-128	-137	-155	-139	-146	-155
OF1	-119	-121	-122	-123	-126	-118	-125	-125	-137	-137	-136	-139	-135	-148
OF2	-114	-118	-114	-117	-120	-118	-120	-120	-122	-130	-128	-133	-130	-137
OB1	-105	-115	-114	-111	-115	-115	-118	-124	-121	bad	-126	-133	-134	-137
OB2	-106	-115	-114	-110	-117	-125	-118	-123	-124	-131	-131	-130	-132	-136
IB	-101	-107	---	---	---	---	---	-108	-111	-118	-126	-119	-115	-124



# PXD9 – Pedestal spread (upper limit)

	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	27	13	14	12	16	13	bad	10	17	14	17	19	12	41	22
OF1	14	13	15	12	17	16	bad	16	21	17	21	25	17	30	22
OF2	16	13	15	15	16	17	bad	16	11	23	16	18	12	24	21
OB1	15	12	15	14	16	19	bad	17	22	14	21	13	23	21	17
OB2	18	14	12	15	17	14	bad	13	15	22	18	13	14	24	18
IB	18	20	17	14	16	15	bad	16	13	13	17	18	14	---	---

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	20	16	30	27	27	26	29	16	25	26	25	20	16	22
OF1	17	26	24	31	24	23	21	23	24	23	21	18	26	20
OF2	18	20	27	31	20	23	18	21	19	25	27	21	18	22
OB1	16	23	20	25	22	19	22	27	18	bad	19	17	15	25
OB2	24	19	22	25	24	22	21	19	17	18	19	18	23	22
IB	15	14	---	---	---	---	---	18	14	16	18	22	21	23



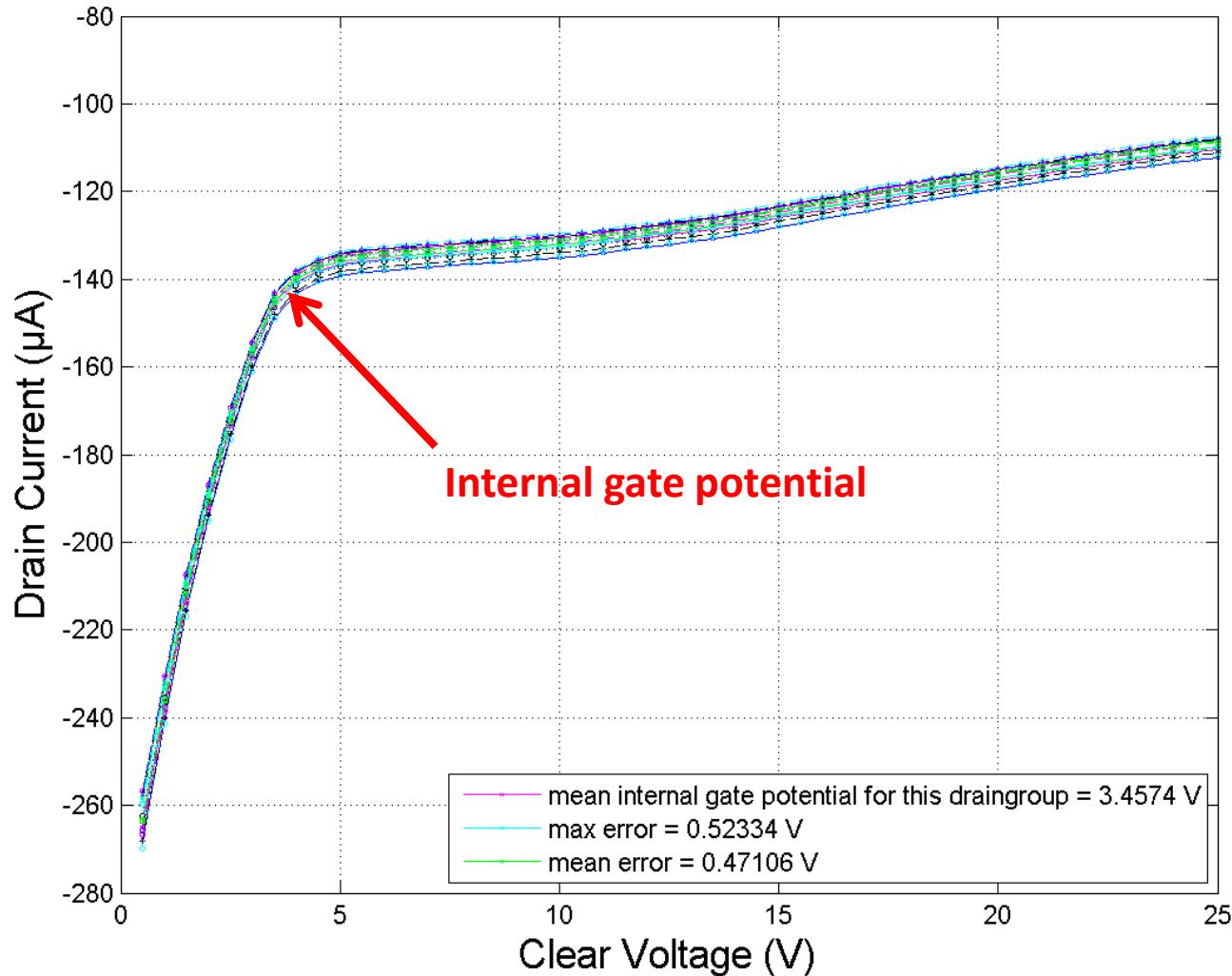
## PXD9 – mean Threshold of one gaterow

	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W30	W31
IF	-0,01	-0,03	0,02	-0,03	-0,07	0,00	bad	-0,07	0,07	-0,03	0,02	0,02	-0,03	-0,14	-0,02
OF1	0,00	-0,04	0,01	0,00	-0,04	0,05	bad	-0,07	0,04	0,03	0,09	0,06	0,02	-0,07	-0,02
OF2	-0,15	-0,06	-0,12	-0,11	-0,05	-0,10	bad	-0,12	0,00	-0,14	-0,02	0,00	-0,11	-0,07	-0,08
OB1	-0,13	-0,09	-0,14	-0,06	-0,12	-0,08	bad	-0,13	-0,02	-0,10	0,08	-0,05	-0,14	-0,15	-0,13
OB2	-0,07	-0,10	-0,03	-0,10	-0,06	0,00	bad	-0,03	-0,00	-0,05	0,02	-0,01	0,00	-0,13	-0,15
IB	-0,21	-0,16	-0,13	-0,18	-0,15	-0,07	bad	-0,13	-0,11	-0,18	-0,13	-0,06	-0,11	---	---

	W32	W33	W35	W36	W37	W38	W40	W41	W42	W43	W44	W45	W46	W47
IF	0,04	0,09	0,10	0,06	0,09	0,10	0,08	0,09	0,12	0,04	0,00	0,02	0,00	0,00
OF1	0,03	0,03	0,09	0,13	0,08	-0,01	0,09	0,08	0,03	0,04	0,05	0,02	0,08	0,00
OF2	-0,02	0,01	0,01	0,10	0,04	0,01	0,05	0,05	0,04	0,12	0,08	0,12	0,12	0,04
OB1	-0,10	0,03	0,00	-0,05	0,01	-0,02	-0,01	0,07	0,02	bad	0,03	0,13	0,10	0,04
OB2	-0,09	0,01	0,00	-0,08	0,02	0,81	0,01	0,08	0,02	0,12	0,09	0,14	0,13	0,04
IB	-0,13	-0,05	---	---	---	---	---	-0,09	-0,12	0,01	0,04	0,04	-0,02	0,02



# Internal Gate Potential PXD9-6

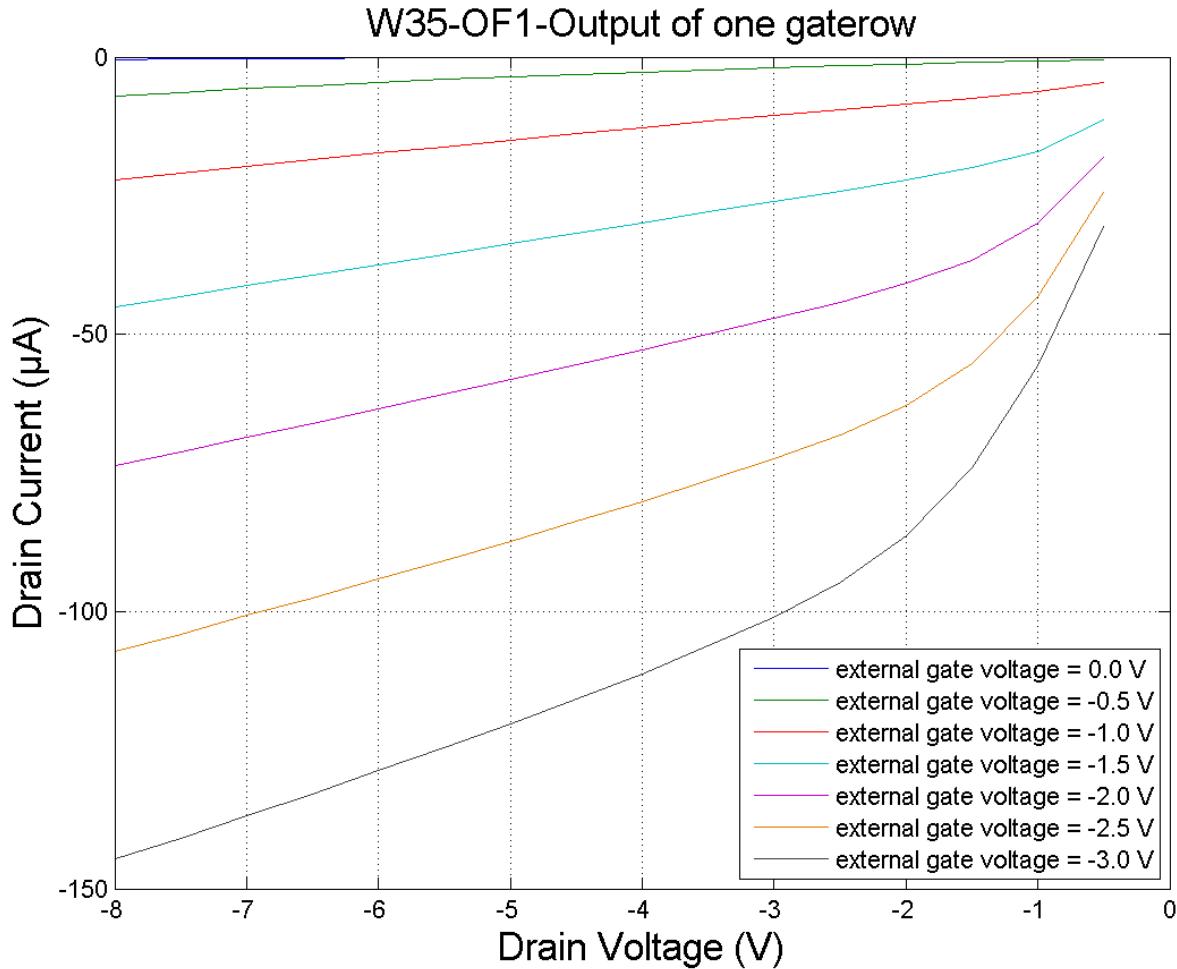


Internal gate potential of one gate row as a function of the clear voltage for 18 drains.

An average over the full gate row (1000 drains) gives:

- Mean internal gate potential:  
 $3.5 \pm 0.5 \text{ V}$

# Output Characteristics PXD9-6



Average output characteristics of one gate row as a function of the drain voltage for different external gate voltages.

- The channel length modulation factor is:  
 $\lambda = 8.8 \pm 0.5 \text{ V}$  at a gate voltage of  
 $V_{GS} = -3 \text{ V}$

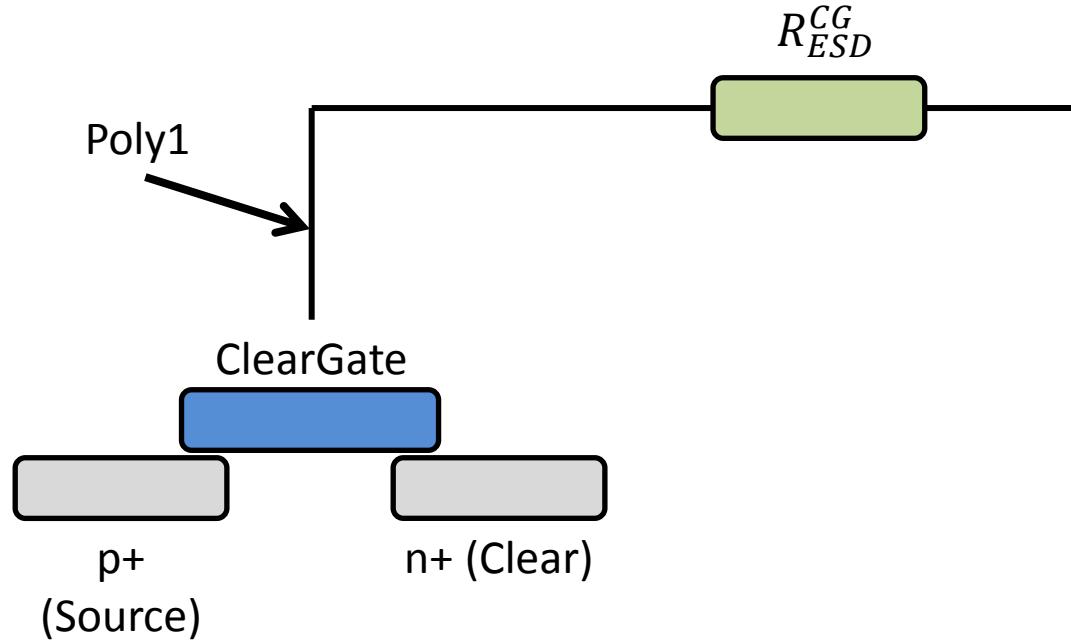
# AllClear (n+) vs Source, Drain and Drift (p+)

ClearGate is coupled with the Clear if:  $RC > t_{Clear}$

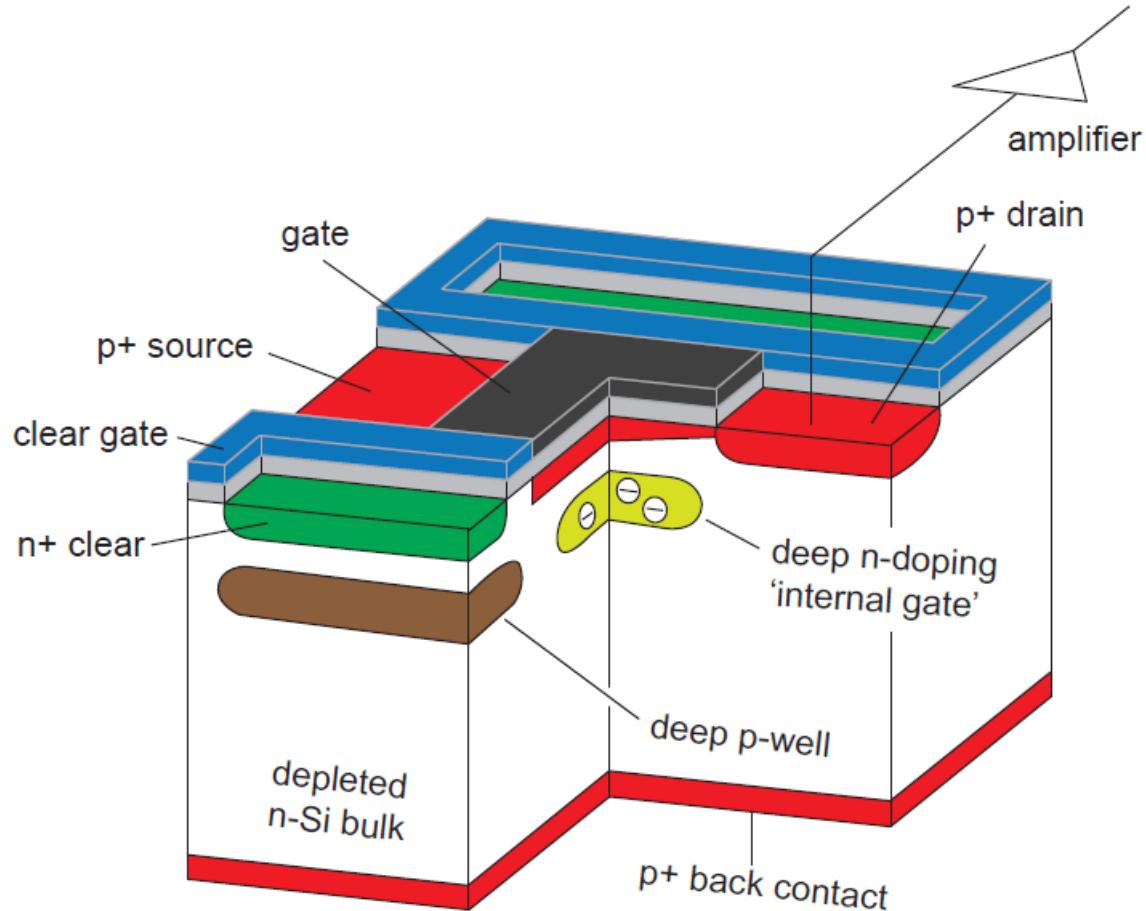
But in static measurements  $t_{Clear} \gg RC$   
 hence  $V_{CG}$  isn't coupled anymore to  $V_{Cl}$  and fixed  
 at 0 V over the  $R_{ESD}^{CG}$

$$\Delta V_{CG} = \Delta V_{CL} * \frac{C_{CG-Cl}}{\sum C_{CG}}$$

↑  
 $\approx 30\%$



# Structure of DEPFET



- Basics of DEPFET
  - e<sup>-</sup> from the e<sup>-</sup>-h pairs move to deep n-doping (internal gate)
  - If enough image charges are collected at the gate due to the collected e<sup>-</sup> charges in the internal gate, a proportional transistor current can be read out
  - n<sup>+</sup> clear removes the e<sup>-</sup> from the internal gate