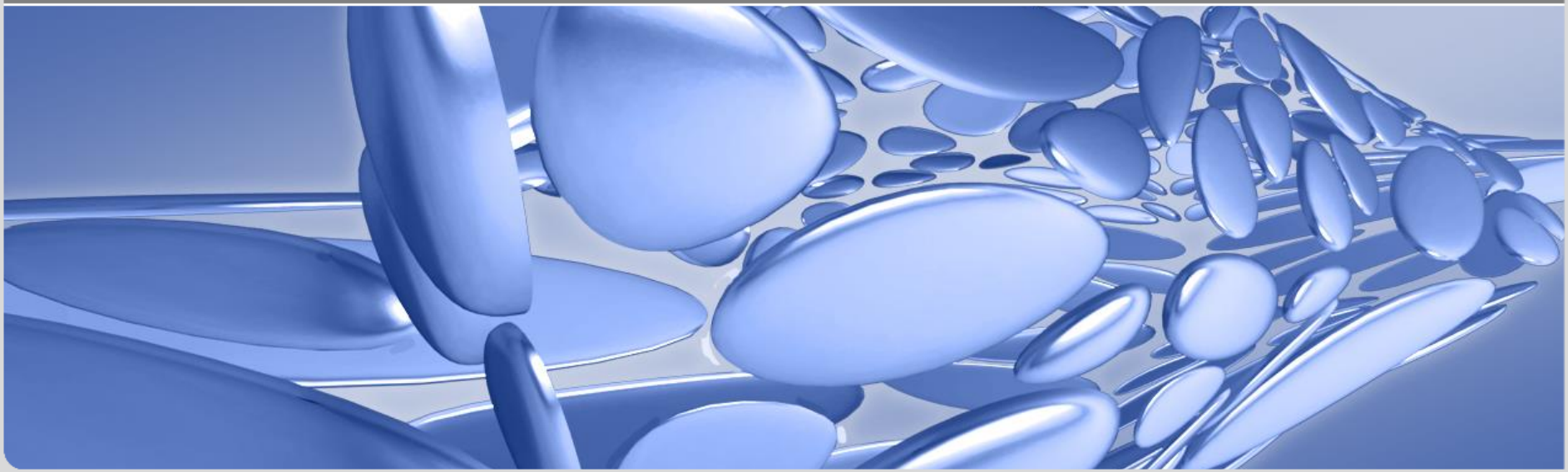
1) DCD/SWB for DEPFET PXD upgrade and 2) HV-CMOS option for VXD upgrade

Ivan Peric, Felix Ehrler, Jan Bader



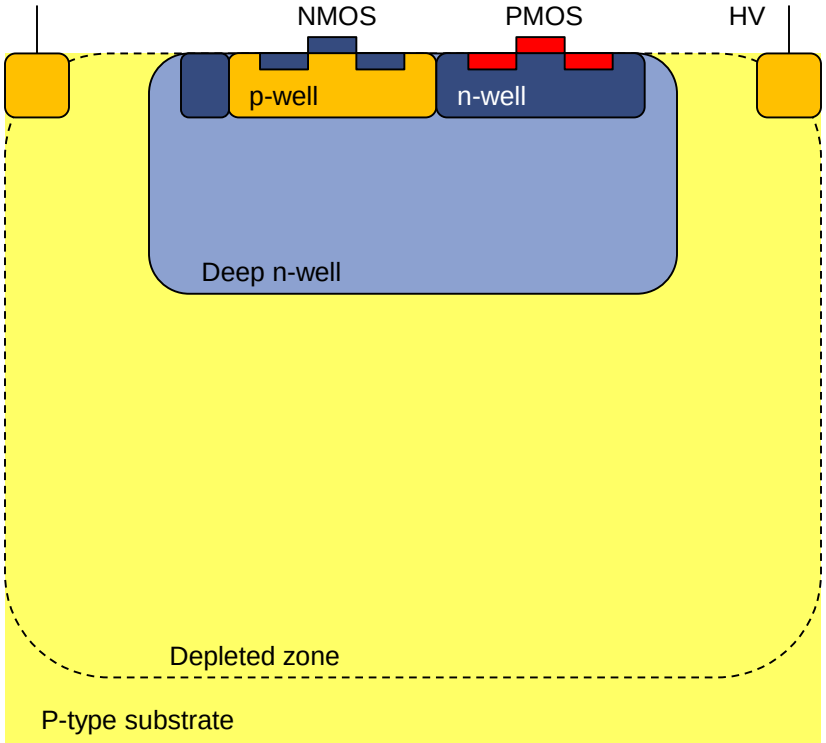
1) DCD/SWB for DEPFET PXD upgrade

- DEPFET readout
- Possible developments (DCD)
- Lower power consumption: DCDC – DCD with SAR ADC
- Faster sampling rate: Motivation Belle upgrades, try to cope with occupancy
  - Example 50ns instead 100ns (256 channels), faster is also possible (time interleaving)
- Implementation of fast LVDS links: motivation DCD to FPGA direct connection
  - Example: 1.6 G bit/s each, 8b10b, 16 such links are equivalent to 64 CMOS links (we have now)
- DCD with extended dynamic range: Motivation diffraction experiments (Electrons, x-rays)
  - Example sampling time 512ns – linear dynamic range ~16 000, generally: dynamic range = $time^2$
- SWITCHER improvements
  - E.g. with more channels

2) HV-CMOS option for VXD upgrade

- The HVCMOS sensors are implemented in standard CMOS technologies

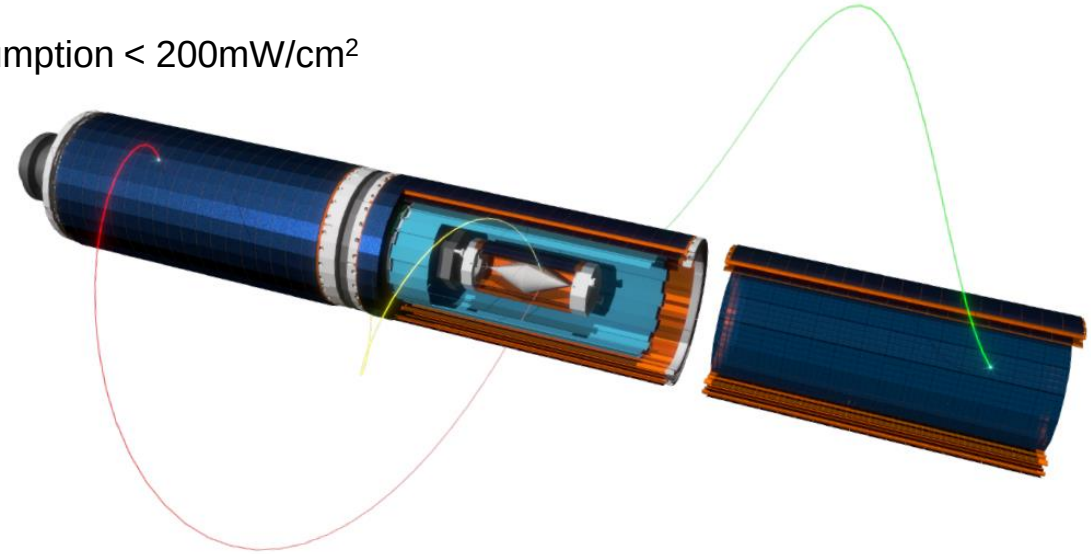
- Pixels are based on floating electronics structure – pixel electronics is placed into a deep n-well.
- Deep-n-well fulfils two tasks:
- 1. Local substrate for electronics (isolated from p-substrate)
- 2. Charge collecting electrode.
- The p-substrate region below the deep n-well is depleted by setting substrate to negative HV. Typical depletion: 30 – 50µm for 80 to 200 Ωcm resistivity. Typical MIP signals are typically >5000e for 200 Ωcm substrate
- The substrate contacts are at the chip surface (undepleted parts of it).



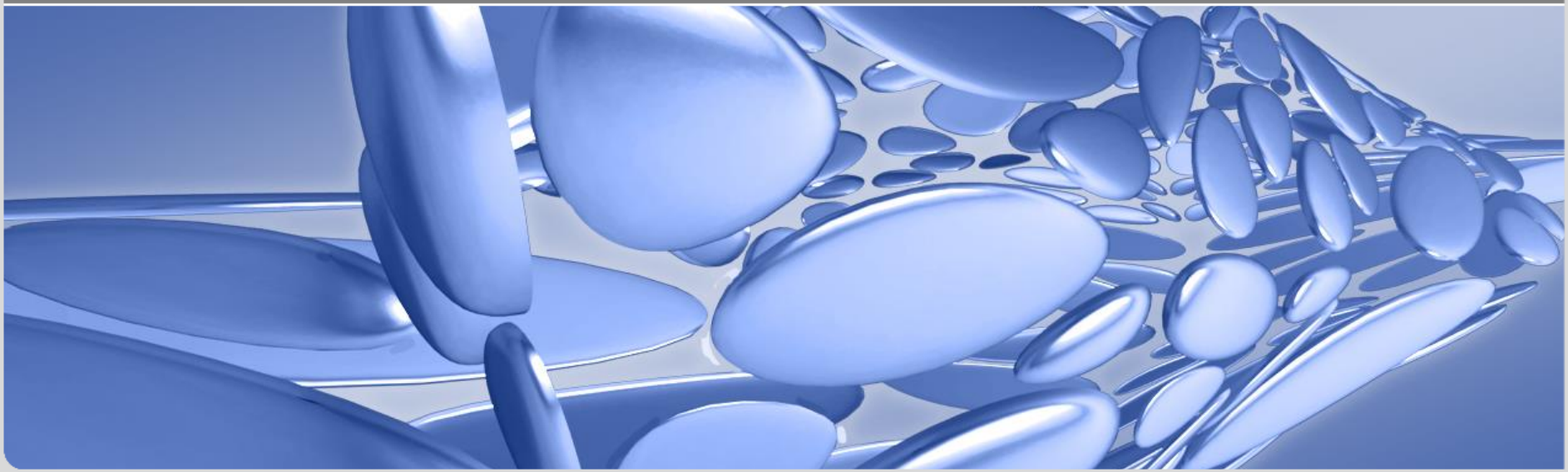
- The advantage of standard process is cost, possibility to have data processing on sensor chip
- Another advantage of HVCMOS is that the sensors can be thinned
- The high voltage is connected from front side
- Radiation tolerance is good
- One limitation:
- CMOS sensors are produced by stepper, this means that the chip size is in principle limited to projection size of 2 x 2cm. Larger chips are possible by reticle stitching, or by post processing
- Some foundries like LFoundry, TSI, XFAB, TJ offer stitching
- Some not: like AMS, IHP

- We develop HVCMOS as R&D, for Mu3e experiment (main option), for CLIC and ATLAS (proposed)
- CMOS sensor for Belle PXD could be based on one oft he existing designs

- Mu3e pixel detector should have extremely little material (0.1% radiation length per tracking layer).
- Only thin Al-Kapton printed circuit provide stability
- Sensors thinned to 50µm
- Sensors chips: 2 x 2 cm
- Chips have inactive region for readout on one side, bonded by single point tape automated bonding (SPTAB) to the Al-Kapton printed circuit
- General specifications:
- Momentum resolution 0.5 Mev/c (low momentum particles < 53 MeV/c), vertex resolution ~ 200µm
- Particle flux: 10^9 muon decays / s -> 1.5M hits/s/cm^2 (like 0.04 hits/BC/cm^2), all hits are readout, no trigger
- Radiation tolerance ~ NA
- Chip specifications:
- Pixel size 80µm x 80µm
- Thickness ~ 50µm
- Cooling with helium -> power consumption < 200mW/cm^2

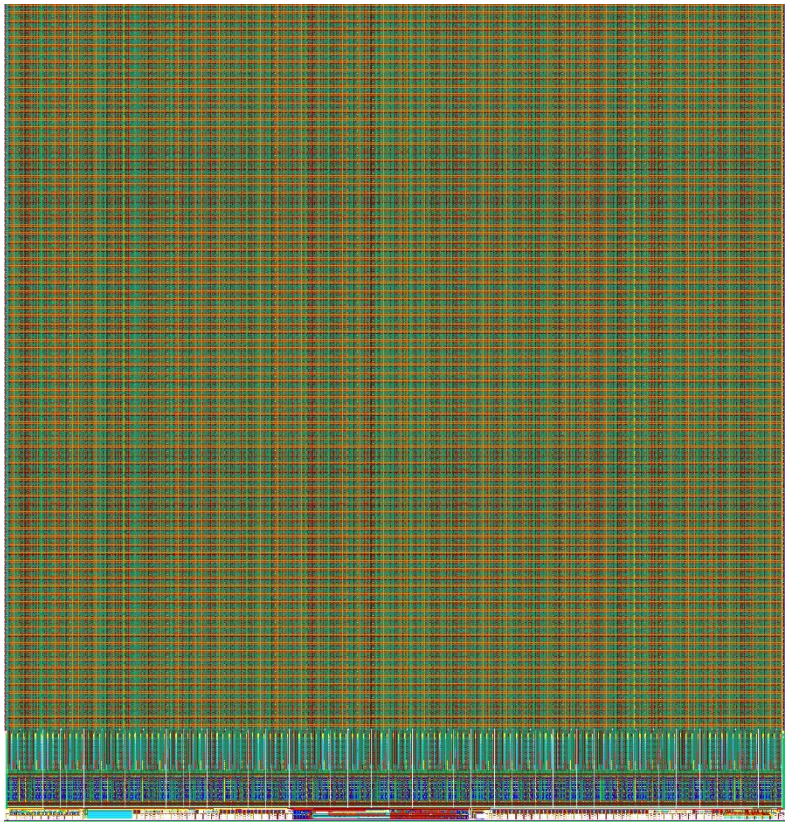


ATALSPIX: Example of a production design

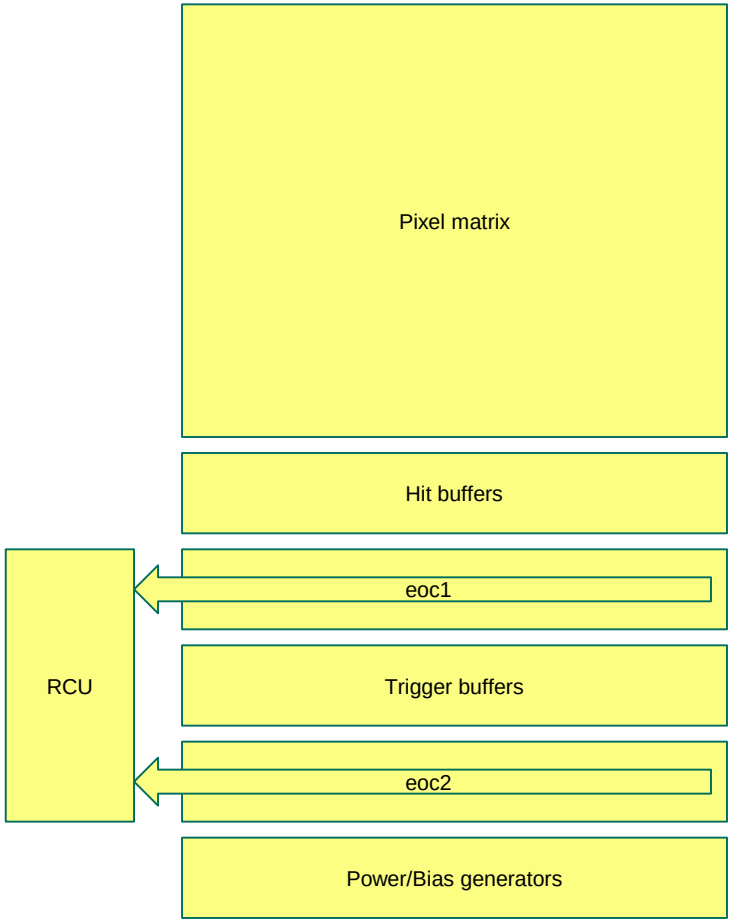


ATALSPIX: Example of a production design

- ATALSPIX3
- HVCMOS sensor for quad module
- Implemented in TSI 180nm HVCMOS technology, licensed IBM/AMS H18 process
- Features and data interface similar as RD53
- Supports triggered readout with trigger latency up to 25µs
- Interface:
- Input CMD line (used for clock generation, L1 triggering with trigger tag, configuring and readback of configuration), like RD53
- Output: Aurora 64b66b, 1.28Gb/s, hit words 32bits, EoE words
- Supports serial powering (only one power supply)
- Size: 20.2mm x 21mm
- Submitted in April 2019



- Chip architecture is shown here: it contains pixel matrix, hit buffers, trigger buffers, digital block (readout control unit), power and bias voltage generators

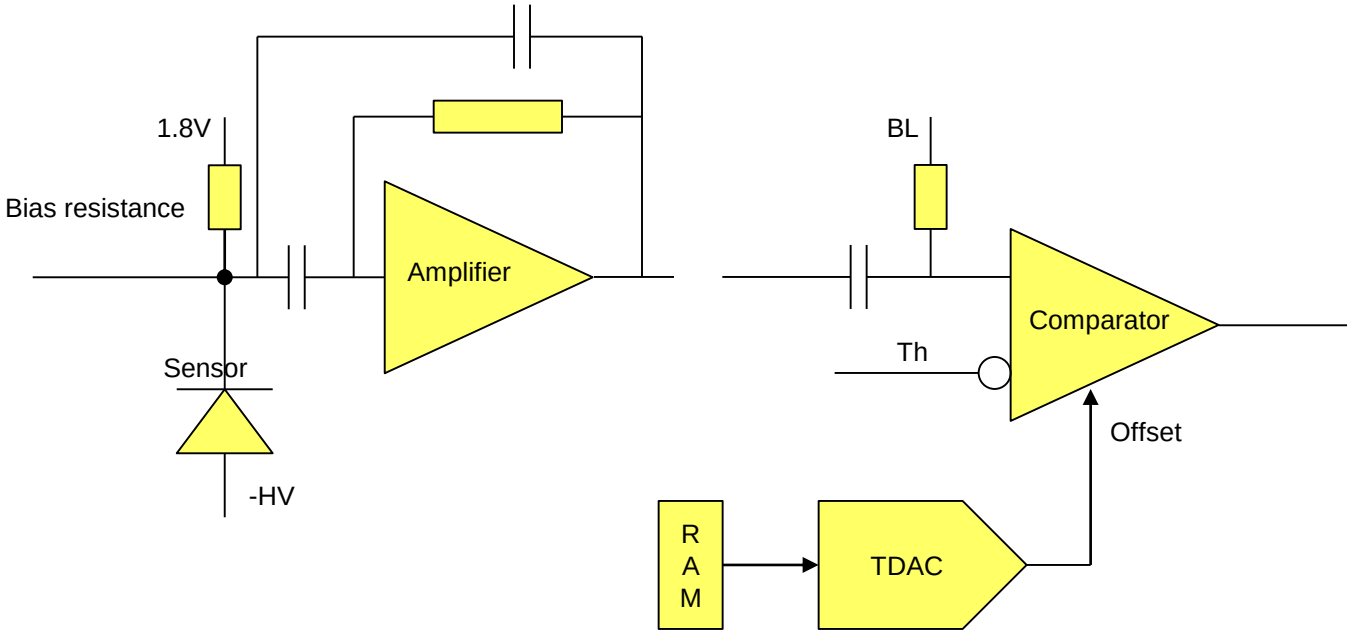


Pixel size (x, y): 150µm x 50µm
Matrix size: 132 x 372

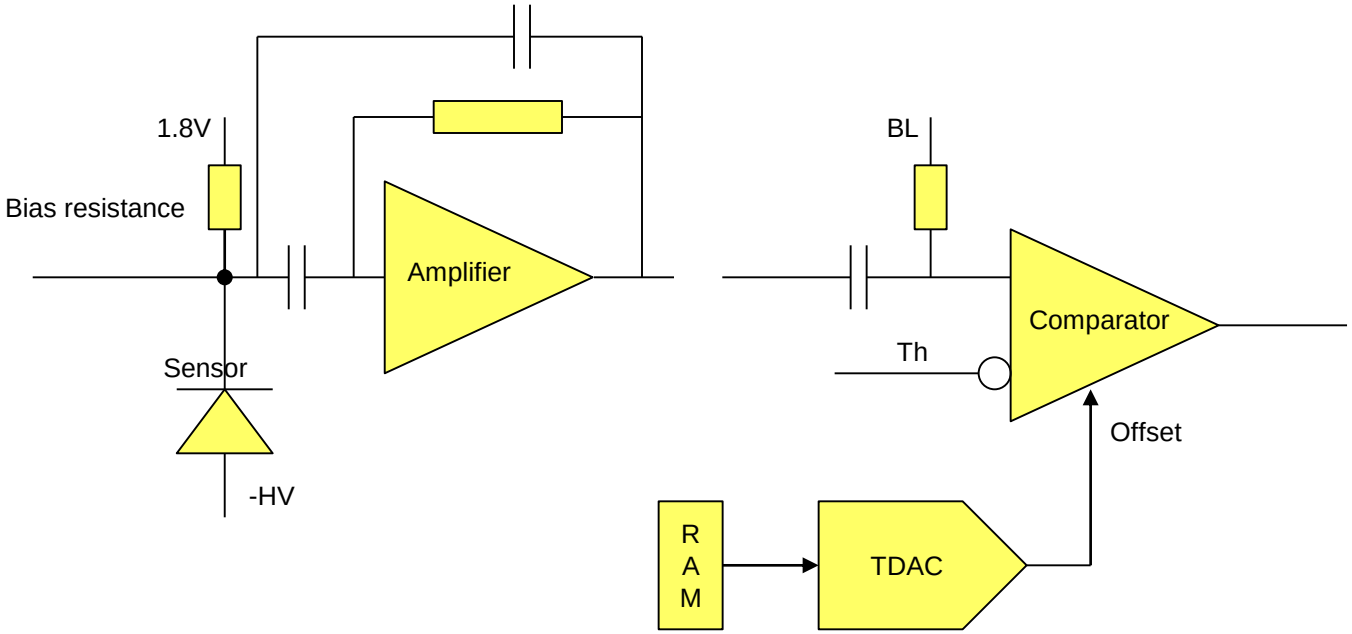
Time stamp: 10 bits, ToT time stamp: 7 bits
TS. frequency: up 80MHz (untriggered), 40MHz (triggered)

Hit word: 9 bit row address, 8 bit column address, 10 time stamp, 7 bit ToT = 34 bits

- Pixels contain continuously running charge sensitive amps.
- This could be compared with DEPFET. In DEPFET, there is also a simple amplifier per pixel. However, only one row is active at a time. In ATLASPIX, the amplifier is always active, it is connected to comparator. This means that the pixel can immediately detect a hit and record a time tamp with short delay after hit
- Advantage of this concept is fast timing (10ns sigma), disadvantage higher power consumption.
- We have about 200mW/cm^2 for ATLASPIX.
- However power consumption depends on time consumption. This means ATLASPIX has time resolution of 25ns and 200mW. The chip can be also done to have 100ns time resolution and 100mW consumption that is simmilar as DEPFET.



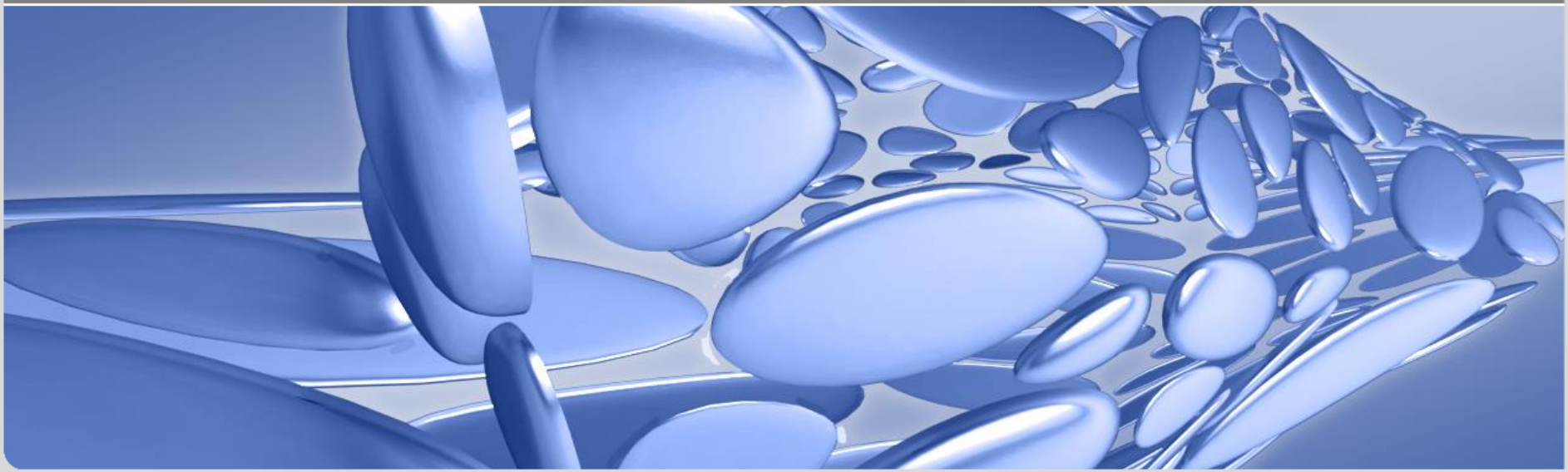
- Comparator is AC coupled to amplifier, it contains threshold tune circuit



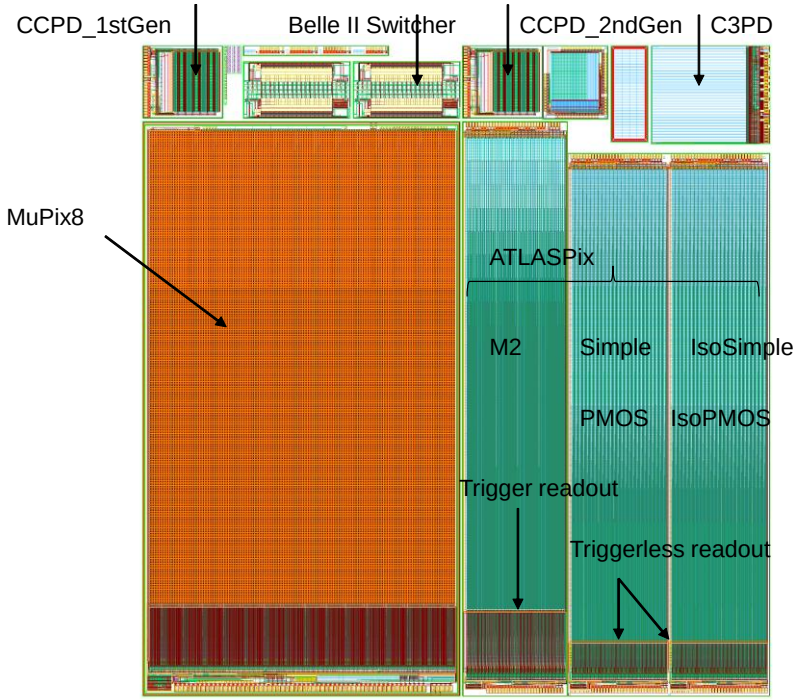
ATLASPIX3 Summary

- ATLASPIX3 has the following properties:
- Chip size: 20.2mm x 21mm
- Active area size: 20mm x 18.6mm
- Periphery height: 2.3mm
- Pixel size: 150µm x 50µm
- Radiation tolerance 100 Mrad and 1 x 10^{15} /n_{eq}
- Readout: triggered (untriggered can be optionally used for testing)
- Analog information: yes (7 bits)
- Time resolution (~ 5ns required, present status 6ns)
- Trigger: up to 4MHz with latency 25µs, trigger window 25ns
- Output data rate: about 0.5 - 1 hit / 25ns / 4cm^2 (after trigger) – one serial link/chip at 1.28gbps
- Typical particle rate: about 1-2 / cm^2 / 25ns or 40 10^6 / cm^2 / s
- By reducing of trigger latency (25µs -> 5µs) the same design can cope with by factor 5 higher particle rate, further improvement is possible by increasing buffer depth

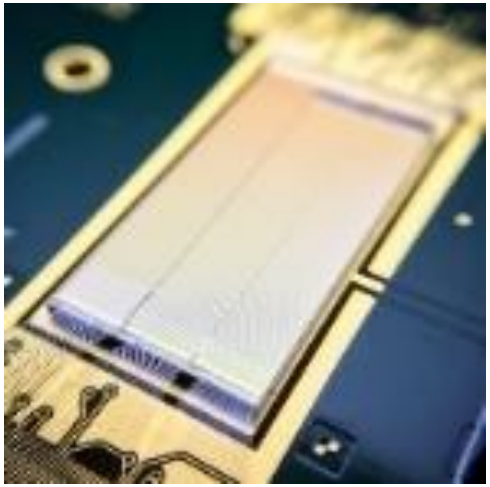
Measurement Results



- Shown the results obtained with MuPix8 and Atlapsix1

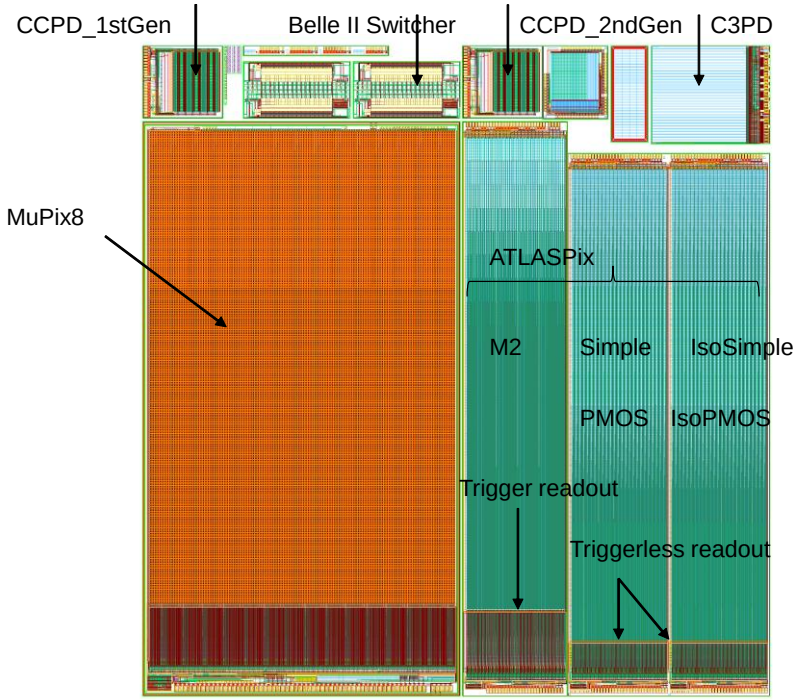


MuPix, ATLASPIX

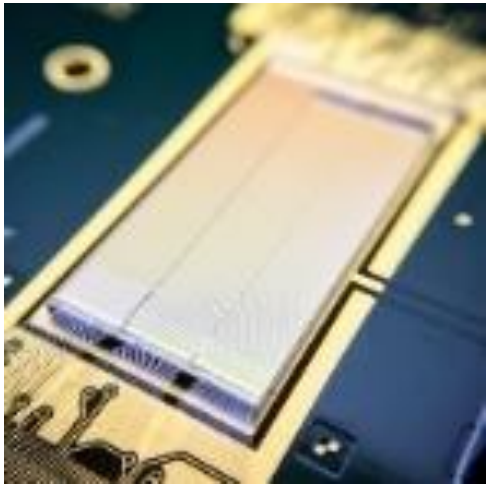


MUPIX8/ATLASPIX1

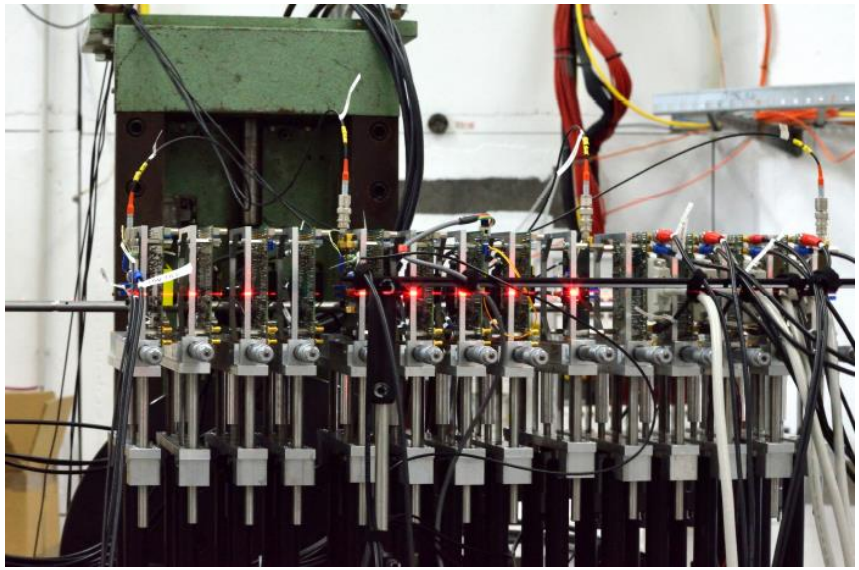
- Two large area prototypes MUPIX8 and ATLASPIX1
- MUPIX8: Area 1cm x 2cm, Pixel matrix: 128 x 200 pixels of 80µm x 81µm size, two matrix types
- ATLASPIX1: two variants: M2 – triggered readout, Simple – untriggered readout (here two flavours “normal” and with isolated PMOS option)
- Example: Simple “normal”: Pixel matrix: 25 x 400 pixels of 130µm x 40µm size
- Submitted within engineering run. Producer AMS. Technology is 180nm HVCMOS, process HV 7sf (H18), variant aH18
- Process has been modified using high resistivity substrate



MuPix, ATLASPIX

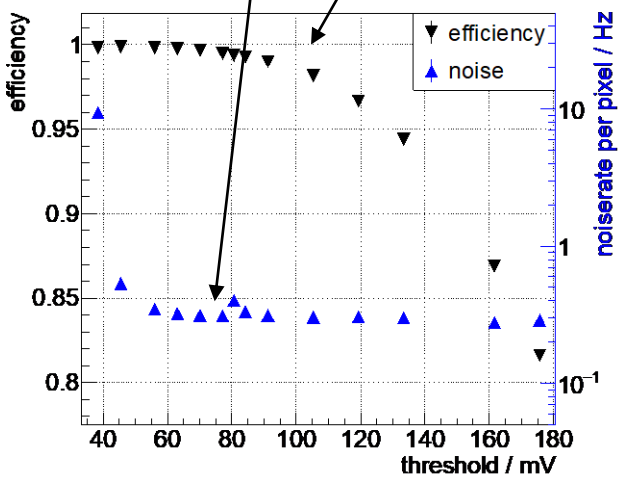


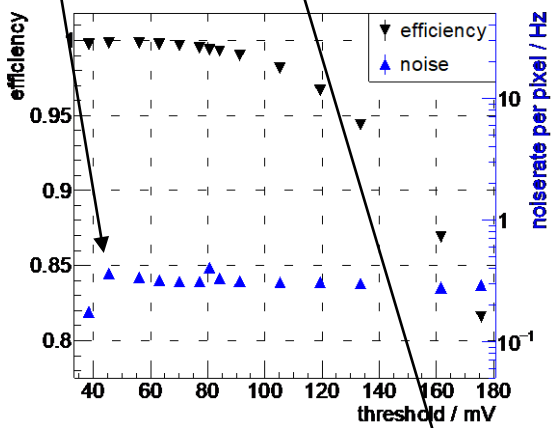
- The efficiency has been measured in beam using MUPIX telescope (developed in Heidelberg)
- Uses 4-8 layers of MUPIX chip, one is device under test (DUT)
- Measurements have been performed at DESY, MAMI and PSI

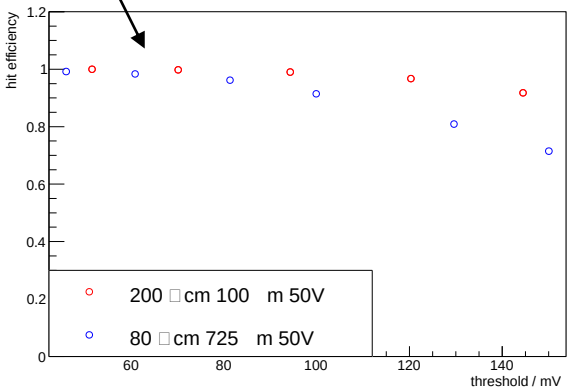


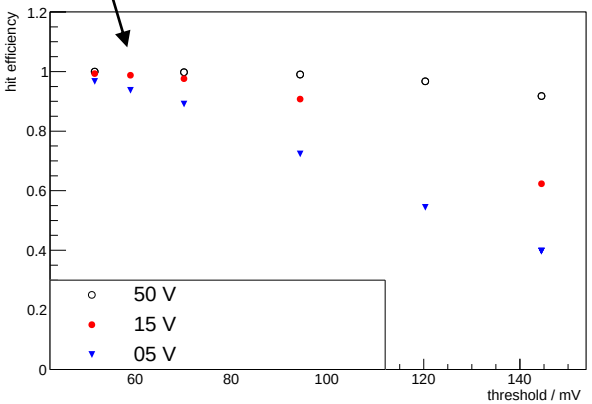
Detection efficiency

- The detector is highly efficient in detection of minimum inonizing charged particles
- The noise is low
- There is a large plateau with high efficiency and low noise.
- Masking of pixels improves noise further
- The efficiency improves with high voltage bias (HV) and with substrate resistivity

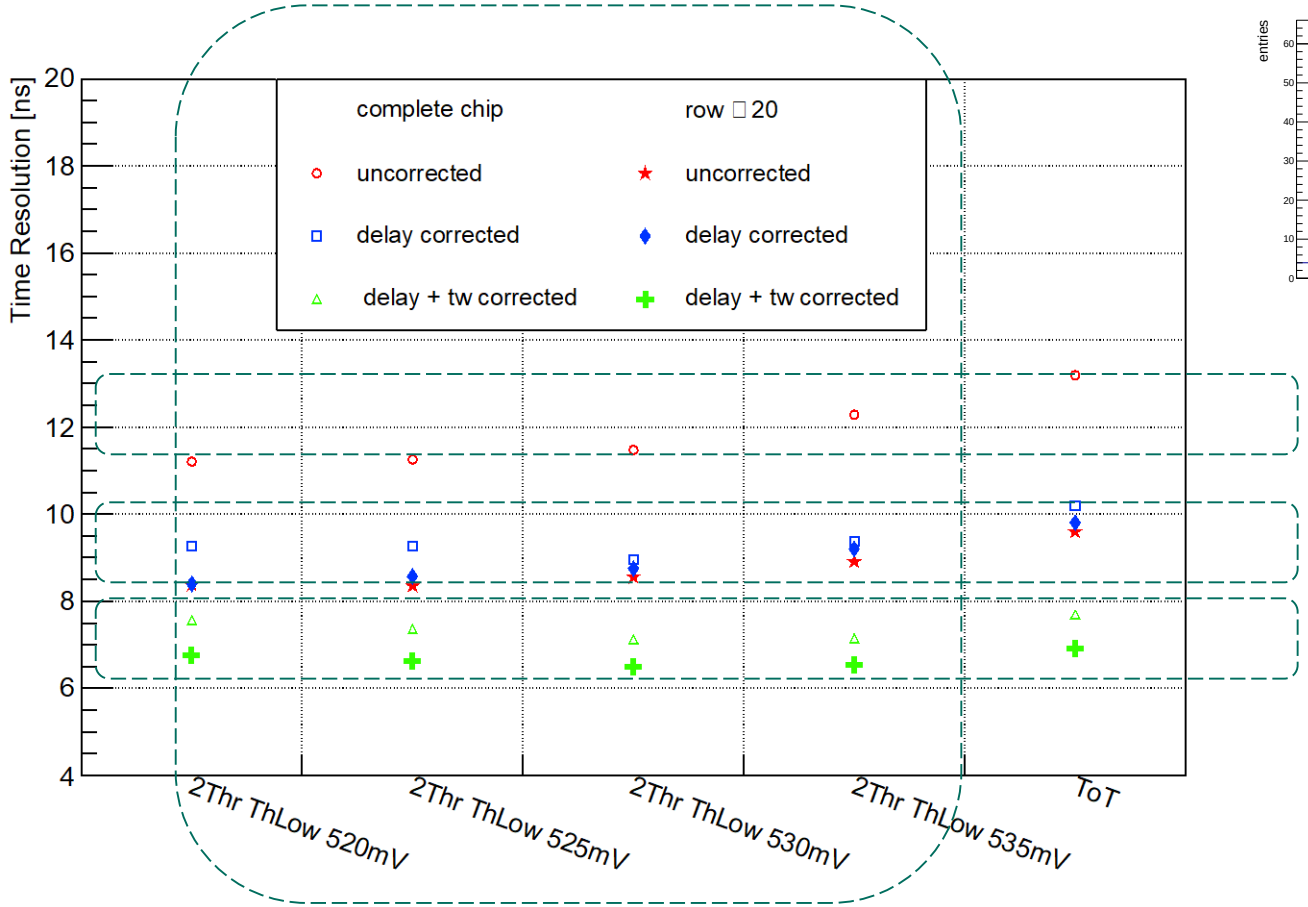


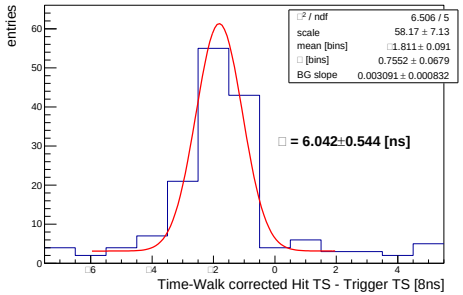






- Using linear correction obtained from the plot time resolution can be improved to ~ 6ns RMS



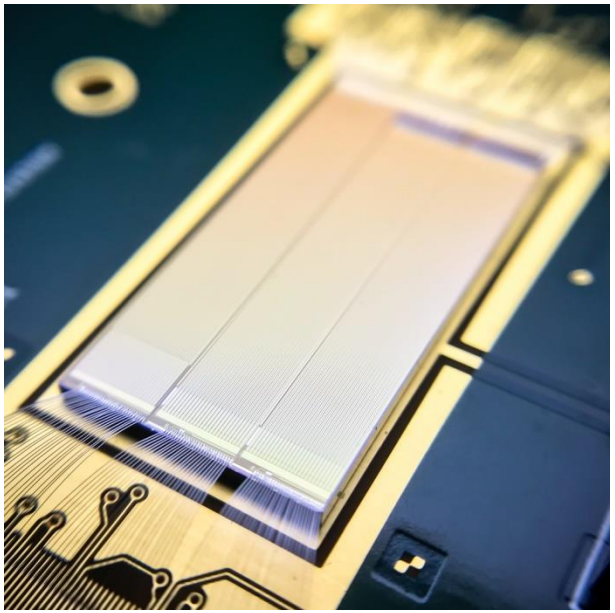


Matrix level time resolution

pixel level time resolution

pixel level time resolution with TOT correction

- ATLASPIX1



Summary of Efficiencies after Irradiation

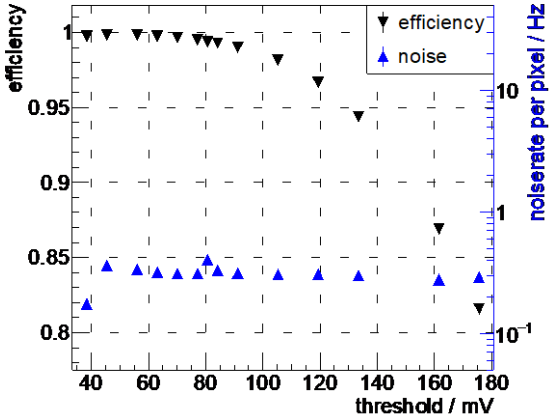
- no tuning of pixels; ≤ 81/10000 pixel masked

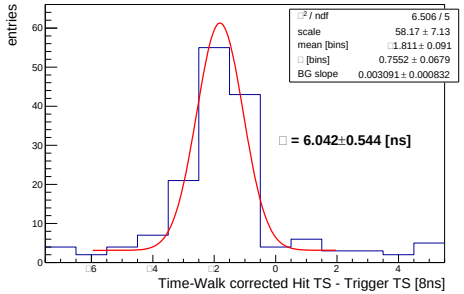
Efficiency$_{40\ Hz}$	sub-strate	thick-ness	bias voltage (#masked pixel)			
fluence (neq/cm^2)	(Ω cm)	(µm)	60 V	70/75 V	80/85 V	90/95 V
n 2e15	80	62	98.5% (81)	98.4% (81)	98.6% (81)	
n 1e15	80	62	99.3% (38)		99.5% (38)	99.5% (39)
n 5e14	80	62	99.5% (19)			
n 2e15	200	100	96.5% (55)		98.7% (60)	98.7% (55)
n 1e15	200	100/725	98.7% (18)	99.4%	99.5%	99.4%
n 5e14	200	100	99.2% (14)			
p 5e14 (50 MRad)	200	100	≥ 99.6% (9)	≥ 99.7% (9)	≥ 99.9% (9)	
p 1e14 (10 MRad biased)	200	725	≥ 99.7%			

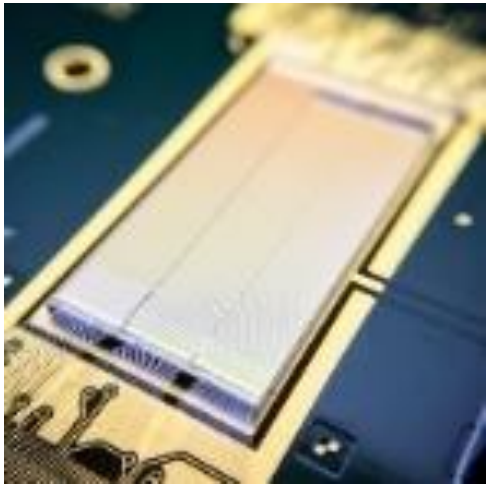
≥ means that the 40 Hz/pixel noise limit was not reached

Summary of measurement results

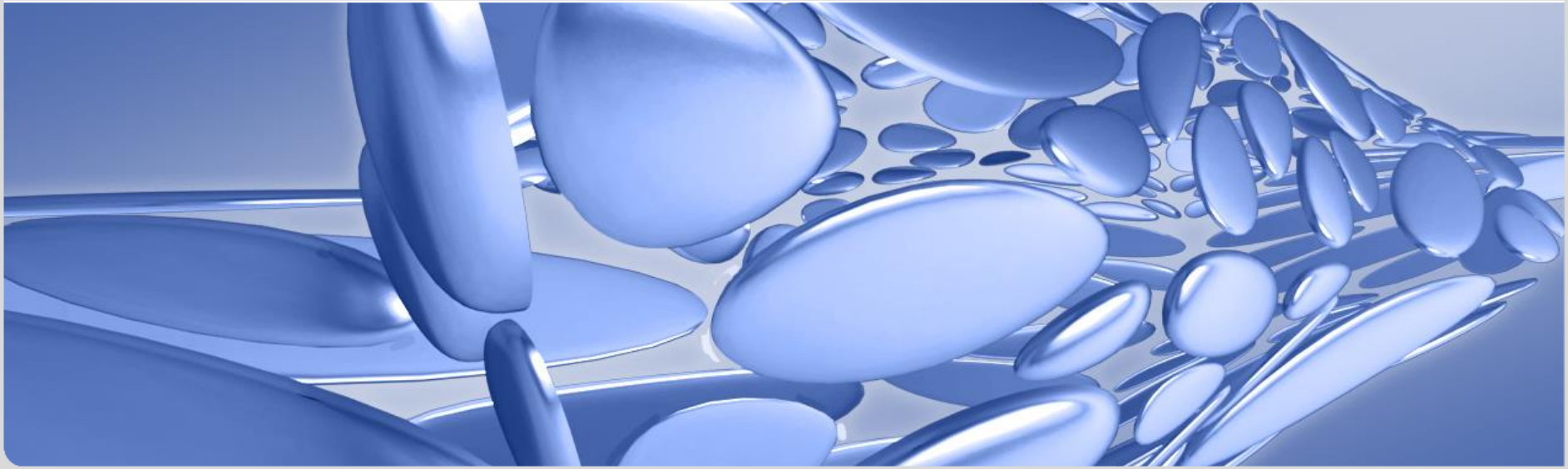
- ATASPIX and MUPX large area designs (MUPIX 1cm x 2cm) work well
- The chips are implemented in HVCMOS process, high resistivity wafer has been used
- The sensors have readout circuits on chip
- Efficiency in beam > 99% for charged ionizng particles.
- Best time resolution achieved with MUPX is 6 ns RMS
- ATLASPIX results will be presented in a separated talk
- We are currently working on the large ATLASPIX3 and MUPIX10 designs







Module concept for Belle II

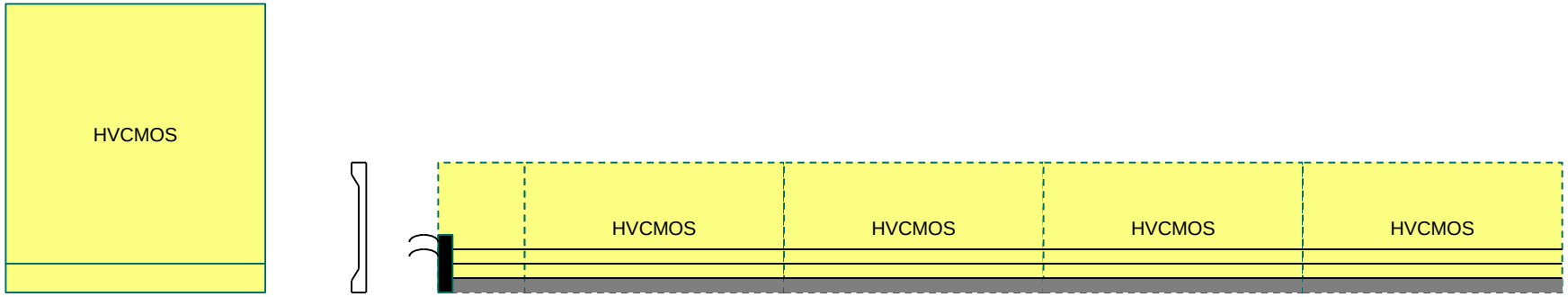


- Module concept for Belle II
- For ATLAS and Mu3e different module concepts are used than in PXD.
- ATLAS is based on quad modules, in case of Mu3e we plan to glue the chips on Kapton PCBs with aluminum lines. Stability is assured by folding

- Here proposed a structure here that is similar as what we have now. We could make multi-reticle CMOS modules. Several chips would be cut from reticle.
- To avoid wire bonding of all chips , we can do additional power and signal lines after CMOS processing. This can be done at IZM.

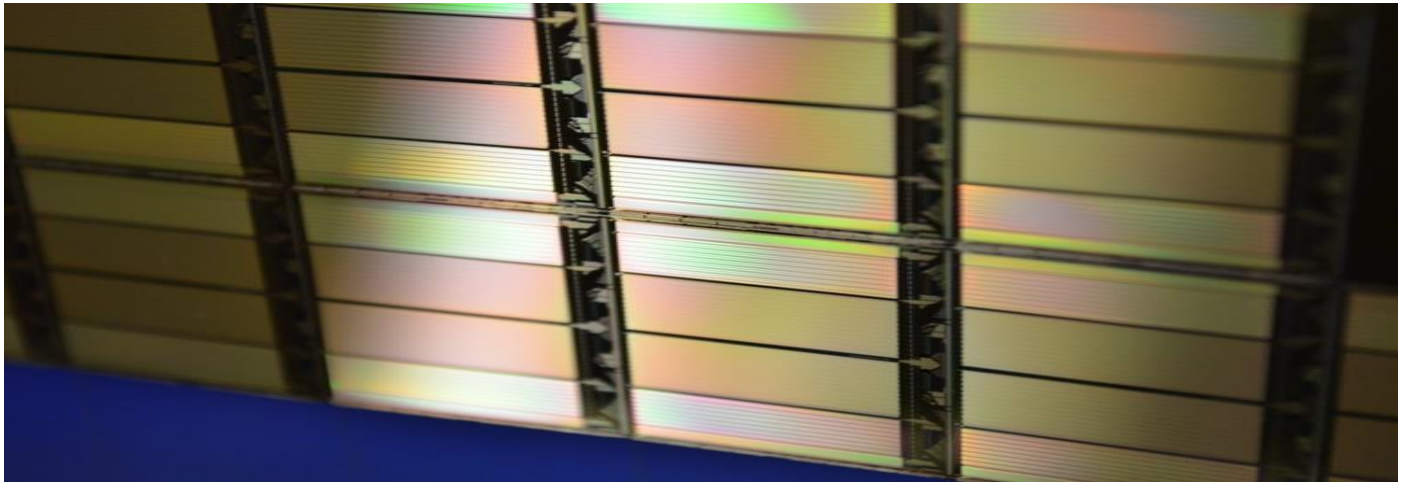
Possible HVCMOS module for Belle II PXD

- Module for Belle II can be based on ATLAS design
- Belle module could consist of 4 - 5 reticles with, each ca. 2cm x 1cm size
- Matrix height would be two times smaller than in the case of ATLAS -> easier design, smaller periphery
- Pixel size ~ 50µm x 50µm

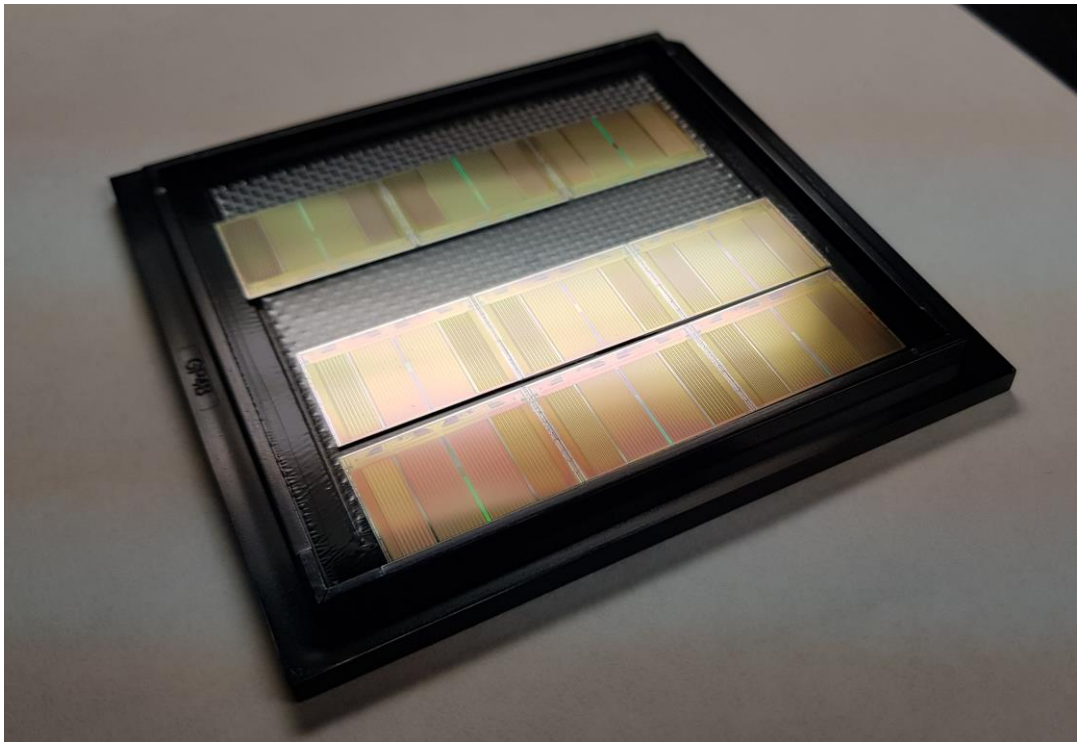


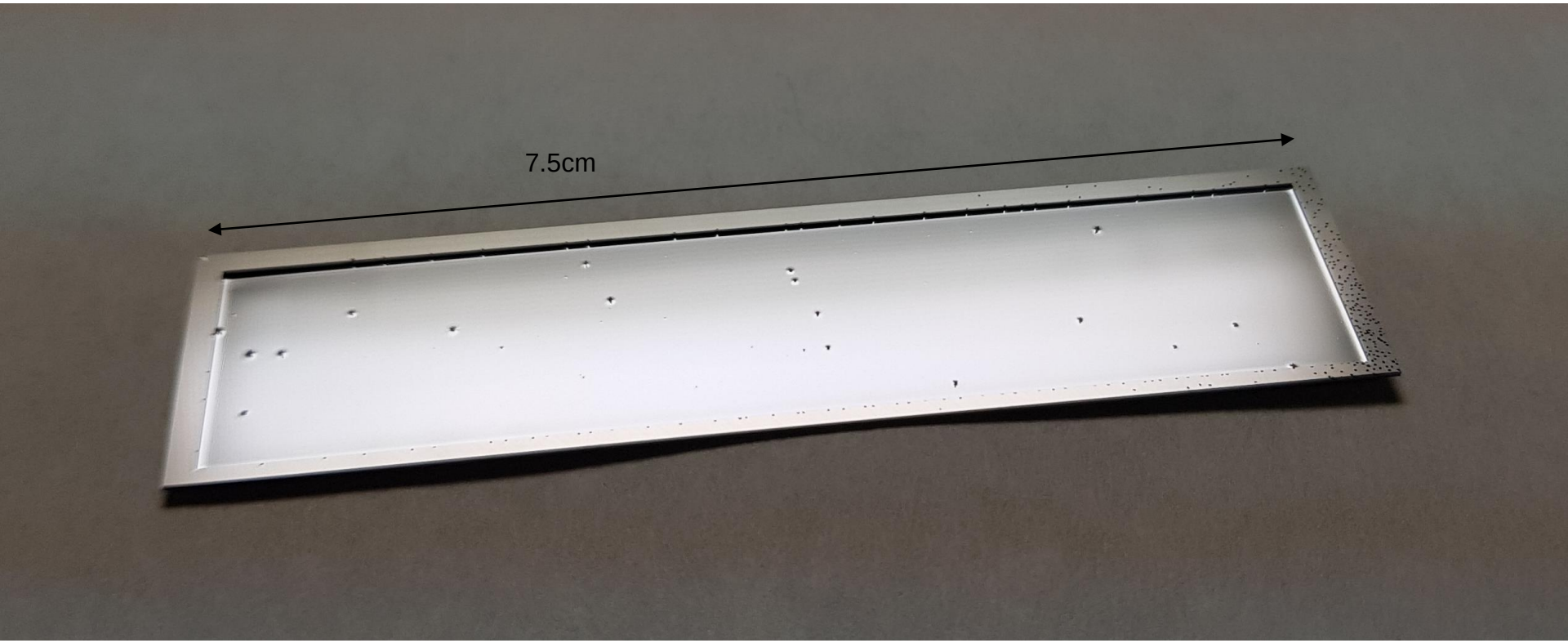
- Another nice feature of DEPFET module is that it has he thick frame and thin active region. This assures mechanical stability
- The question, is can it be done on CMOS as well?
- To test this we have send several wafers to IZM Berlin. We have used an older HVMOS design (350nm) technology H35DEMO. This was the first HVCMOS engineering run
- (ATLASPIX1 was at this moment in production)
- HV35DEMO is a chip of 2 x 2 cm, size with several matrix types. Similarly to ATLSPIX we have nice results. However, large technology 350nm leads to a bit large power consumption
- IZM has performed patterning of the backside so that we have an active region of 100µs and frame
- The modules are mechanically stabile

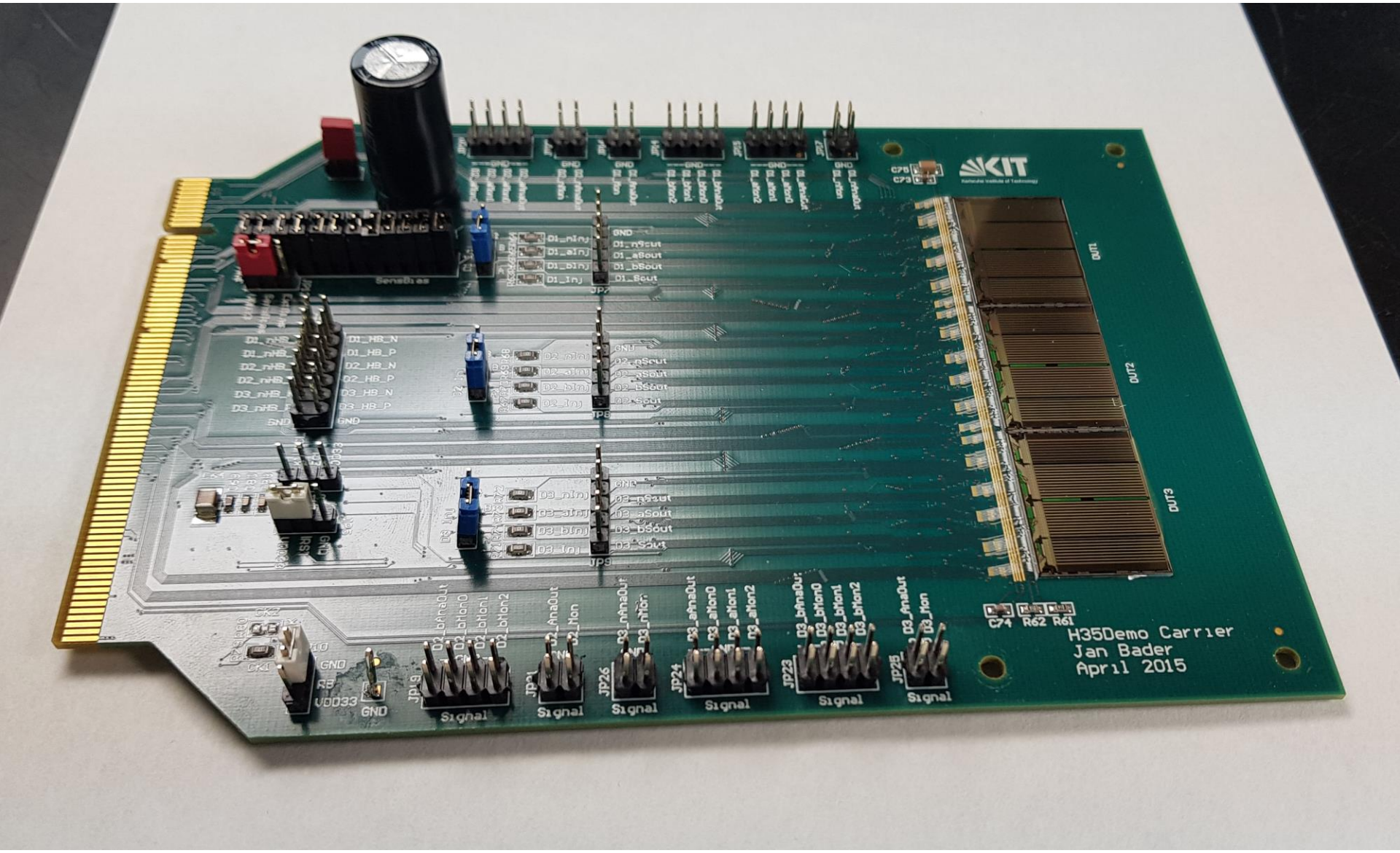
[1] Benoit, M., et al.; Test beam measurement of ams H35 HV-CMOS capacitively coupled pixel sensor prototypes with high-resistivity substrate; Journal of Instrumentation 13(12),P12009; 2018

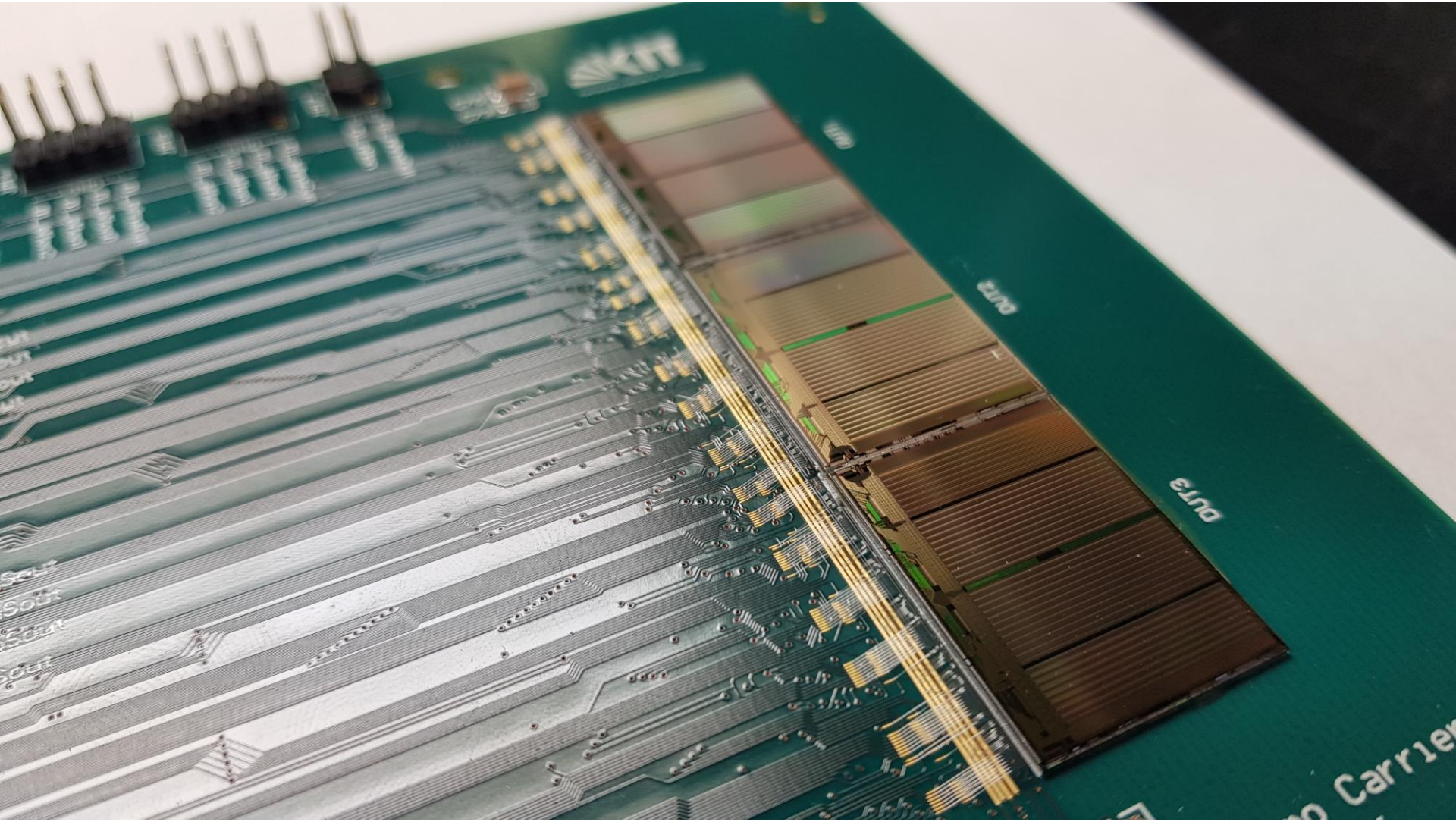


- In the next slides we see the module structure and the system

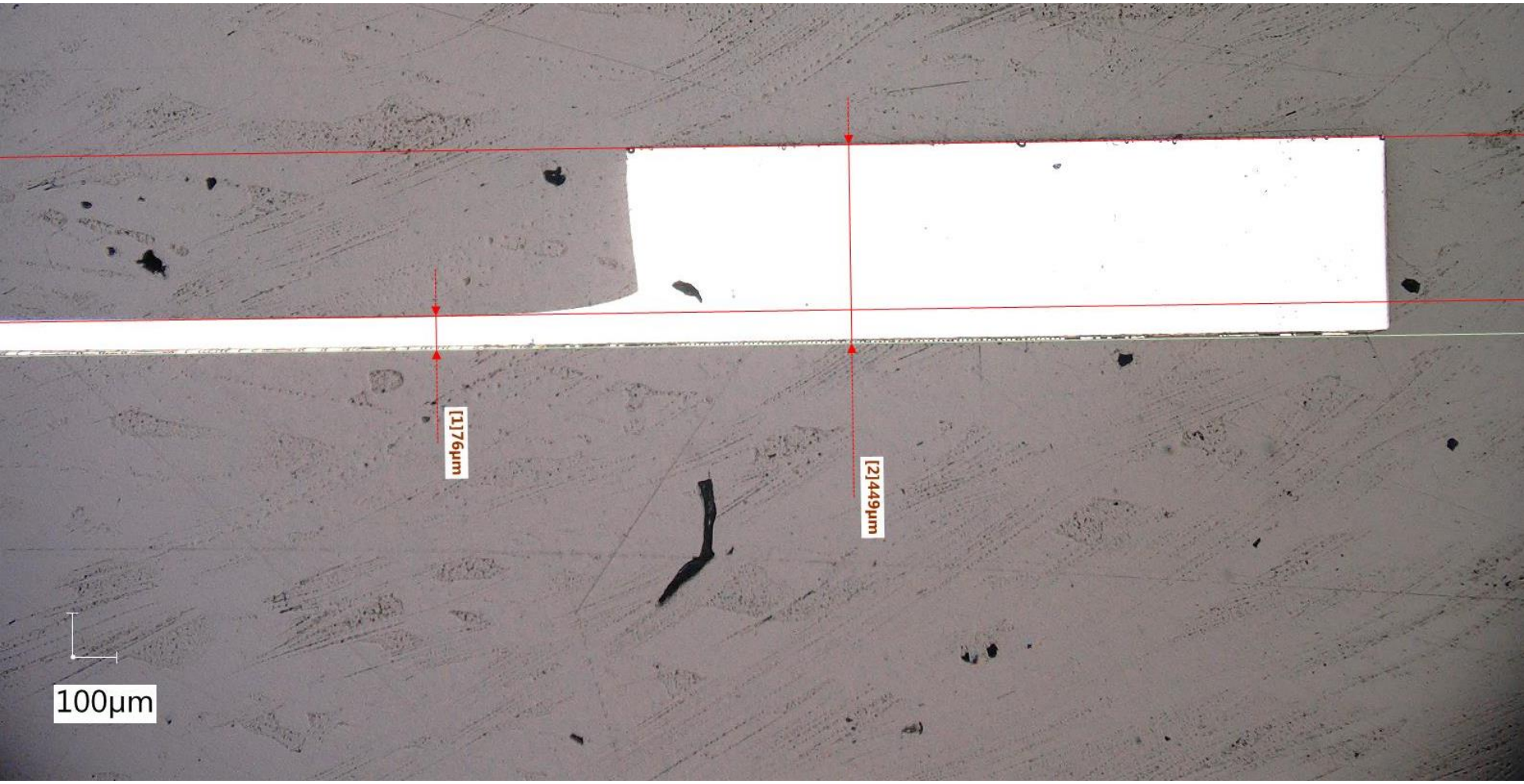


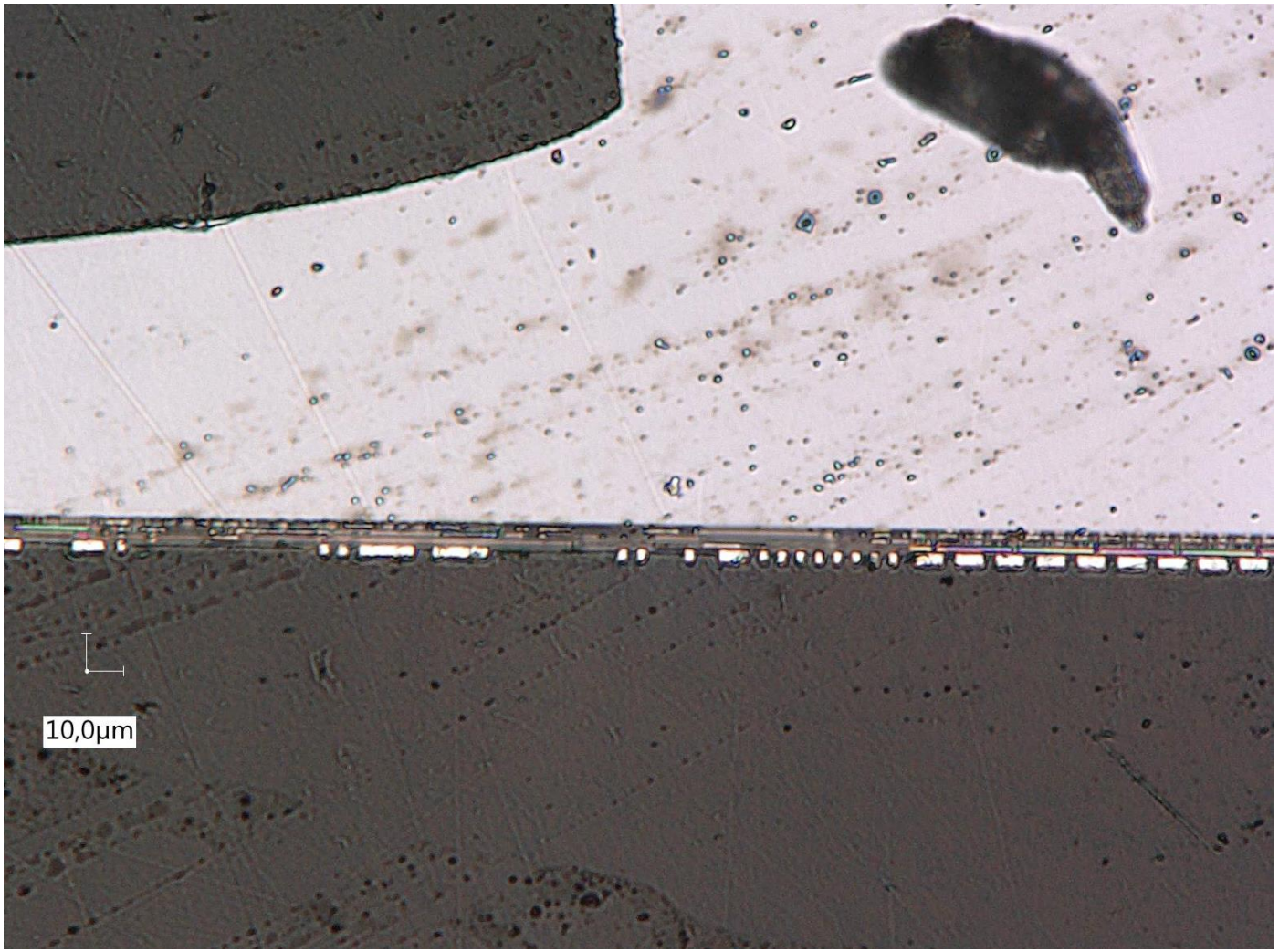

7.5cm


H35Demo Carrier
Jan Bader
April 2015
OUT1
OUT2
OUT3
JP19
JP21
JP26
JP24
JP23
JP25
Signal
Signal
Signal
Signal
Signal
Signal

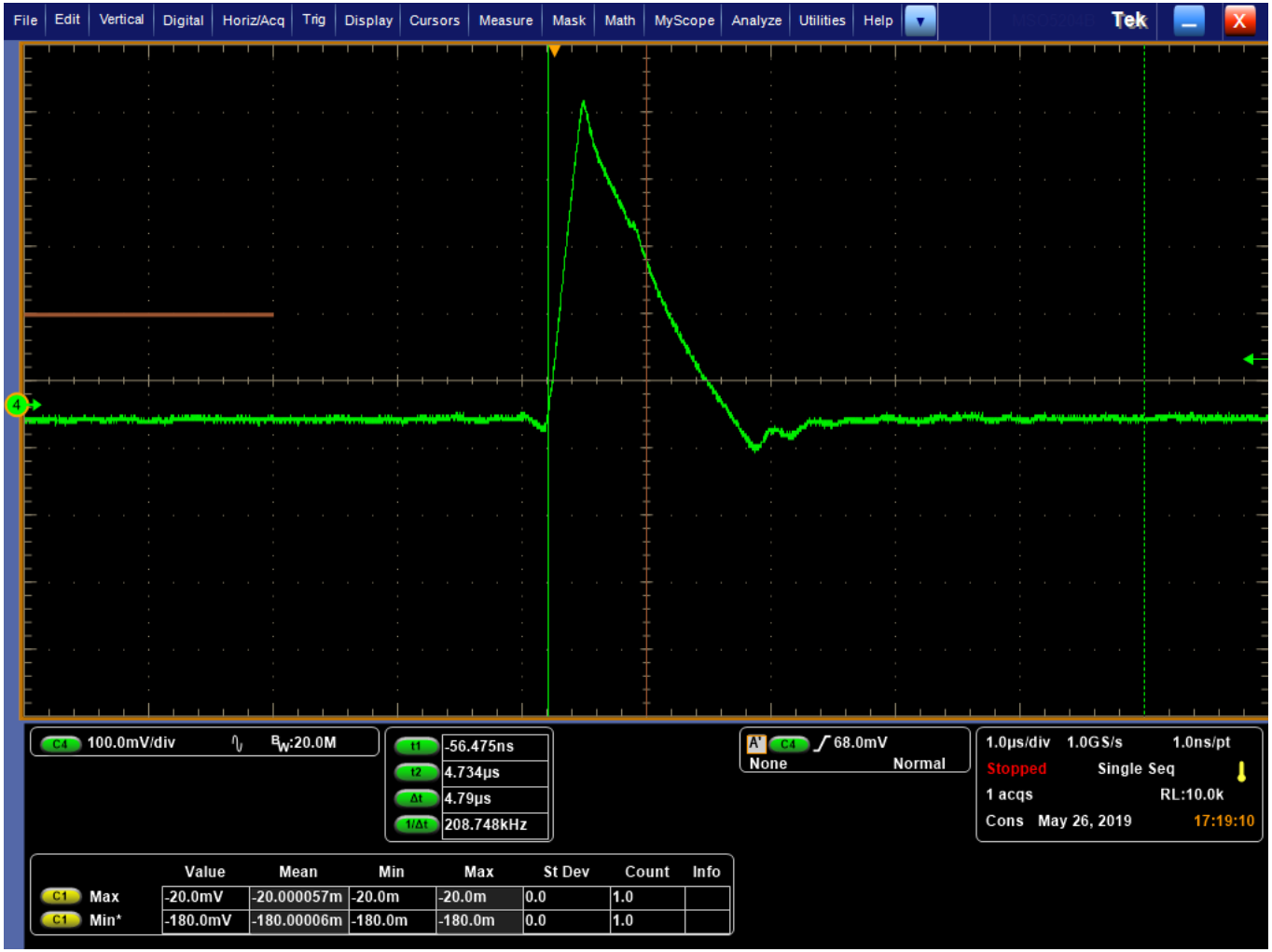

KIT
DUT2
DUT3

- The module was cut and the cross section measured
- Thickness in active region 76µm



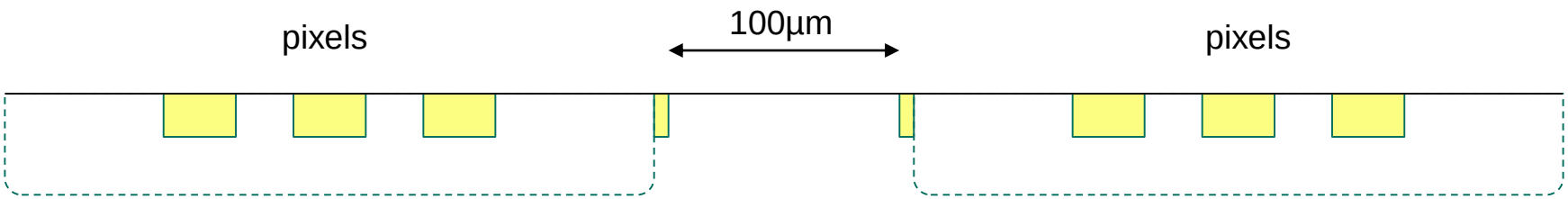

10,0µm

- We have tested one chip and it seems to work well. We see that it is possible to operate a pixel. Configuration works



Gap between chips

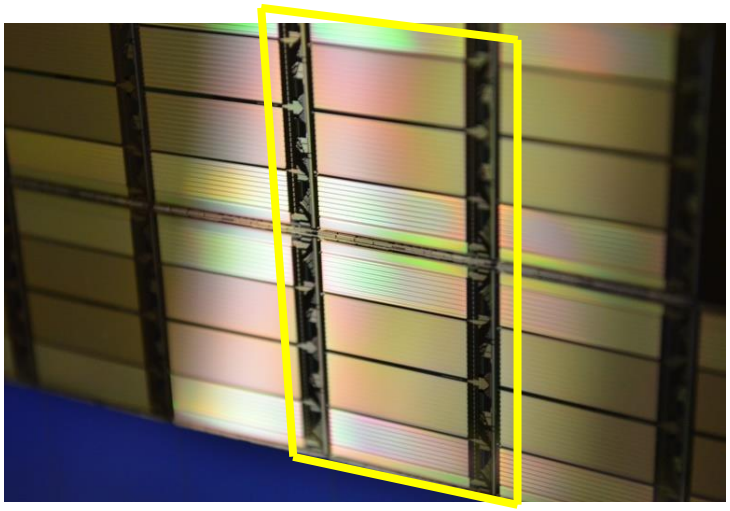
- Gap between chips is probably not a serious issue

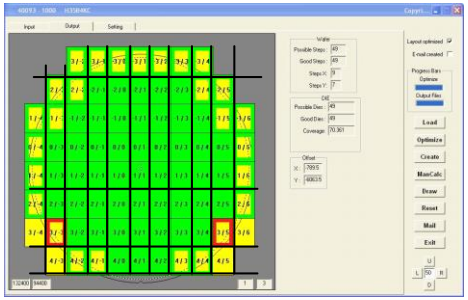


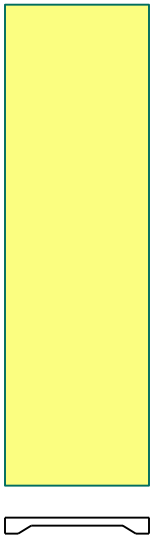
Multi reticle thin modules - Summary

- Thinning and inter-reticle connections can be done at IZM
- First multichip sensor structure with the profile similar as DEPFET produced (only thinning)
- The module would be compatible with present mechanics

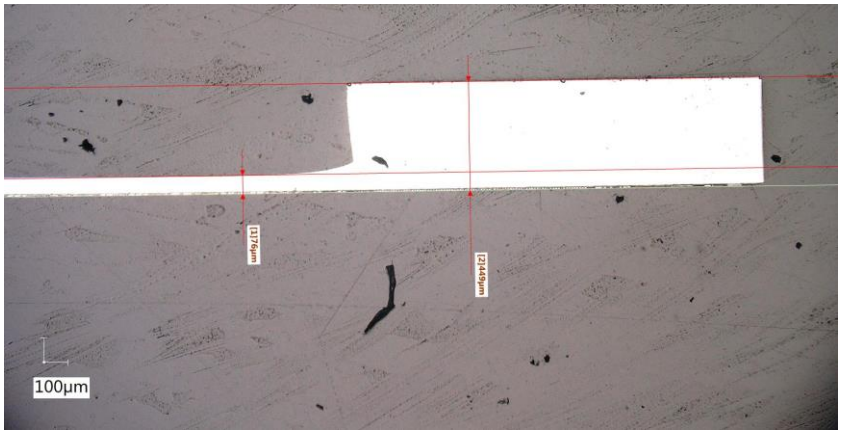
HVCMOS pixel sensor in H35 technology



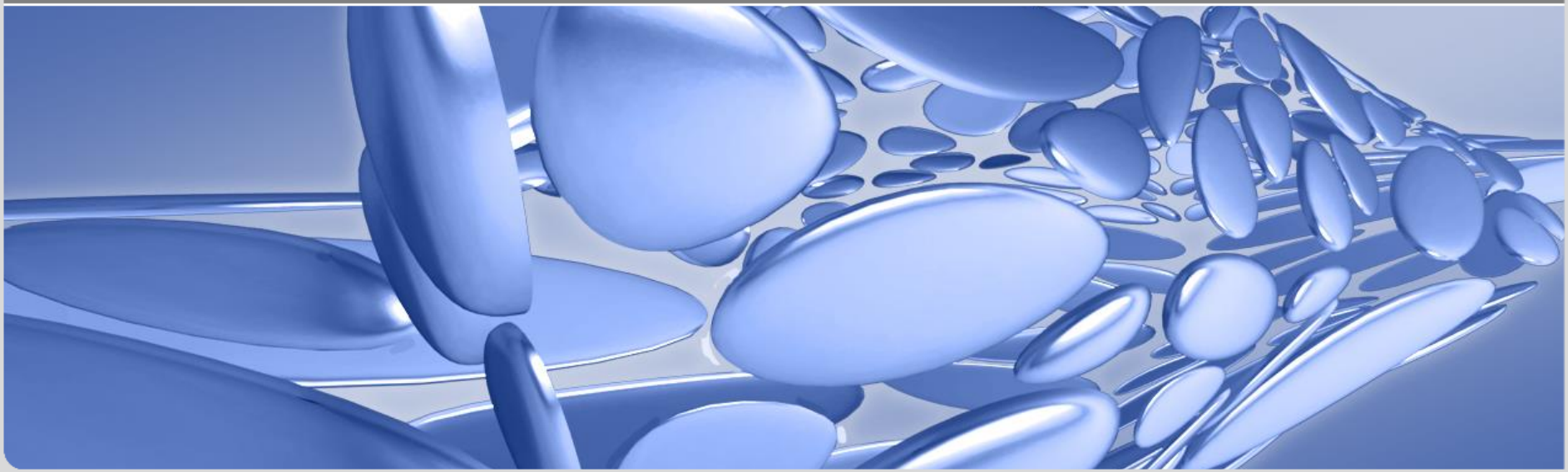




Thinning at IZM – first try

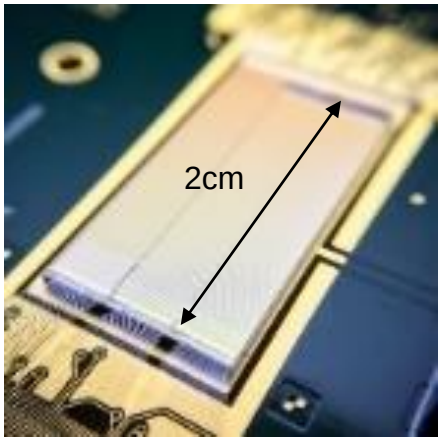


Summary

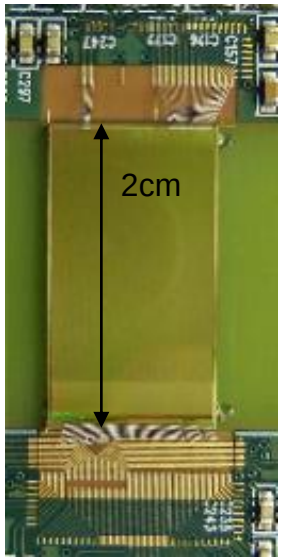


Summary

- HVCMOS will be used for Mu3e experiment and are proposed for Layer 4 of ATLAS
- Mu3e requires production start in 2020 -> technology will be ready till then
- Specifications for Belle II are similar as specifications for ATALS
- Belle II sensor module can be based on the ATLAS sensor design
- Present status for ATLAS and Mu3e
- We have successfully tested reticle-size sensors produced in 180nm HVCMOS technology
- We have measured > 99% detection efficiency after proton and neutron irradiations
- Time resolution is of the order of RMS = 6ns (zero suppressed readout on pixel level with time measurement, not a rolling shutter)
- Power consumption depends on amplifier on-chip setting and can be ~ 100mW/cm^2 (switchers consume similar power presently)
- Several foundries can produce the sensors: TSI (main option) (TSI has done reticle stitching, engineering runs not expensive 100k, wafer cost 1.4k)
- Production of multireticle modules seems to be possible



ATLASPIX1



MUpix

ATLASPIX3

H35DEMO thinned at IZM

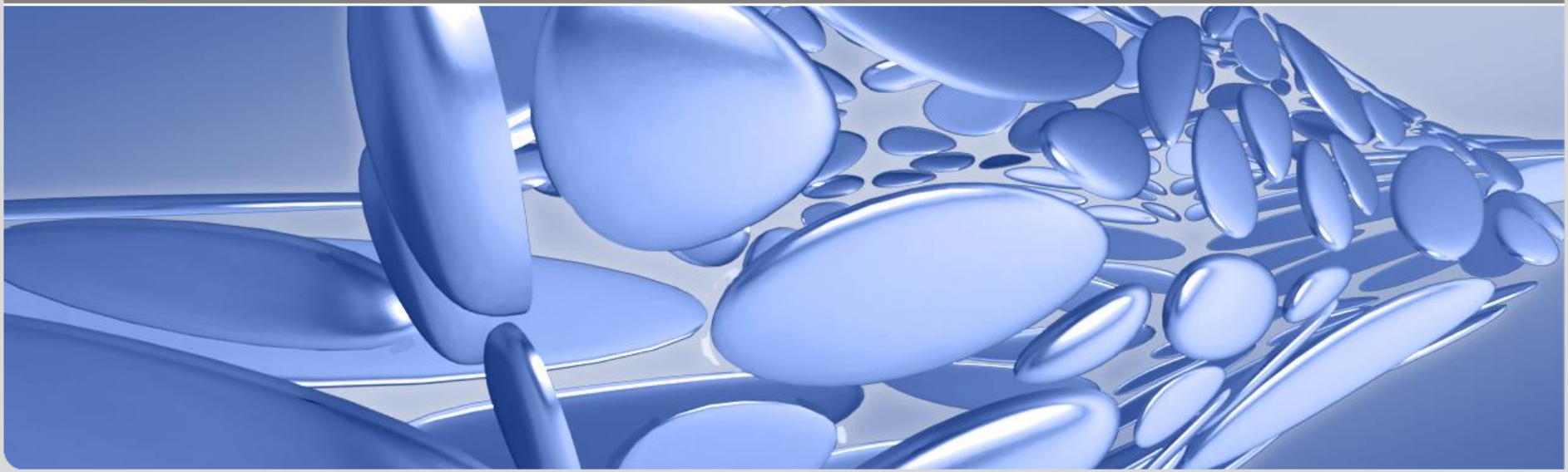
Comparison of specifications

	Belle II DEPFET	HL - ATLAS layer 4 HVCMOS	Belle II upgrade HVCMOS
Trigger	20kHz (50µs)	Up to 4MHz (0.25µs)	200kHz (5µs) ?
Trigger latency	5µs	25µs	5µs ?
Time resolution	20µs	25ns	100ns
Occupancy	1 hit / cm^2 /25ns	1-2 hit / cm^2 /25ns	10 hits / cm^2 /25ns ?
Readout	Rolling shutter	Zero suppressed	Zero suppressed
Readout rate		4 * 2/25ns * 25ns/250ns = 0.8hits/25ns	4 * 10/25ns 100ns/5µs = 0.8hits/25ns

Proposed project plan

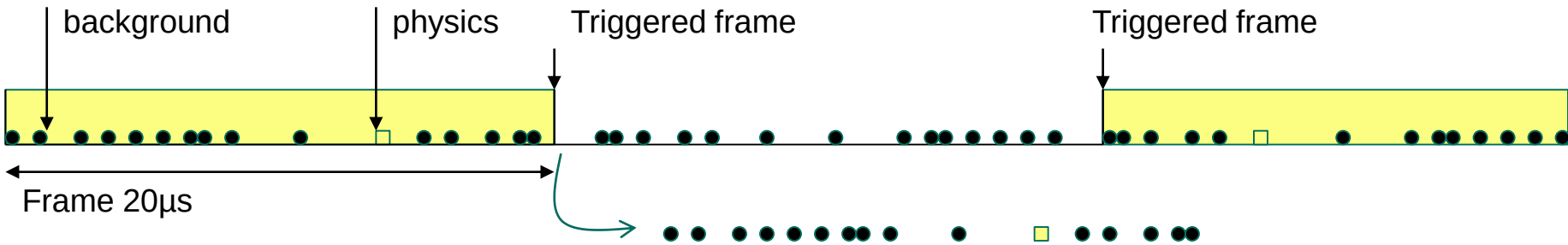
- We could start from ATLASPIX, halve the pixel size. Change the geometry. All these changes are not difficult. The engineering run cost is 50k (shared between two projects)
- We could then send modules to IZM, where the backside processing and redistribution can be done
- Time resolution would be 100ns instead of 20µs, chips need only one power supply + HV
- Modules available in 2020

Backup slides



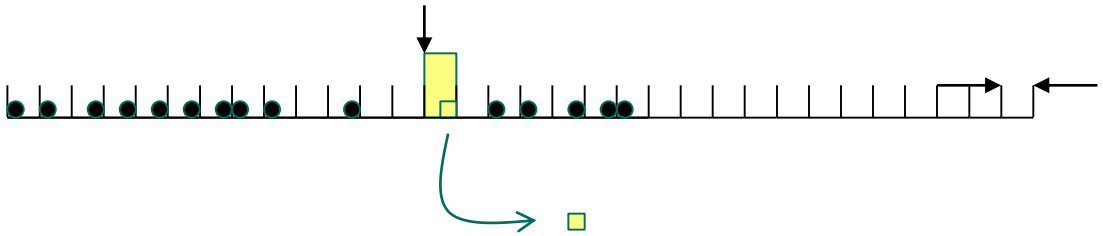
Comparison of sensors

- HVCMOS sensor can cope with increased luminosity
- Slow pions can be detected by measuring amplitude



Triggered DEPFET frame: a few % of transmitted hits are relevant for physics, majority are background

Triggered HVCMOS event, nearly only hits relevant for physics are transmitted



Triggered HVCMOS event, ~ only hits relevant for physics are transmitted