Future of the EDet.

Would the result of our work be competitive

in two years from now?

"My dear, here we must run as fast as we can, just to stay in place. And if you wish to go anywhere you must run twice as fast as that."

Lewis Carroll, "Alice in Wonderland"

Future of the EDet.

True 80k acquisition.
Is it possible?

The data is already there. All we need is to bring it to a storage.

Future of the EDet.

Back-to-front end electronics overview.

Overall data stream for 1M device is in the order of 84 GB/s or 670 Gb/s + overhead.
What are the approaches able to handle such streams?

1. Bufferization in fast memory (DRAM) and „slowly“ writing to a disk system. HMC technology.
2. Writing to a disk system on-the-fly.
3. On-the-fly data classification marking the data for being written (AI).

Future of the EDet.

Back-to-front end electronics overview.

Is it feasible to form such a stream of data?

A technologie we have already in house is 10G ethernet.
The market offers throughput/cost effective FPGA-based solutions able to handle 20x10G.

Future of the EDet.

DCD-FPGA interface.

Is it possible to receive the data from DCD by FPGA?

DCD:

$$V_{OH} = 1{,}24\,V$$

$$V_{OL} = 1{,}00\,V$$

FPGA:

r Single-ended POD10 and POD12 I/O Standards

V_{IL}		V_{IH}	
	V, Max	V, Min	
	V_{REF} - 0.068	V_{REF} + 0.068	
	V_{REF} - 0.068	V_{REF} + 0.068	

Future of the EDet.

DCD-FPGA interface.

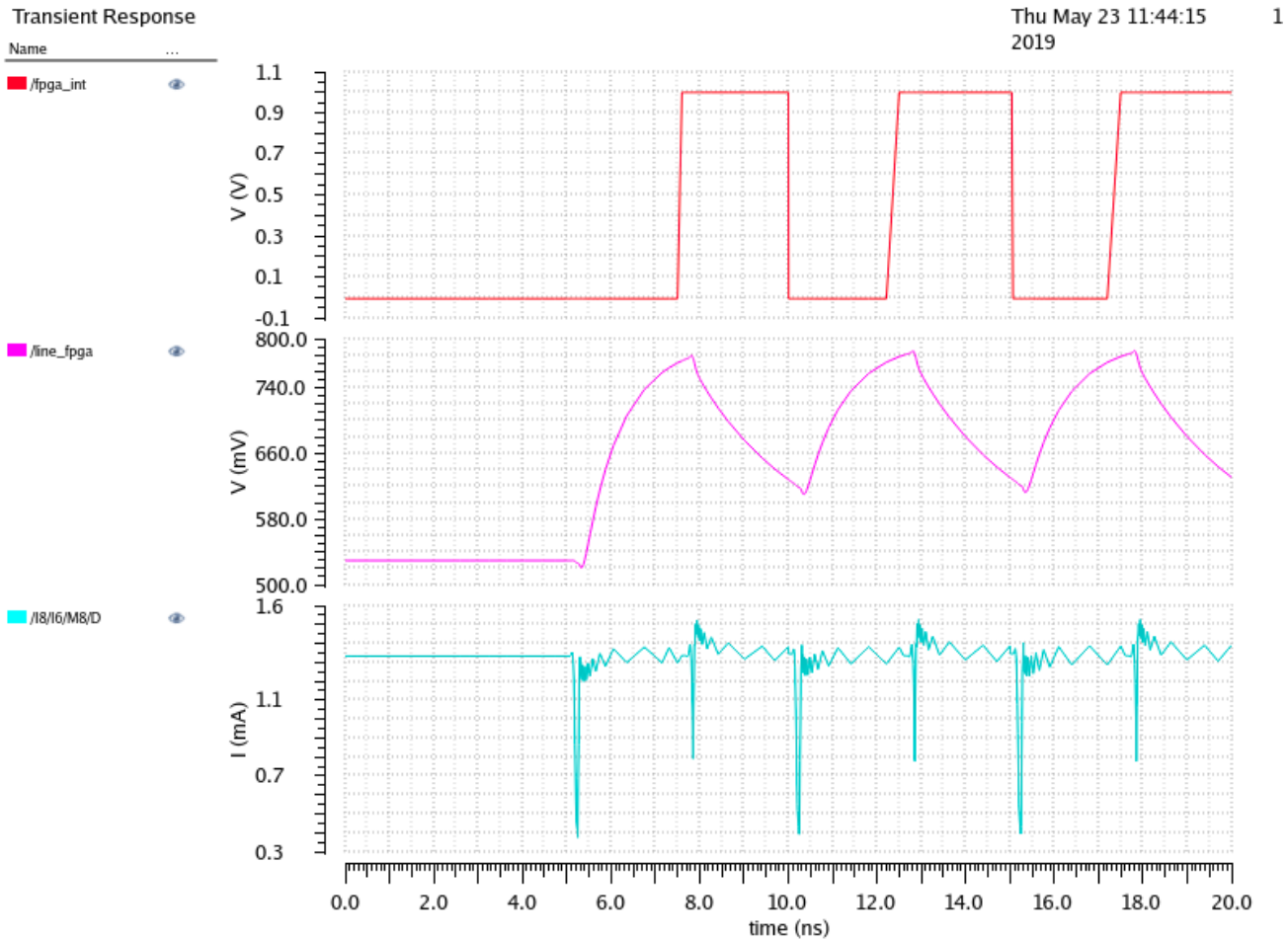
Is it possible to receive the data from DCD by FPGA?

Let‘s take a look onto simulations.

Future of the EDet.

DCD-FPGA interface.

DCD output.

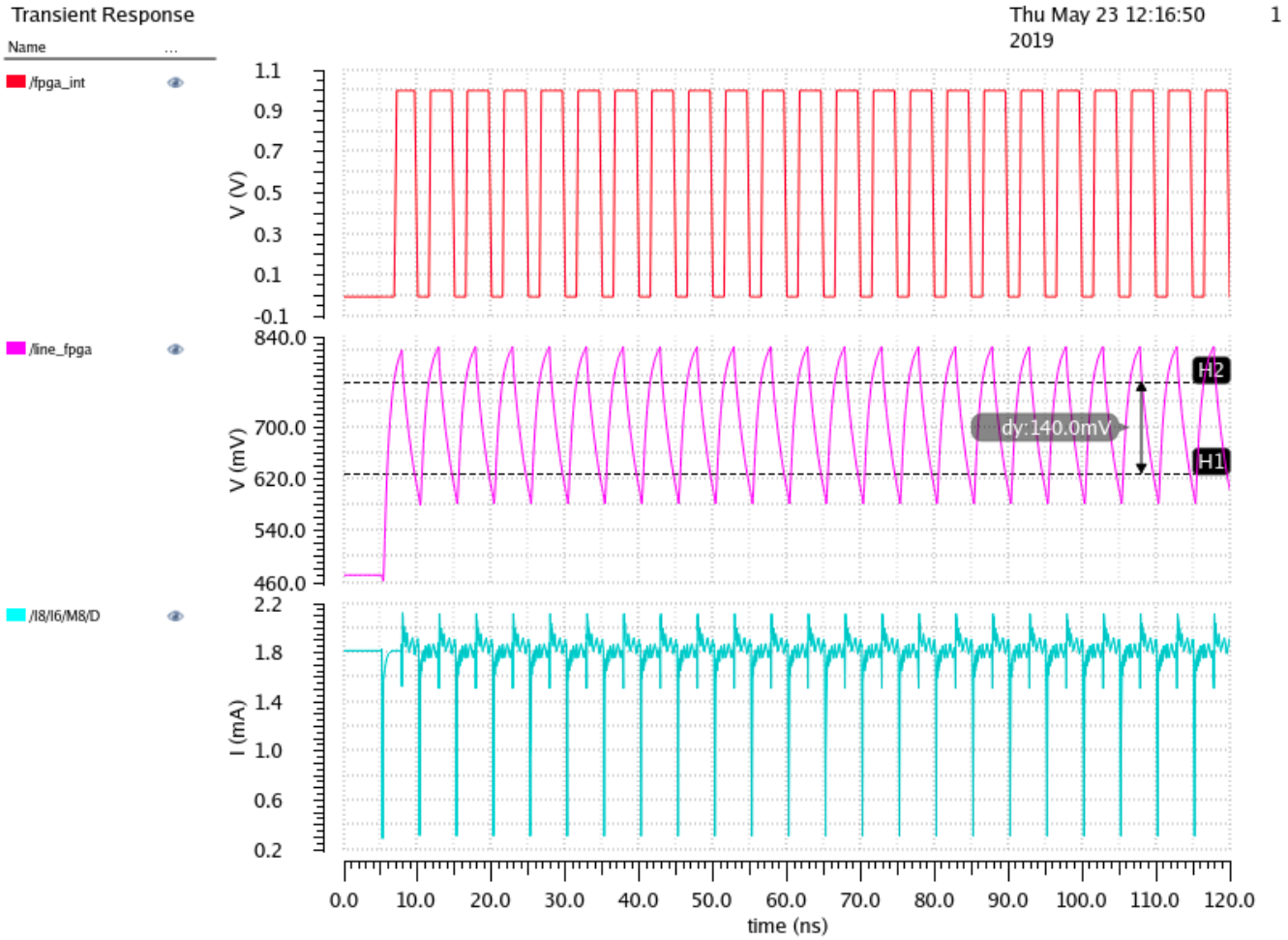


Future of the EDet.

DCD-FPGA interface.

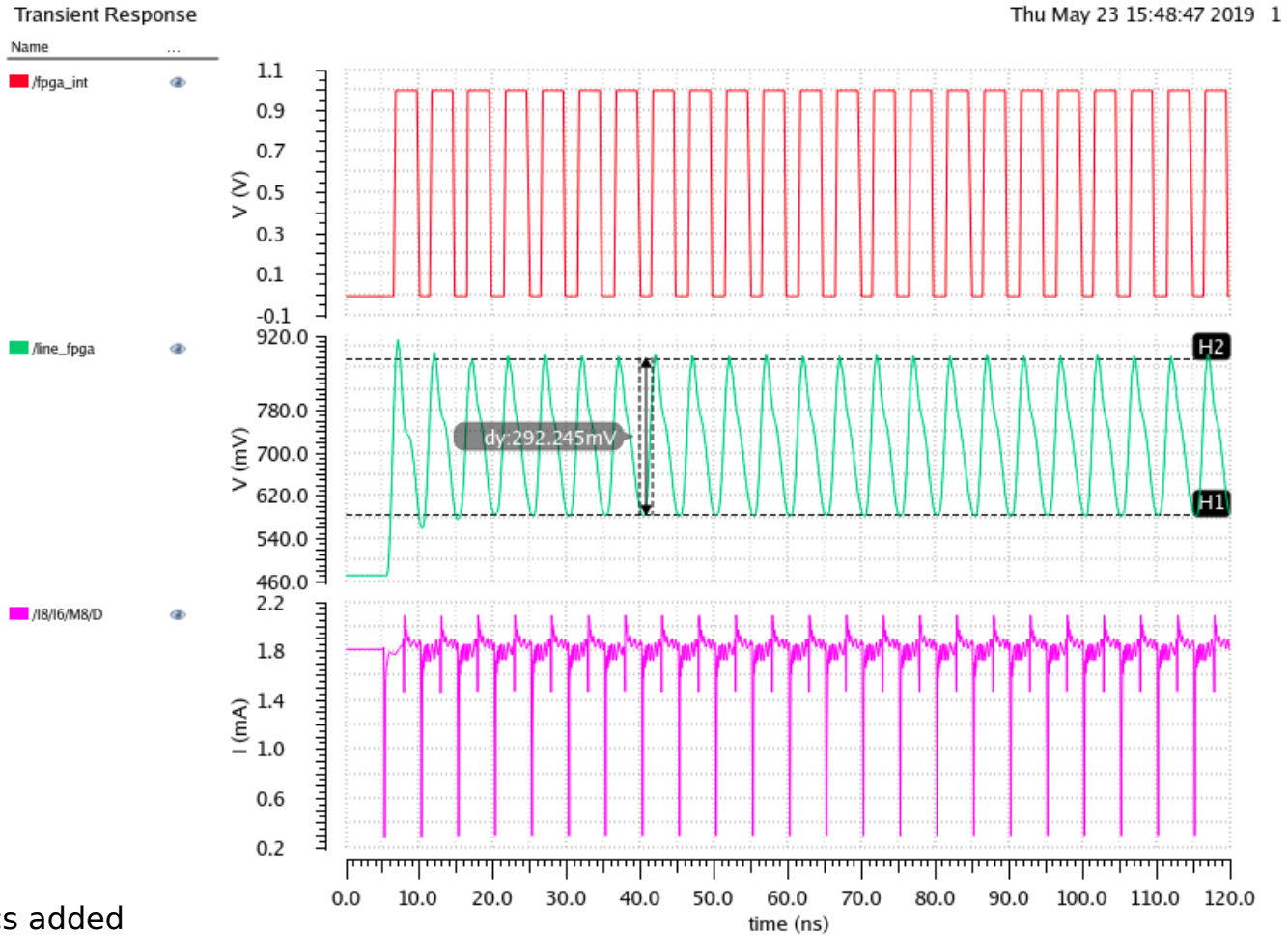
DCD output.

DCD current.



Future of the EDet.

DCD-FPGA interface.



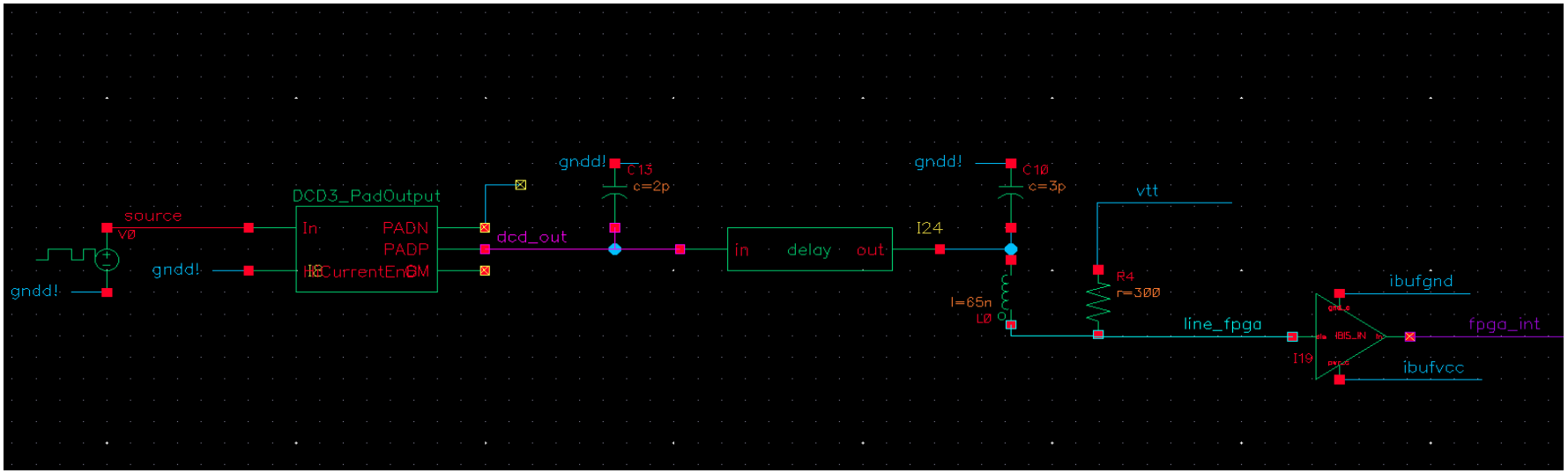
DCD output.

DCD current.

*Some parasitics added

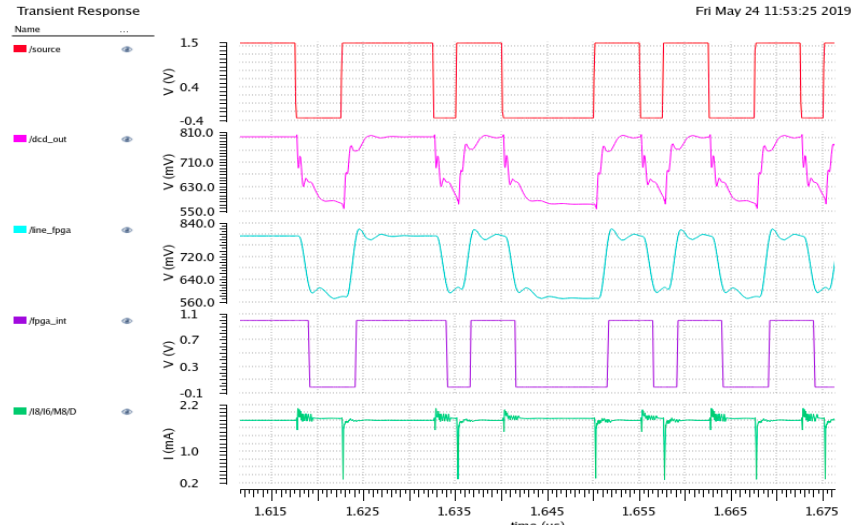
Future of the EDet.

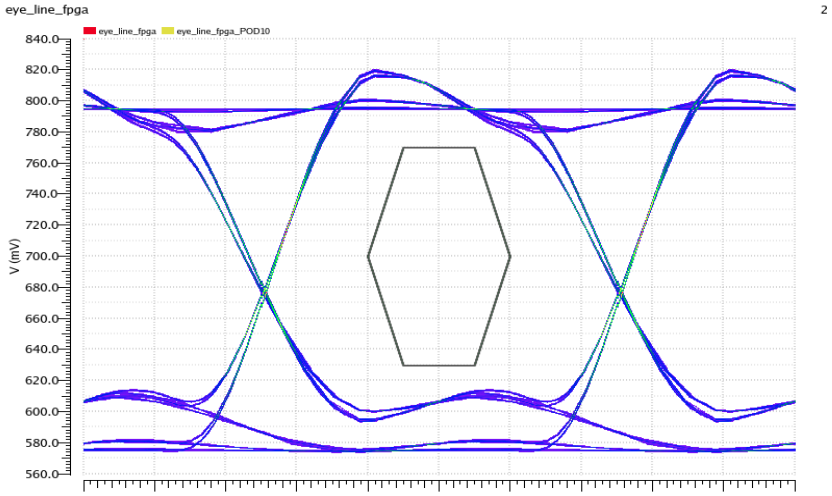
DCD-FPGA interface. Schematics.

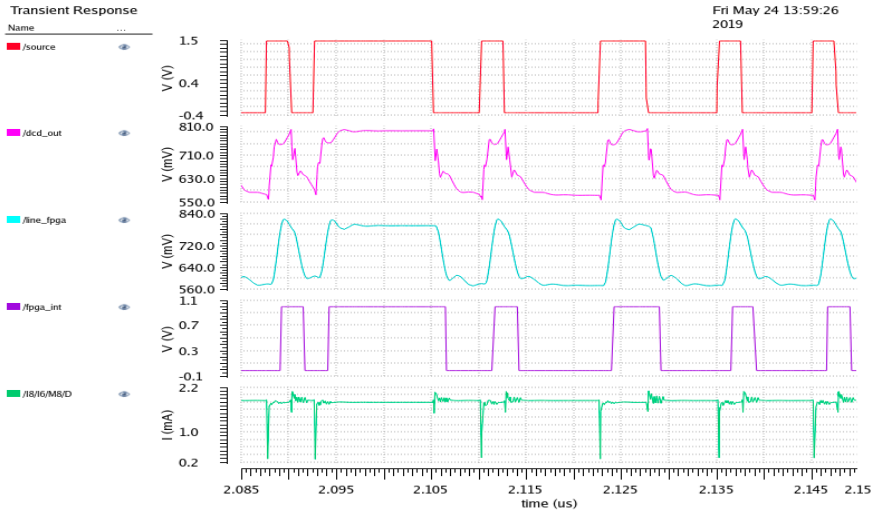


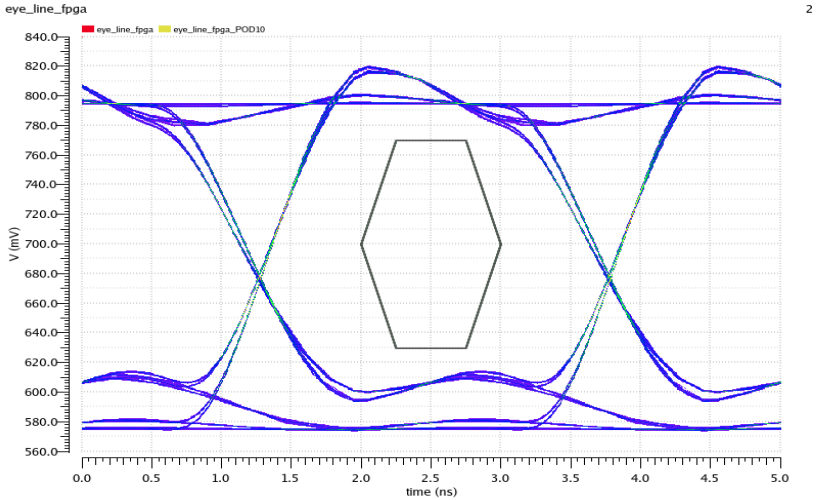
Future of the EDet.

DCD-FPGA interface. First reliability tests.









Future of the EDet.

What have we done already?

1. Found a way how to get bare-die Xilinx FPGA suitable for the project.
2. Interposer designer/manufacturer found.
3. Technology for datapath FPGA-network is found(Andrey‘s talk).
4. Initial DCD-FPGA simulation results received.

Future of the EDet.

What else could we do?

Improve digital side of DCD:

1. Utilize less IO
2. Release constraints to the line properties between DCD and FPGA
3. Simplify the design(one FGPA insted of two).

Test the weakest point(as it is seen from now) in hardware.

Future of the EDet.

Questions?

(I beleive you've got a lot)

Thanks for your attention.