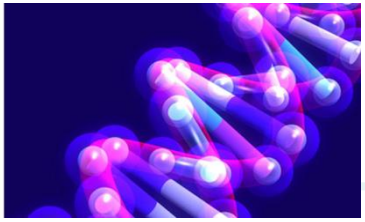
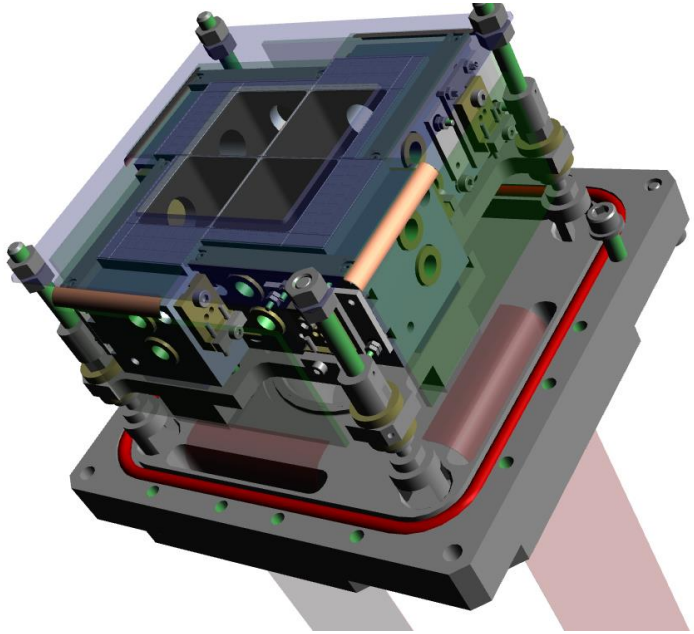



RESULTS FROM PROTOTYPE DCDE Transfer Curves

Belle vs Edet PS

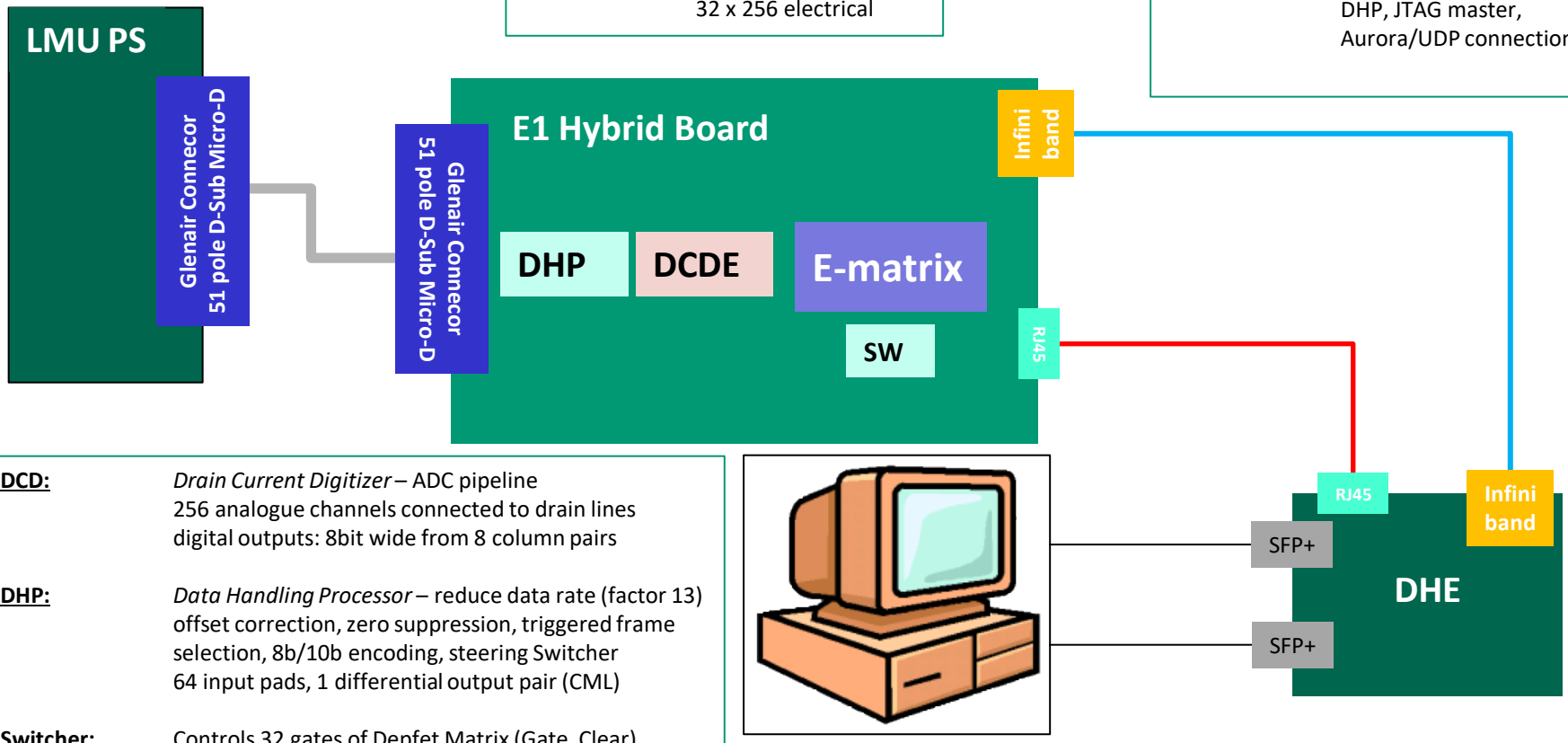


SMALL MATRIX TEST-SYSTEM – BELLE PS

Starting with the functional BELLE II chain all components are stepwise replaced and tested

Matrix Size: 12 x 7 mm
128 x 64 physical pixels
32 x 256 electrical

DHE: *Data Handling Engine*
data reader, framing, data buffering, steering DHP, JTAG master, Aurora/UDP connection

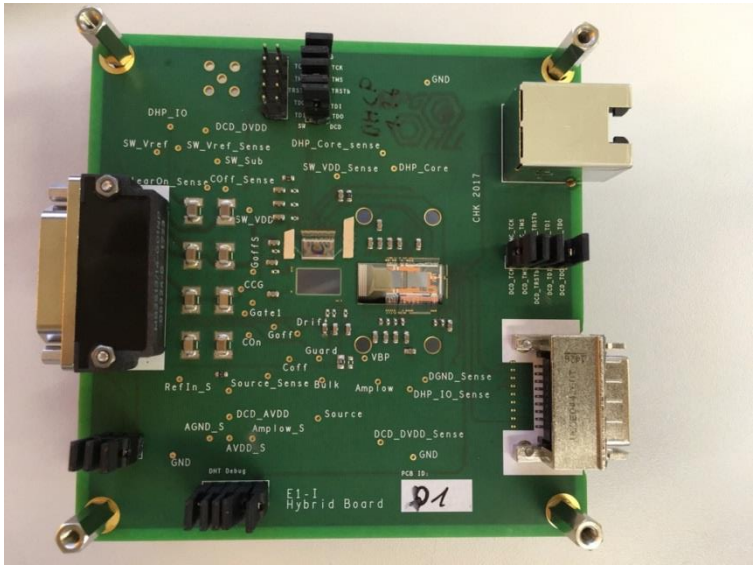


DCD: *Drain Current Digitizer* – ADC pipeline
256 analogue channels connected to drain lines
digital outputs: 8bit wide from 8 column pairs

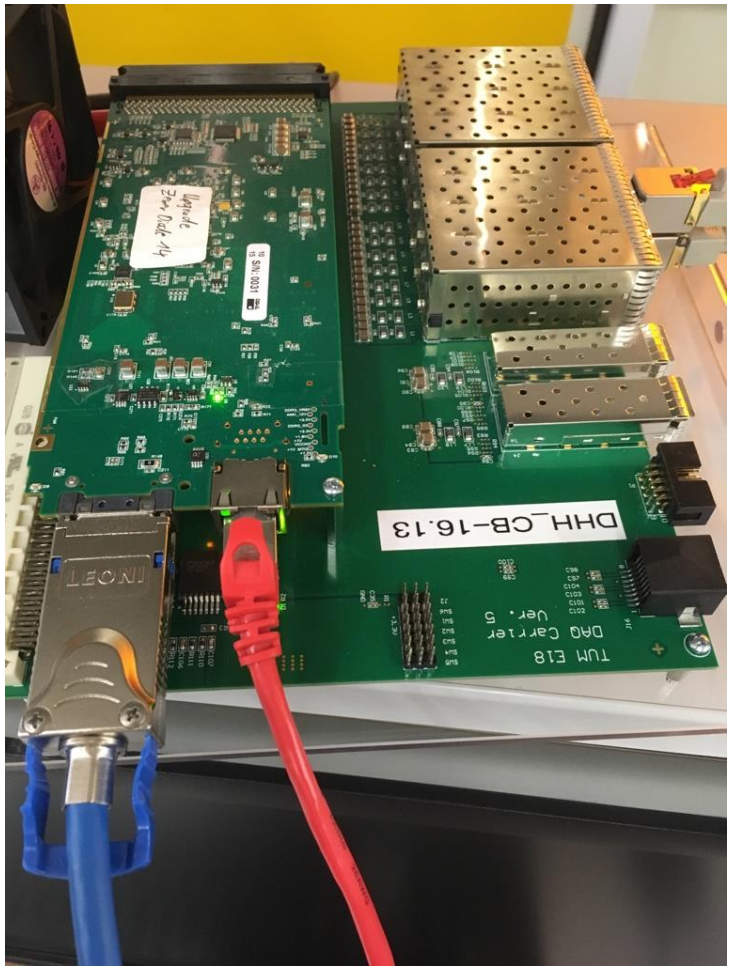
DHP: *Data Handling Processor* – reduce data rate (factor 13)
offset correction, zero suppression, triggered frame selection, 8b/10b encoding, steering Switcher
64 input pads, 1 differential output pair (CML)

Switcher: Controls 32 gates of Depfet Matrix (Gate, Clear)
high voltage CMOS technology supporting up to 20V

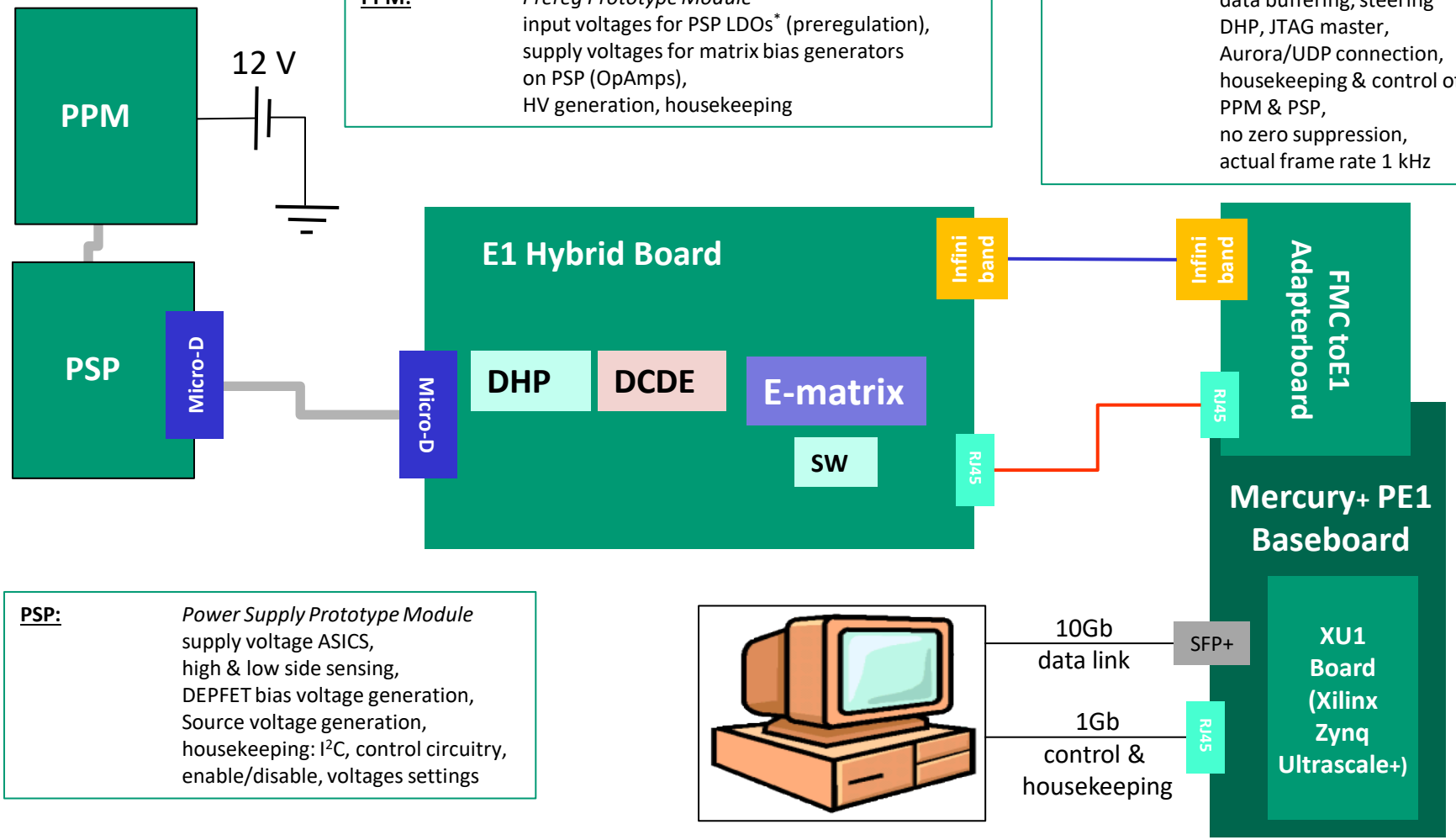
TEST SYSTEM – MAIN COMPONENTS



LMU PS: 9 different boards for each unit



SMALL MATRIX TEST-SYSTEM – EDET PS



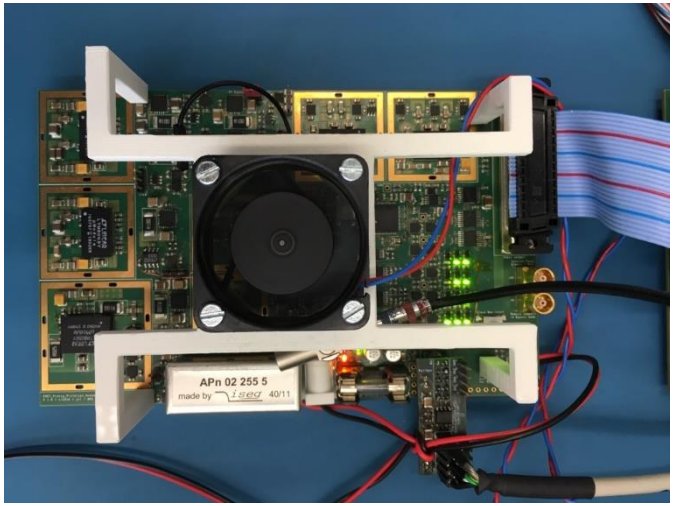
PPM: *Prereg Prototype Module*
input voltages for PSP LDOs* (preregulation),
supply voltages for matrix bias generators on PSP (OpAmps),
HV generation, housekeeping

XU1 FPGA: data reader, framing, data buffering, steering DHP, JTAG master, Aurora/UDP connection, housekeeping & control of PPM & PSP, no zero suppression, actual frame rate 1 kHz

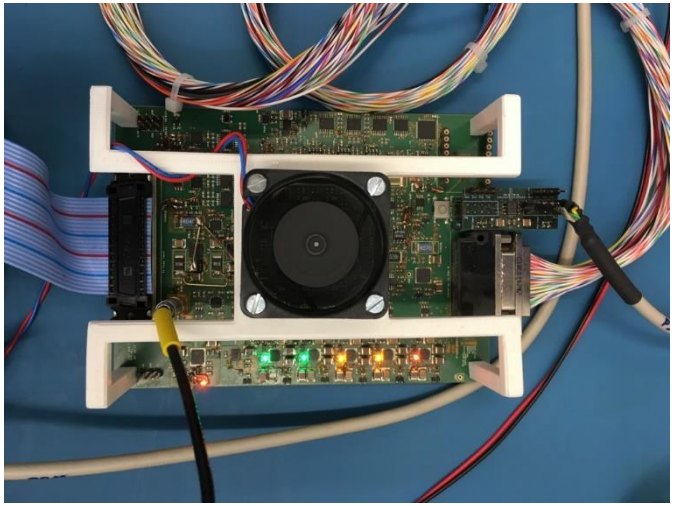
PSP: *Power Supply Prototype Module*
supply voltage ASICS,
high & low side sensing,
DEPFET bias voltage generation,
Source voltage generation,
housekeeping: I^2C, control circuitry,
enable/disable, voltages settings

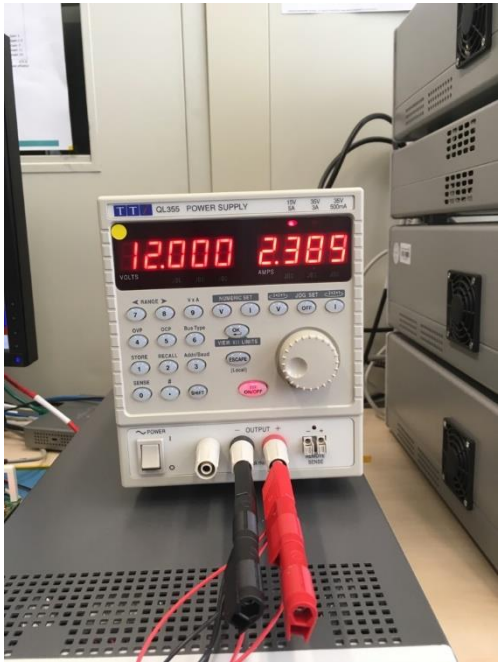
* Low Dropout Regulator

TEST SYSTEM – MAIN COMPONENTS



PPM (top) & PSP (bottom)

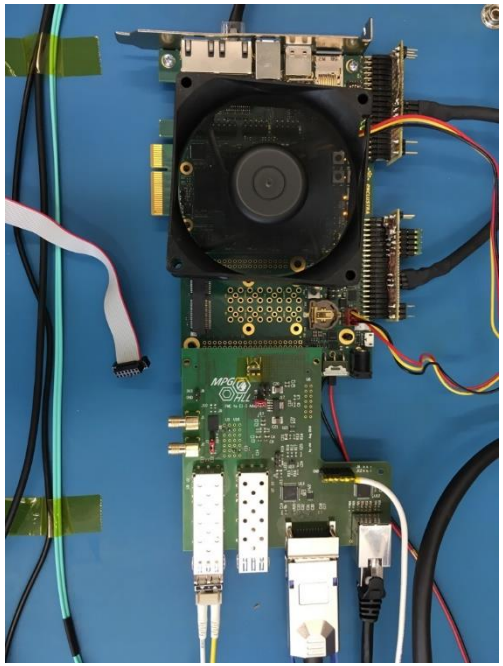




Mercury+ PE1 Base Board

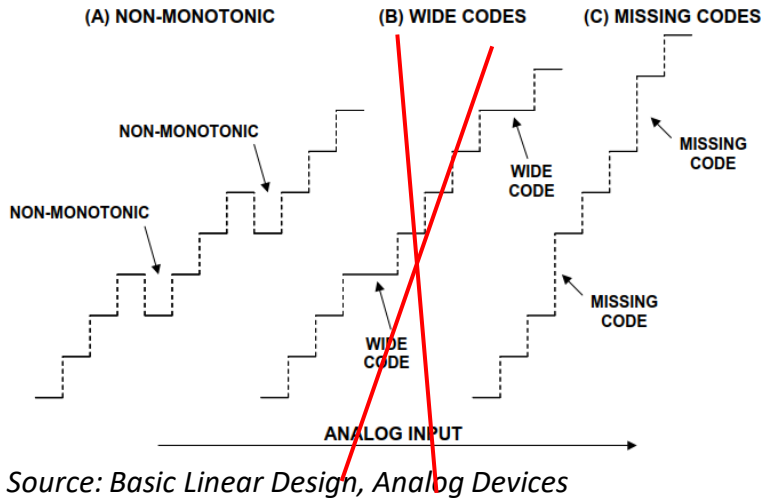
XU1 Board (Xilinx Zynq Ultrascale+ MPSoc Module FPGA)

FMC to E1 Adapterboard

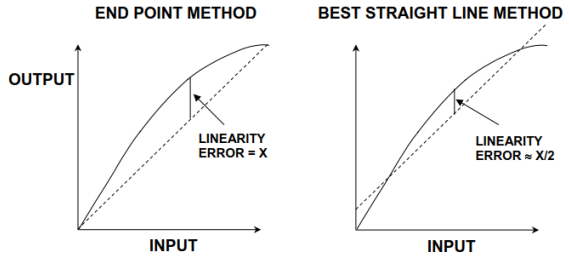


DCDE Testing Procedure

- Optimize settings within DCDE manual specifications
  - INLpp < 6 LSBs within +/- 100 ADU
  - DNL missing codes < 6 LSBs
  - Noise < 1 LSB



Source: Basic Linear Design, Analog Devices



INL of a code *c* is here defined as the deviation of the *mid-points of the quantization steps* between the 40-240ADU straight line (end point method) and the measured real transfer function

$$INL = |V_{ideal\ 40-240}(c) - V_{real}(c)|$$

$$DNL(i) = \frac{V_{out}(i) - V_{out}(i-1)}{ideal\ LSB\ step\ width} - 1$$

$$ideal\ LSB\ step\ width = \frac{V_{240} - V_{40}}{\#steps\ between}$$

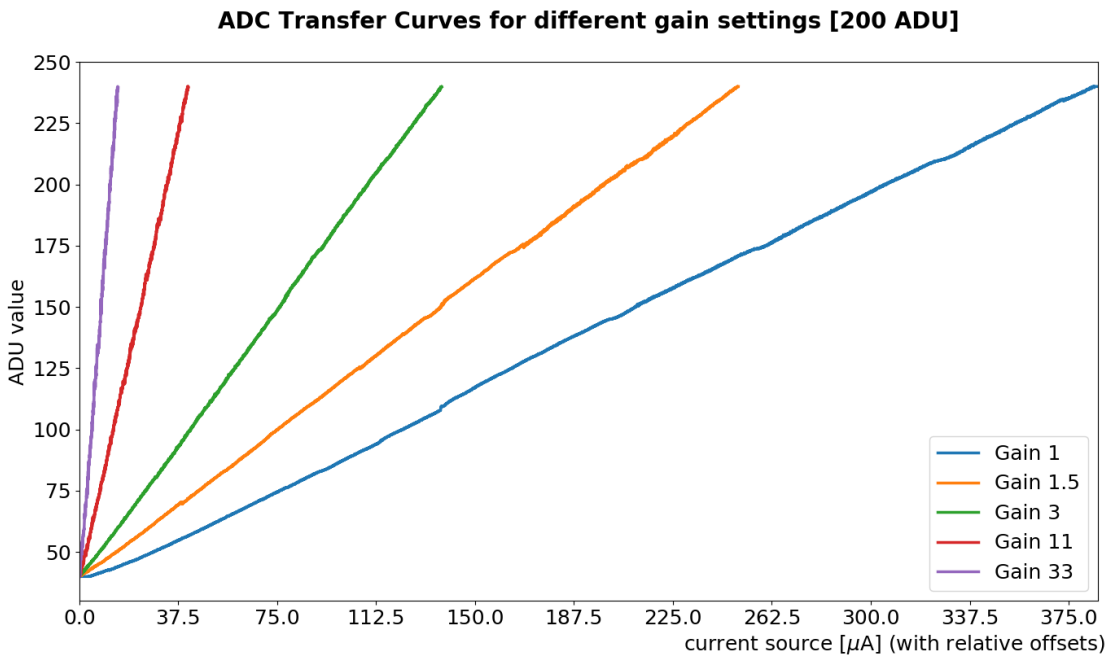
$-1 \leq DNL \leq 1$ … *ideal*

DNL < -1 … non-monotonic

DNL > 1 … missing code

TRANSFER CURVE DCDE GAIN IMPLEMENTATION

En30	En60	En90	En120	Gain	Times lowest Gain
1	1	1	1	0.061	1.0
0	1	1	1	0.063	1.0
1	1	1	0	0.065	1.1
0	1	1	0	0.067	1.1
1	0	1	1	0.087	1.4
0	0	1	1	0.091	1.5
1	0	1	0	0.095	1.6
0	0	1	0	0.100	1.7
1	1	0	1	0.154	2.5
0	1	0	1	0.167	2.8
1	1	0	0	0.182	3.0
0	1	0	0	0.200	3.3
1	0	0	1	0.667	11.0
0	0	0	1	1.000	16.5
1	0	0	0	2	33



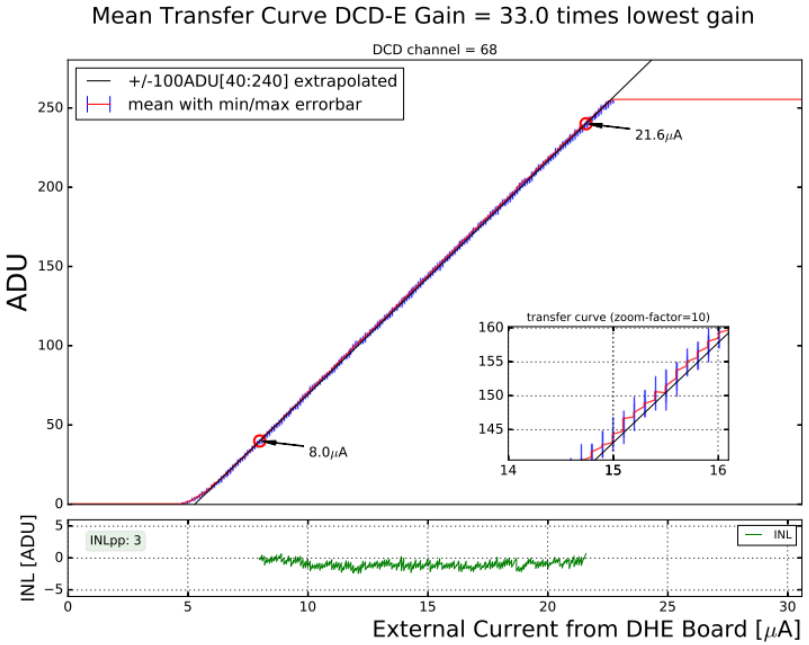
R_s: En30 = 30k
En60 = 3k
En90 = 1.5k
En120 = 15k

R_f = 15k

$$Gain = \frac{R_s}{R_f}$$

ADC-TRANSFER CURVE for different GAINS

E1_I_05 Hybrid Board

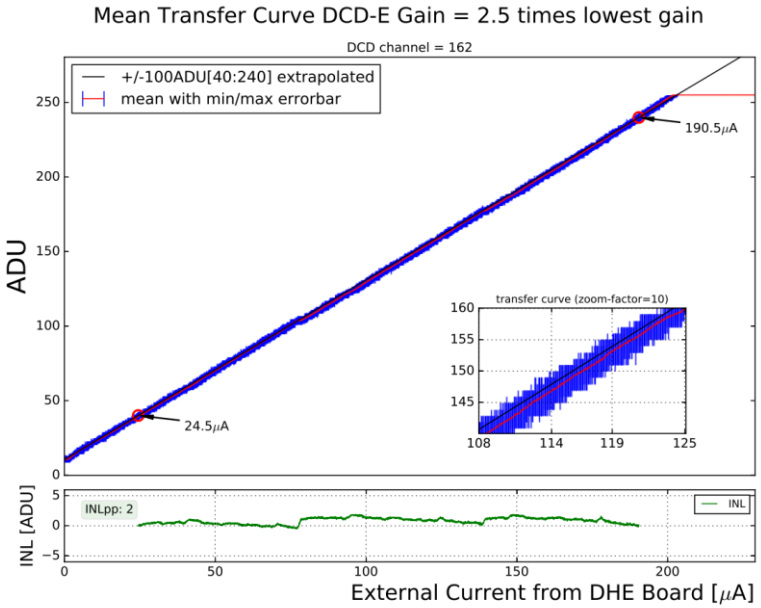


Gain	200ADU
33.0	13.6μA
2.5	166μA

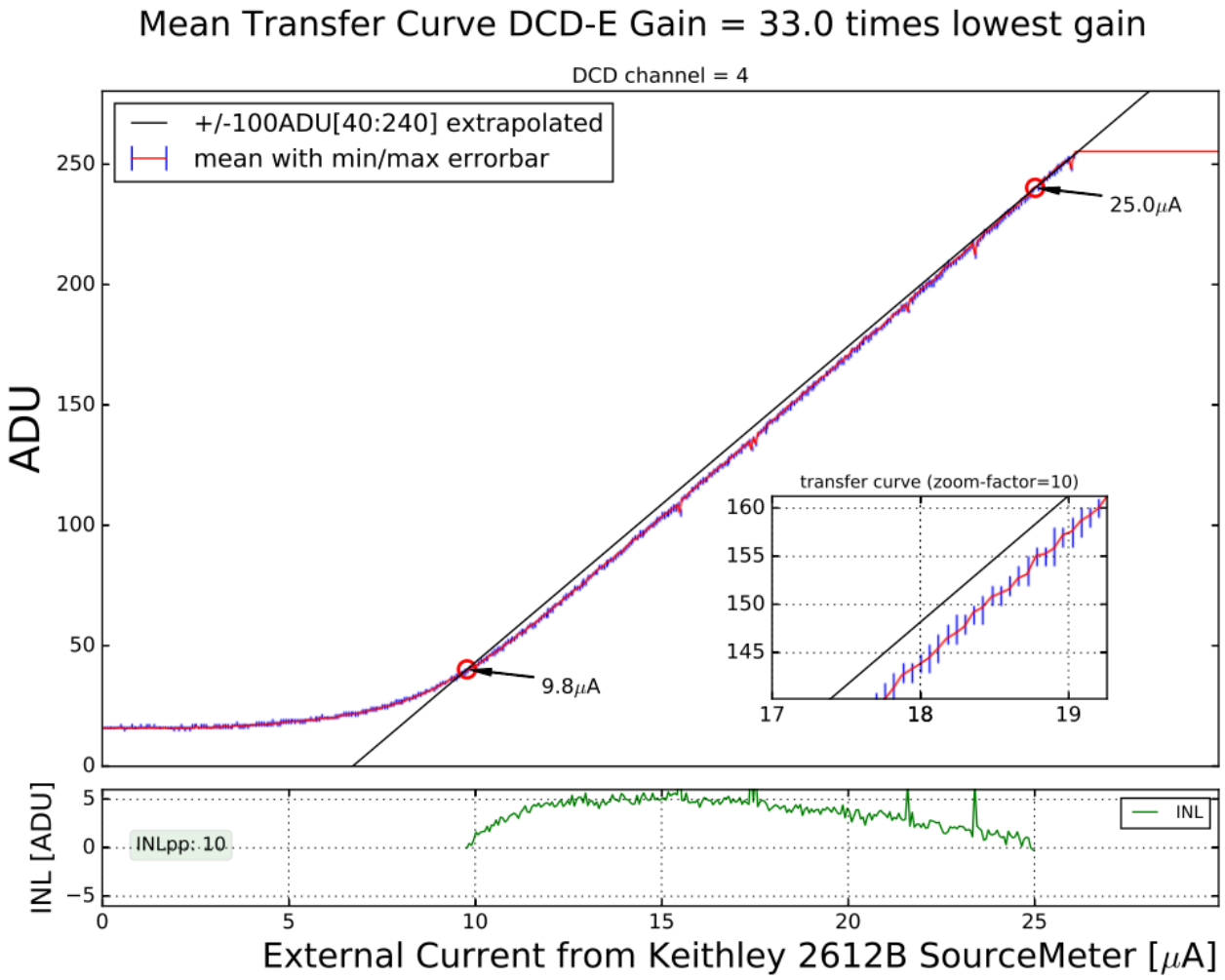
DHE current source 248μA, 65k DAC steps

→ strengthen switch for higher currents

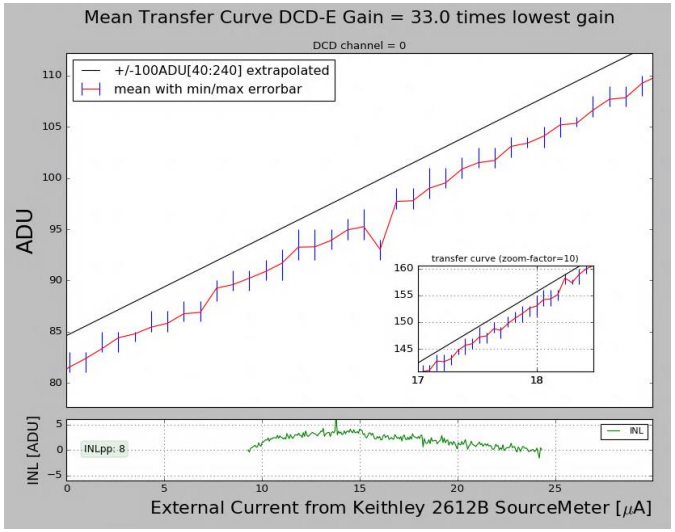
(VNSubIN 1DAC≈6μA)

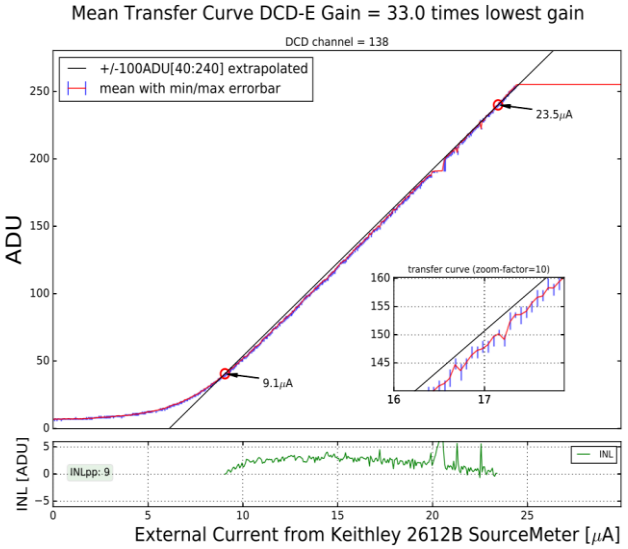


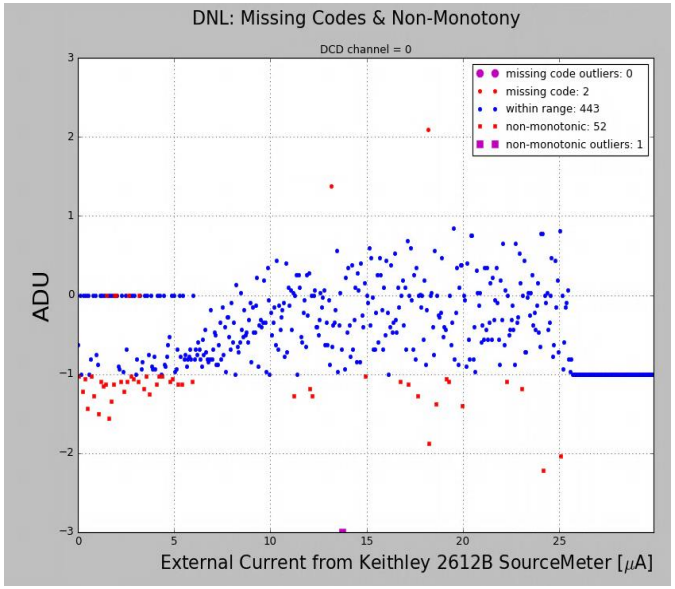
INL EDET PS E1_I_05 Board

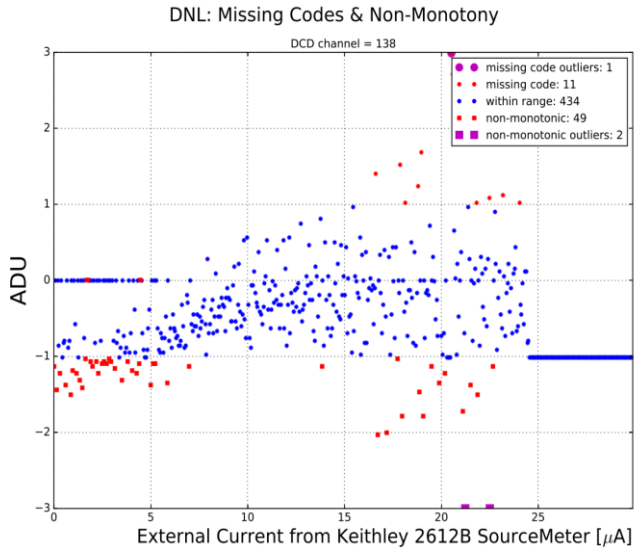


DNL: Non-Monotonicity, Missing Code

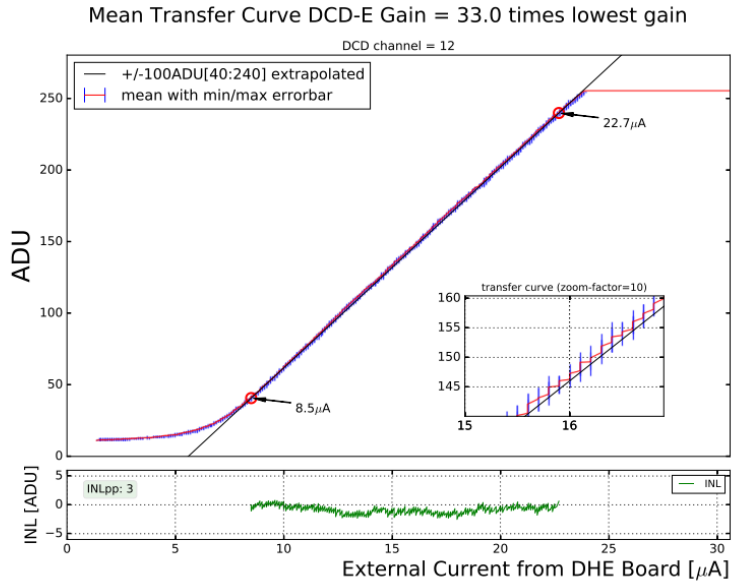




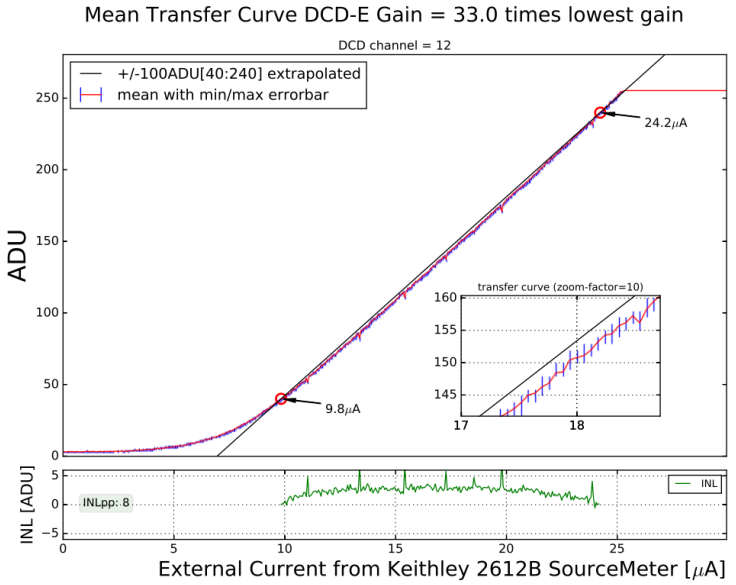




High Gain: BELLE vs EDET PS Channel 12 (1)

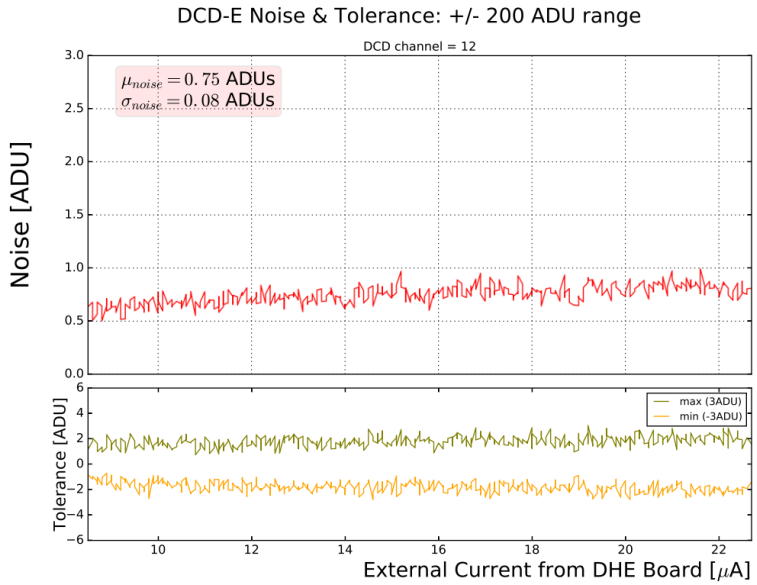


EDET: 600 vs 850 data points,
worse INL,
larger dynamic range
(14.4 vs 14.2 µA)

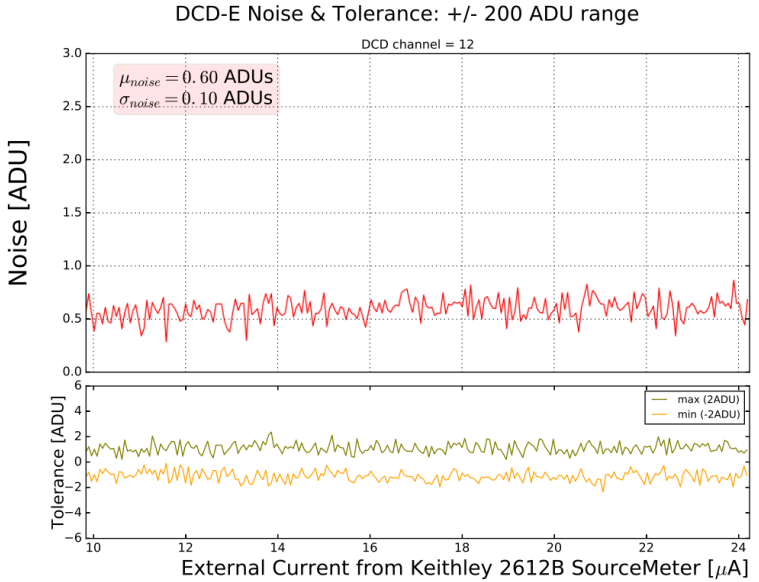


High Gain: BELLE vs EDET PS Channel 12 (2)

Noise

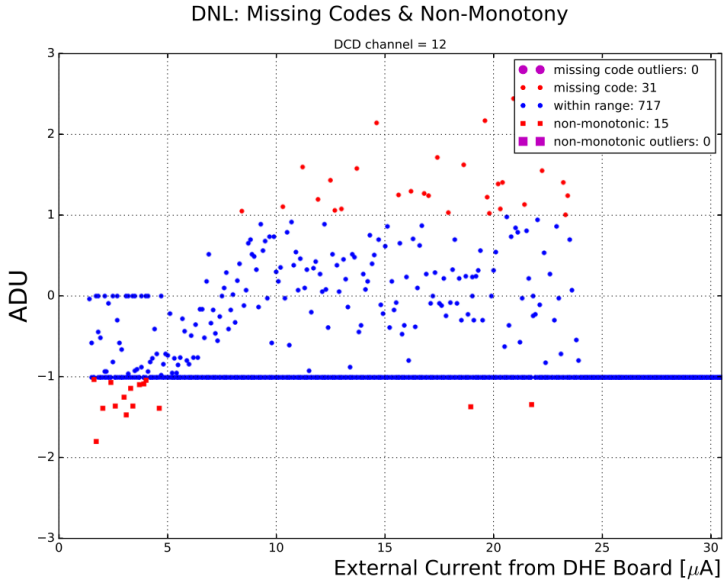


EDET: slightly lower noise
slightly lower tolerance

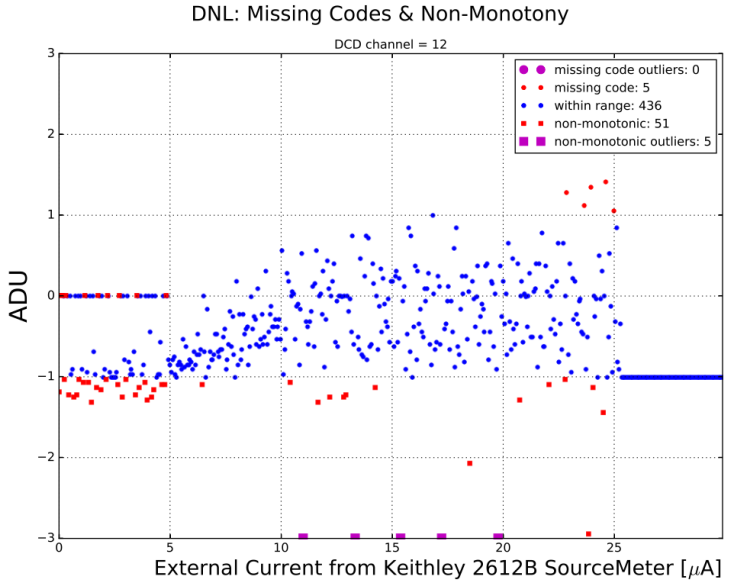


High Gain: BELLE vs EDET PS Channel 12 (3)

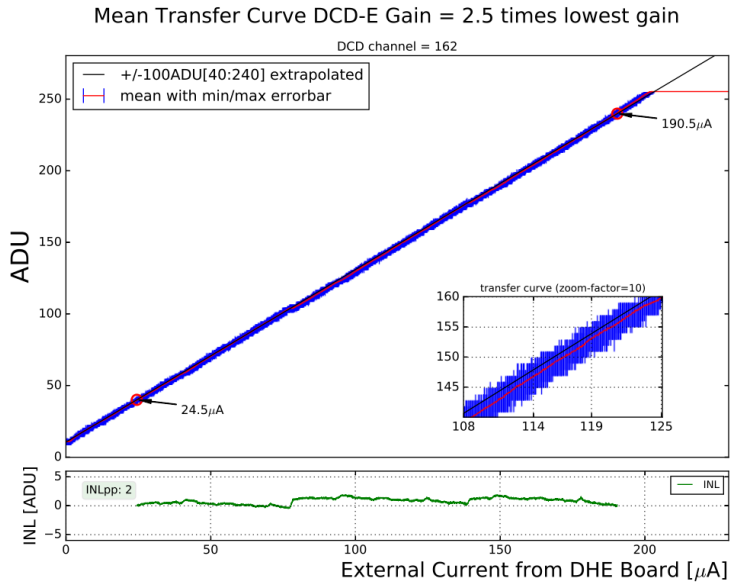
DNL: Missing Codes & Non-Monotonicity



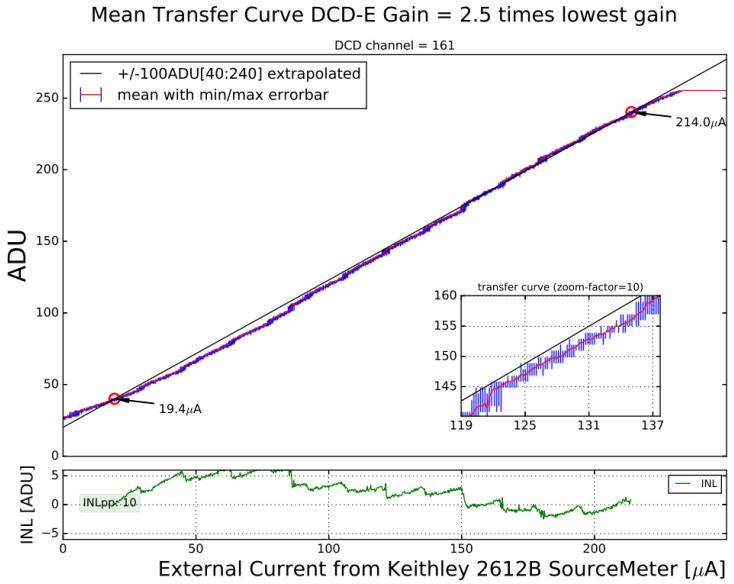
EDET: non-monotonic (software?)



2.5 Gain: BELLE vs EDET PS Channel 162 (1)

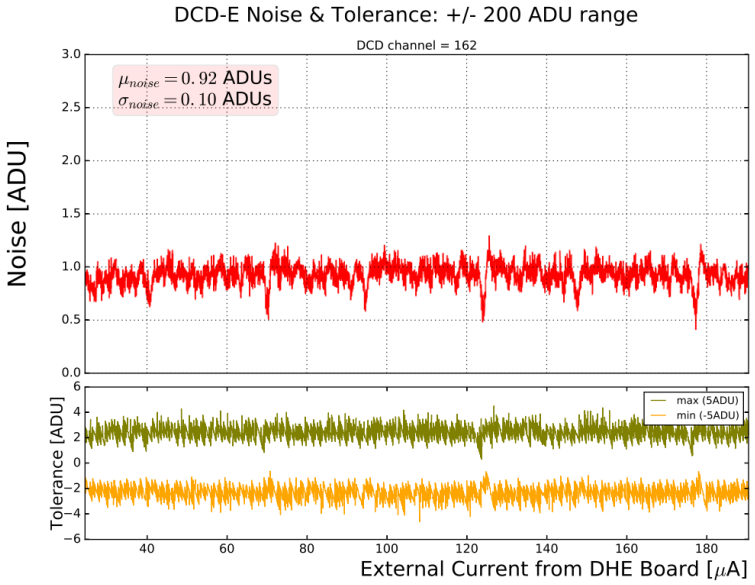


EDET: 8500 vs 1200 data points,
jagged ADC curve,
worse INL,
larger dynamic range
(194.6 vs 166 µA)

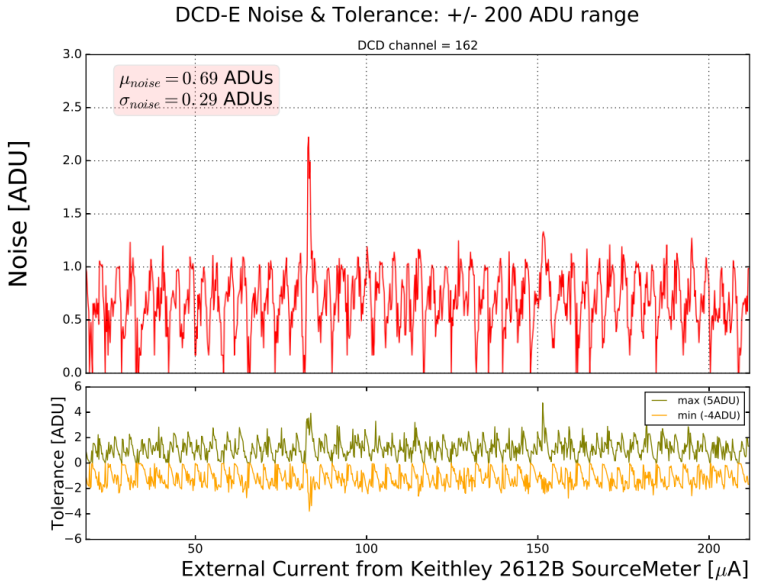


2.5 Gain: BELLE vs EDET PS Channel 162 (2)

Noise

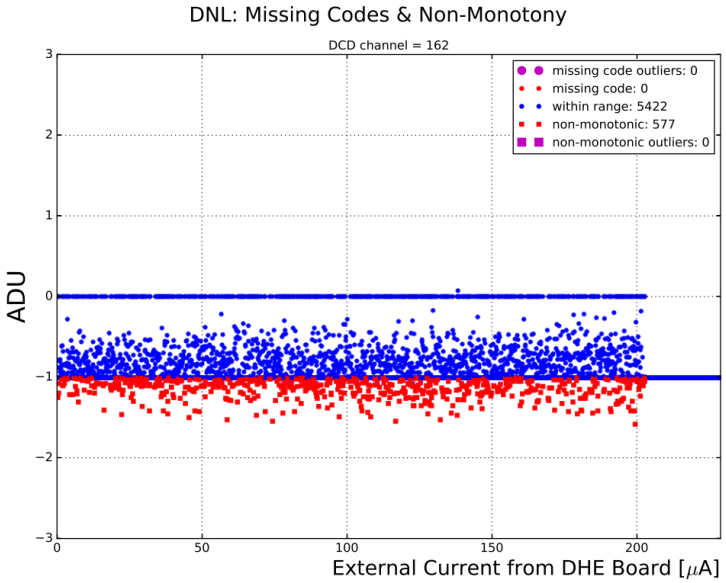


EDET: lower noise

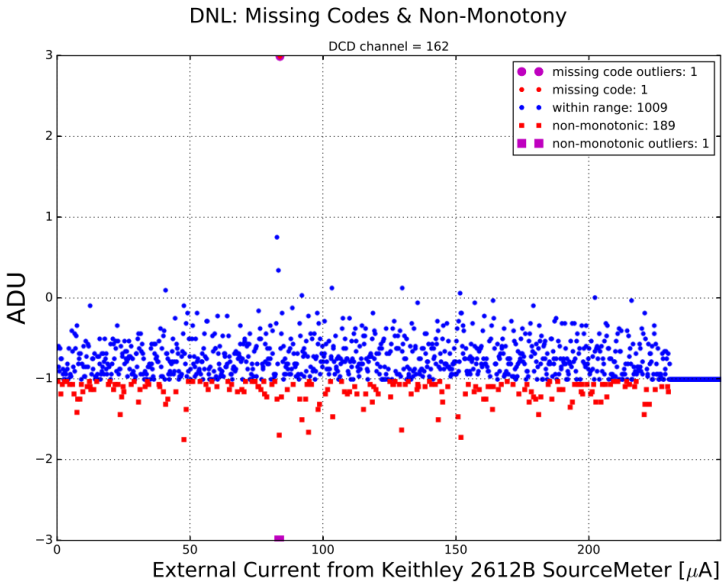


2.5 Gain: BELLE vs EDET PS Channel 162 (3)

DNL: Missing Codes & Non-Monotonicity

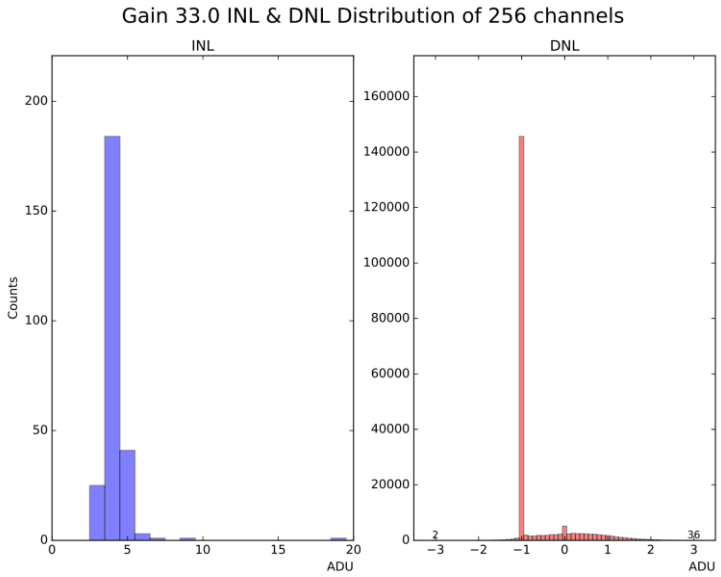


EDET: both similar



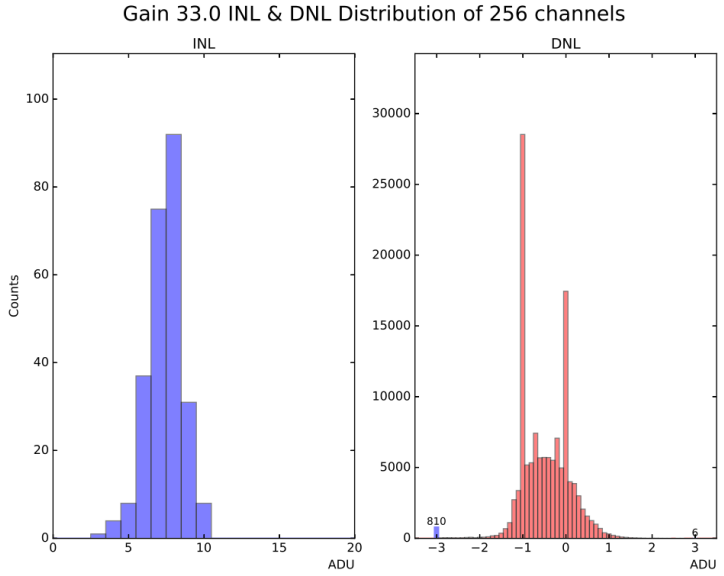
33 Gain: BELLE vs EDET PS

INL & DNL Distributions



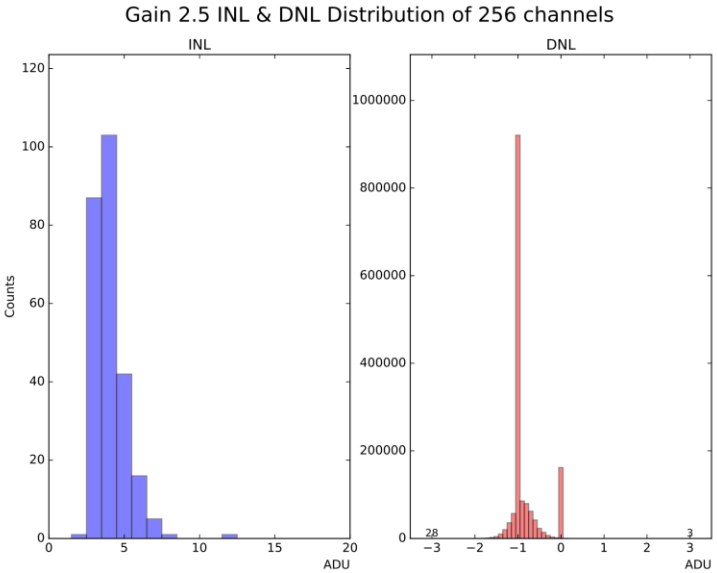
BELLE

EDET



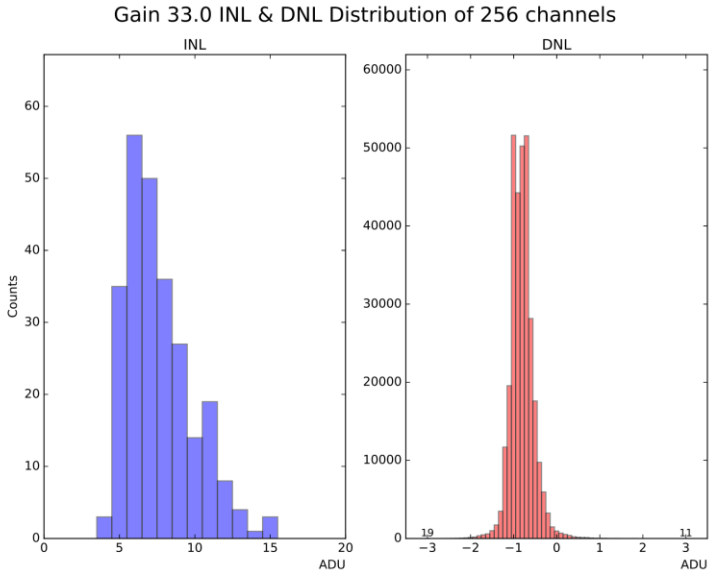
2.5 Gain: BELLE vs EDET PS

INL & DNL Distributions



BELLE

EDET



CONCLUSION

- KEY SYSTEM DIFFERENCES:
  - external current source
  - different FPGA and firmware
  - different PS
  - (slightly different DCDE settings?)
- KEY OBSERVATIONS:
  - EDET PS system seems to deliver higher INL violating DCDE limits from specs
  - both BELLE and EDET PS: most transfer curve not perfectly smooth
  - some channels markedly “jagged” transfer curves for EDET PS
  - noise for both PS no problem

All channels on: hll.mpg.de/~exp711

THANK YOU FOR YOUR ATTENTION