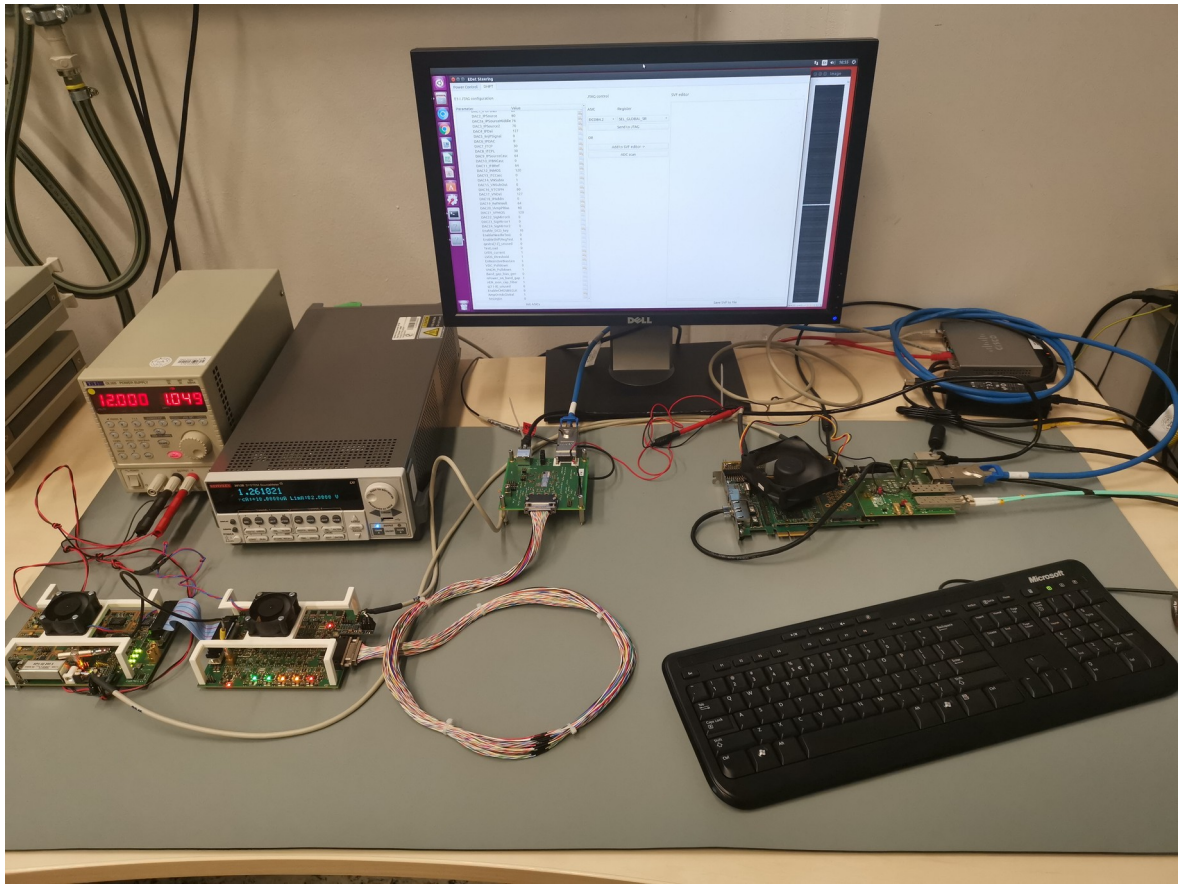
Firmware status update.

* XG link SI issue root cause disclosure,
* DHPT link stability improved,
* Advanced configuration,
* Further steps

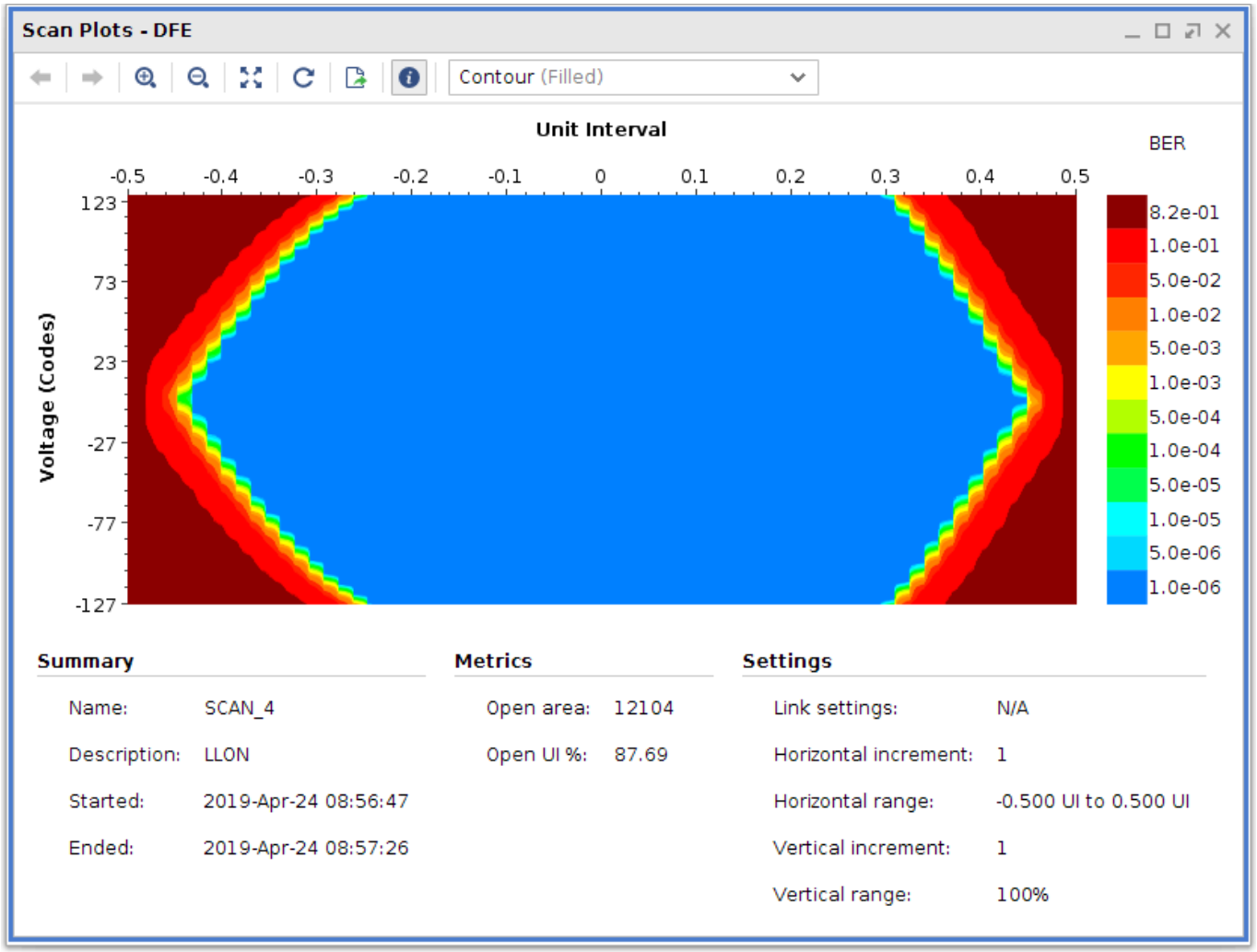
DHPT image streaming.



Migration to MSM.

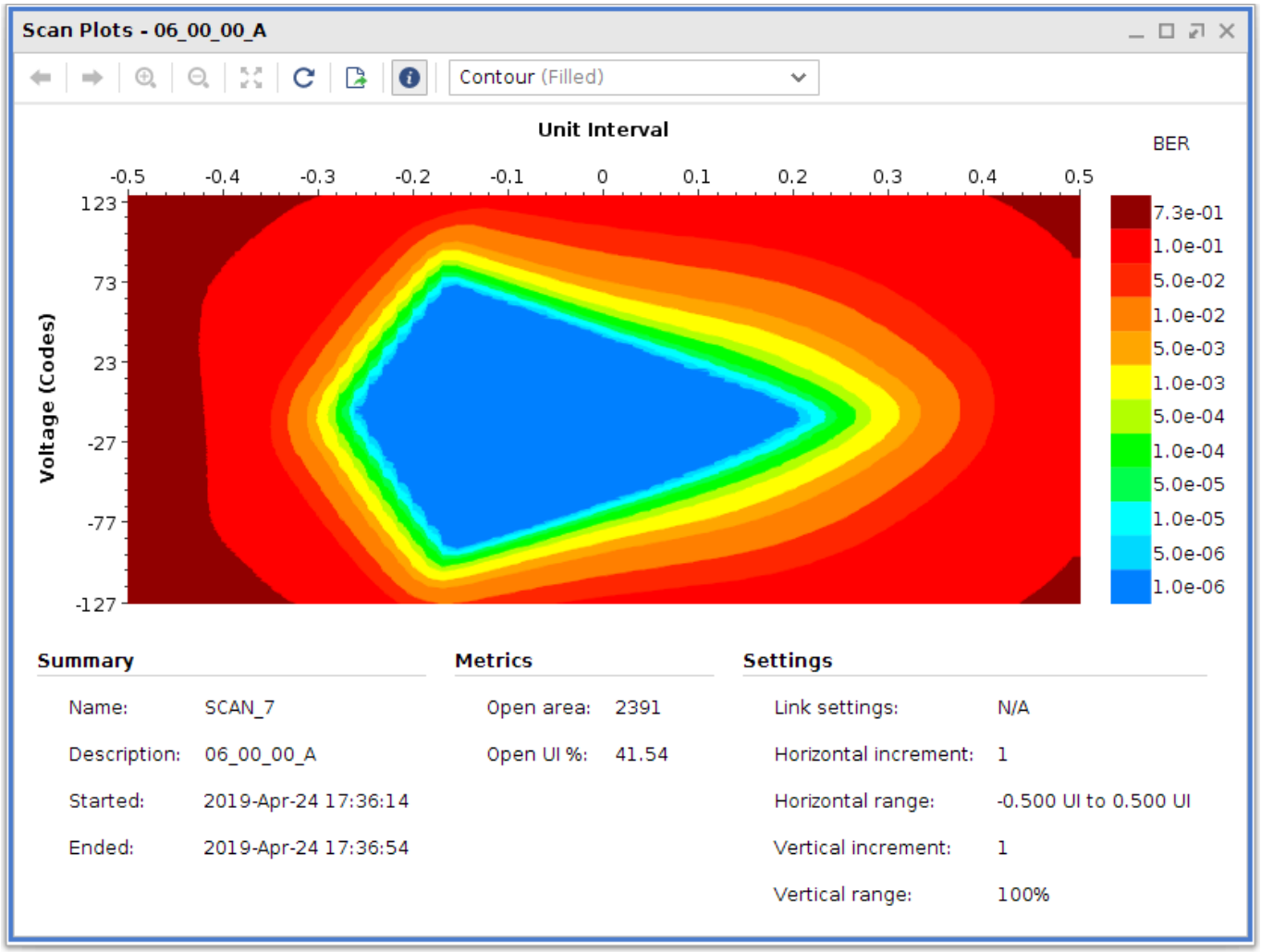
Cold boot from the network.

Migration to MSM. SI.



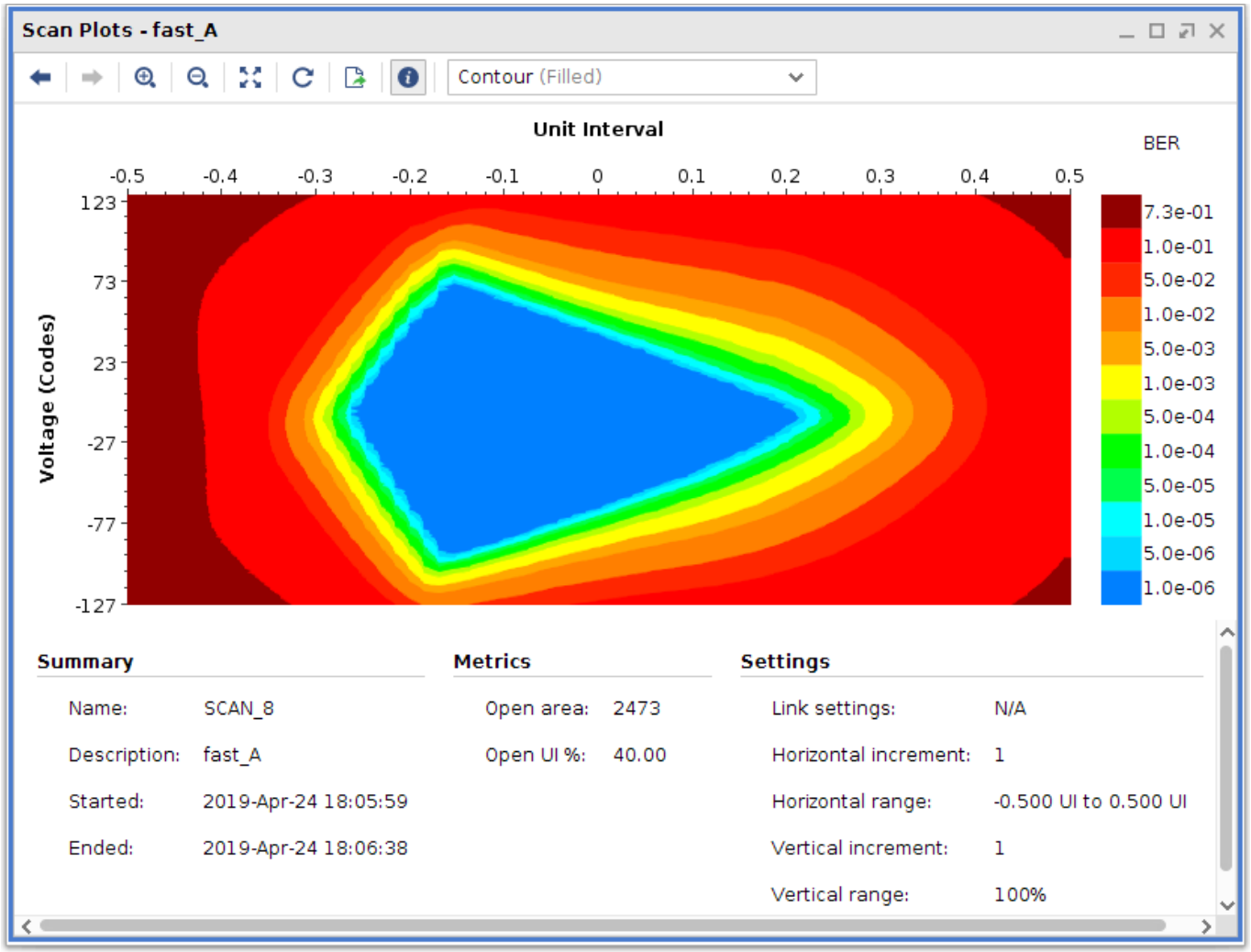
FPGA loopback.

Migration to MSM. SI.



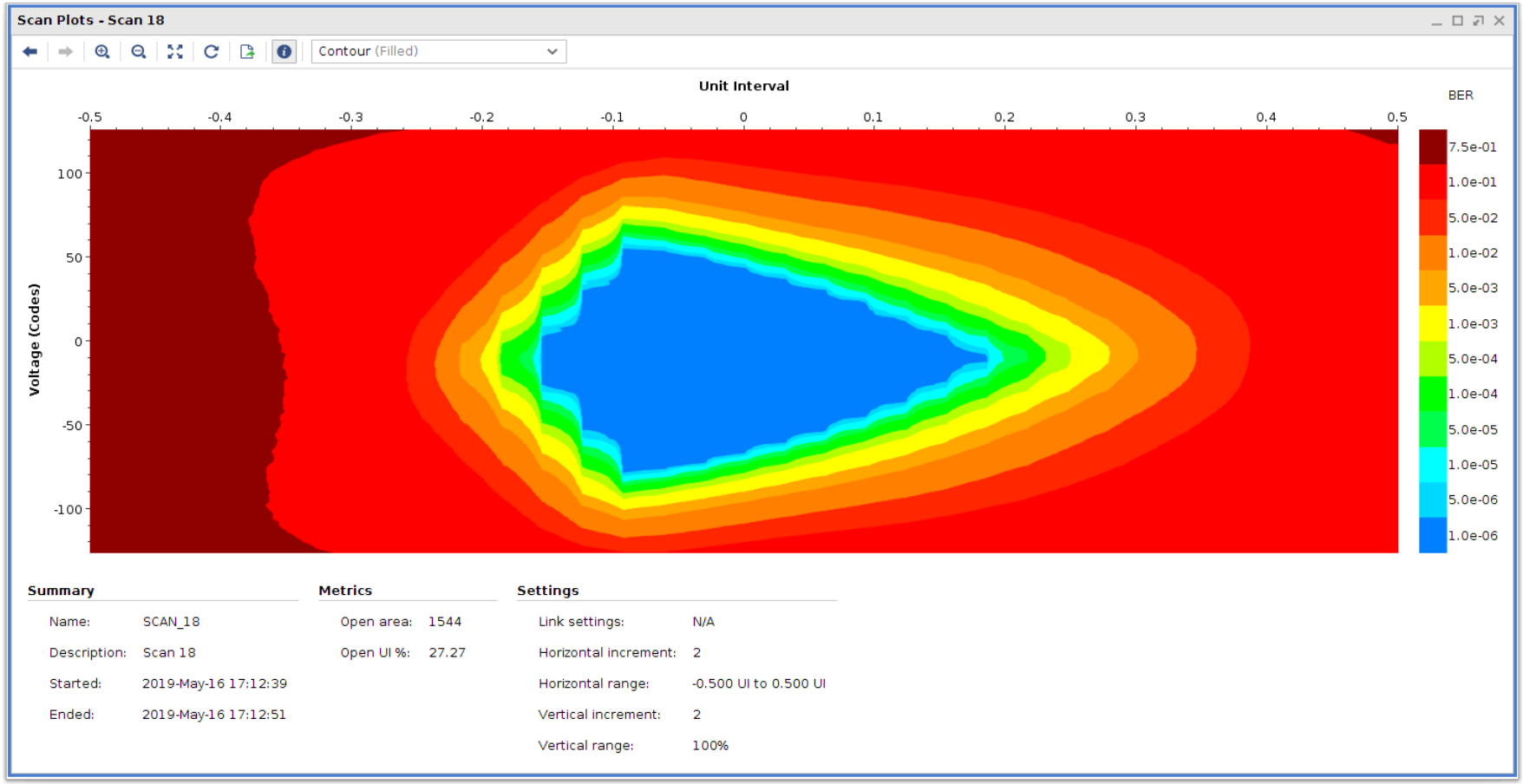
Local optical loopback. Optimal parameters #1. Simple EQ.

Migration to MSM. SI.



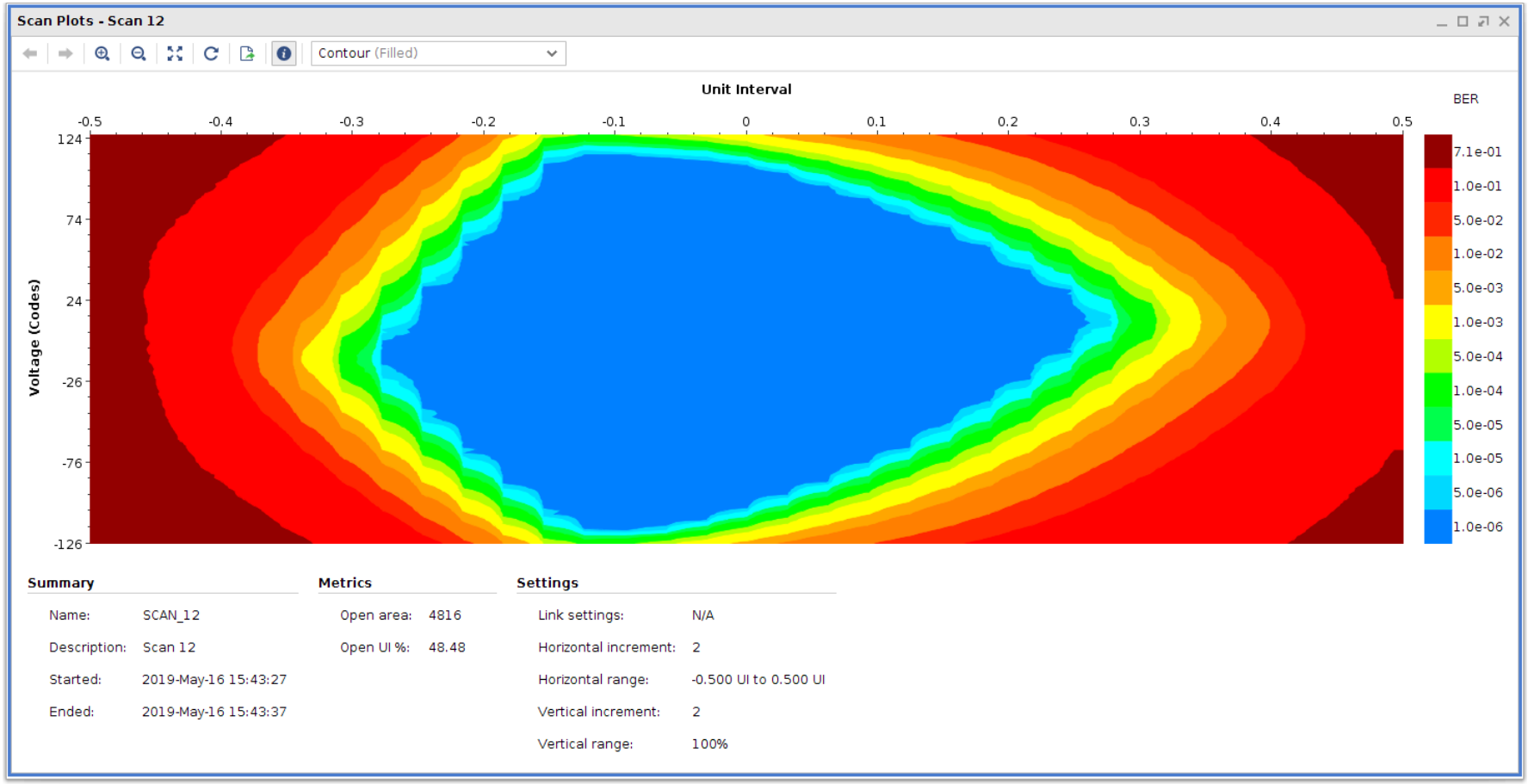
NIC fiber connection. Optimal parameters #2. Simple EQ.

Migration to MSM. SI.



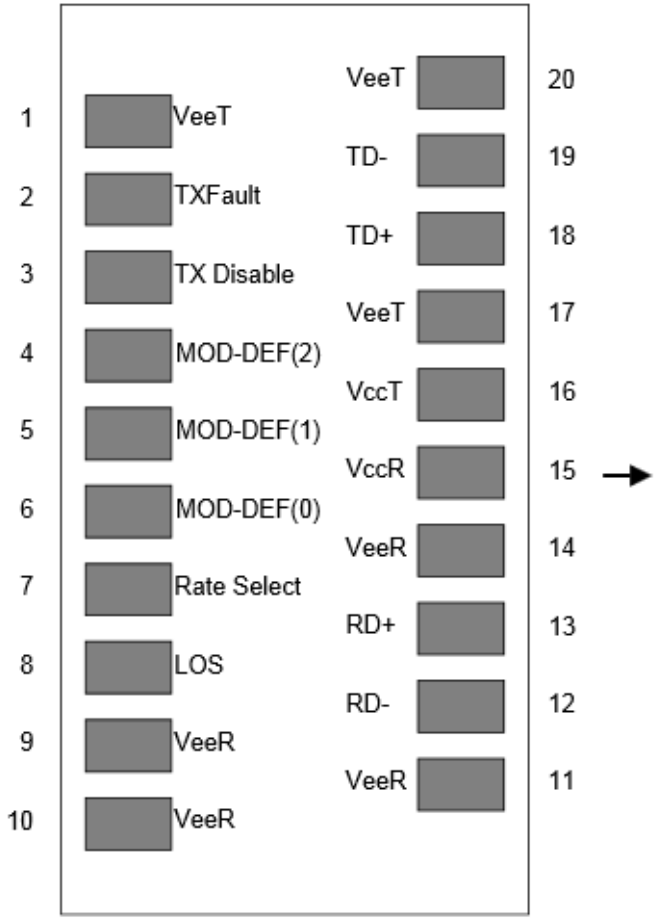
Cross check with PE1+Adapter as signal source. Simple EQ.
Rx line eye diagram on MSM#01.

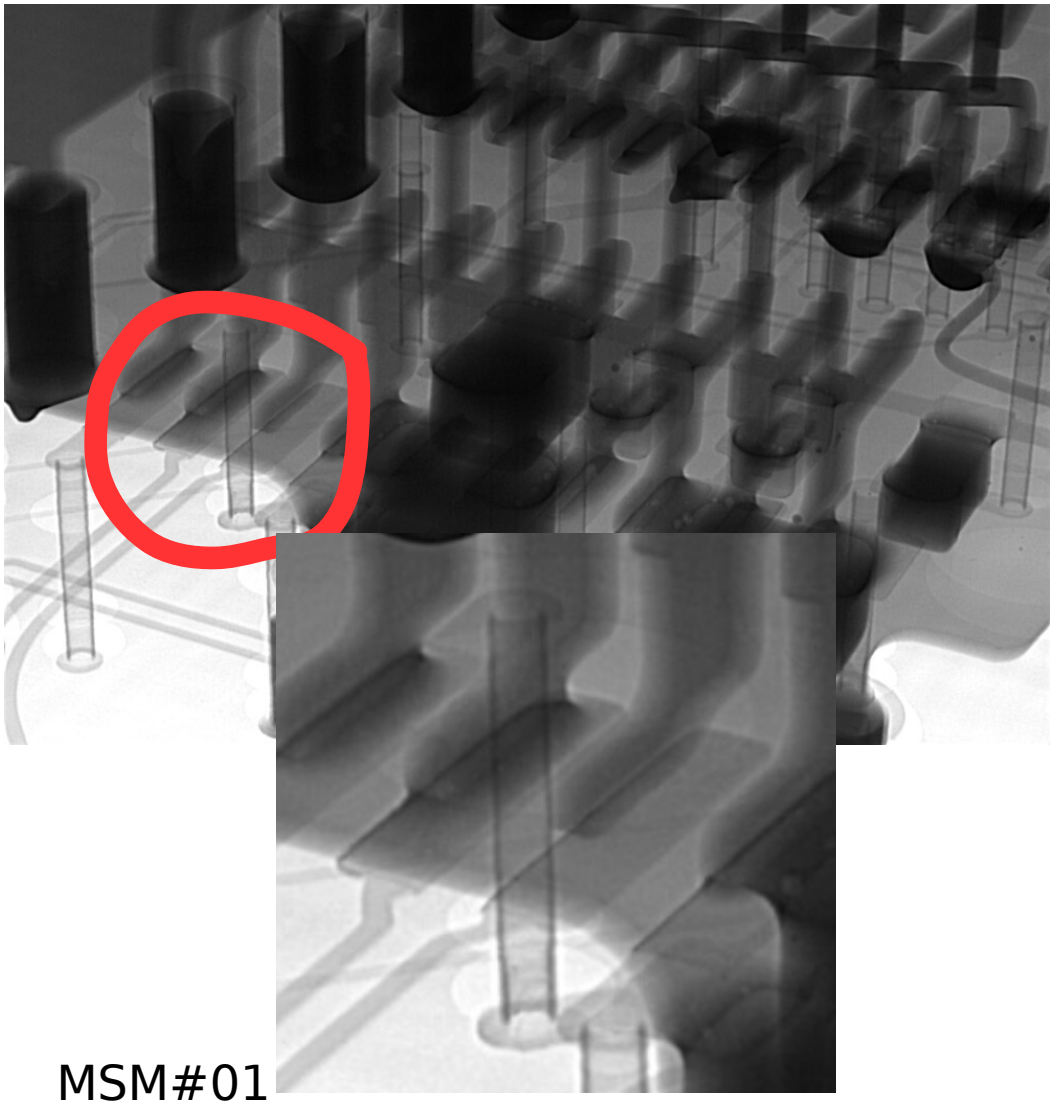
Migration to MSM. SI.



Cross check with PE1+Adapter as signal source. Simple EQ.
Rx line eye diagram on MSM#02.

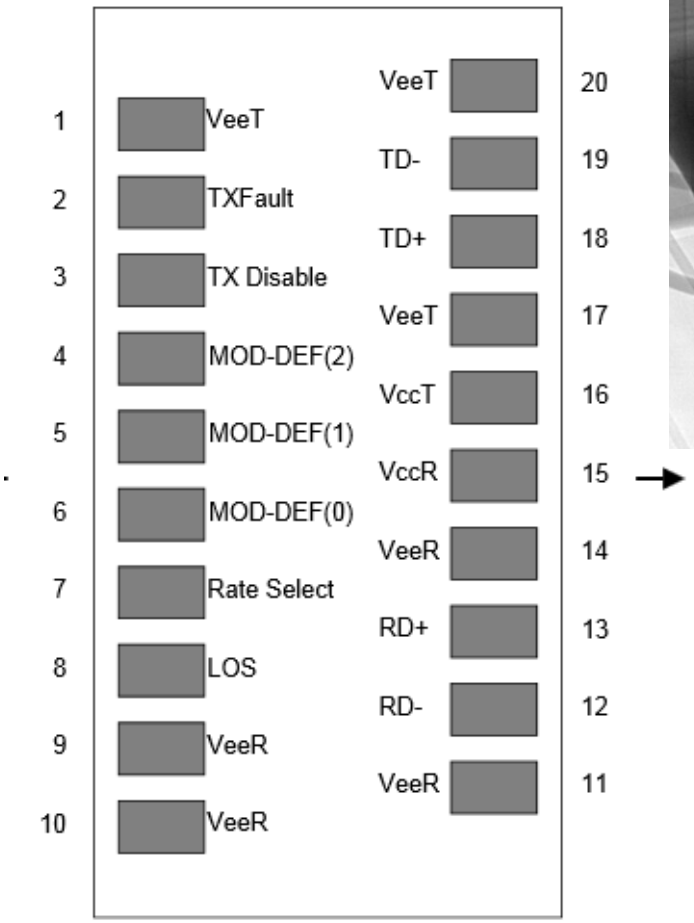
MSM 10G Rx line fault disclousure

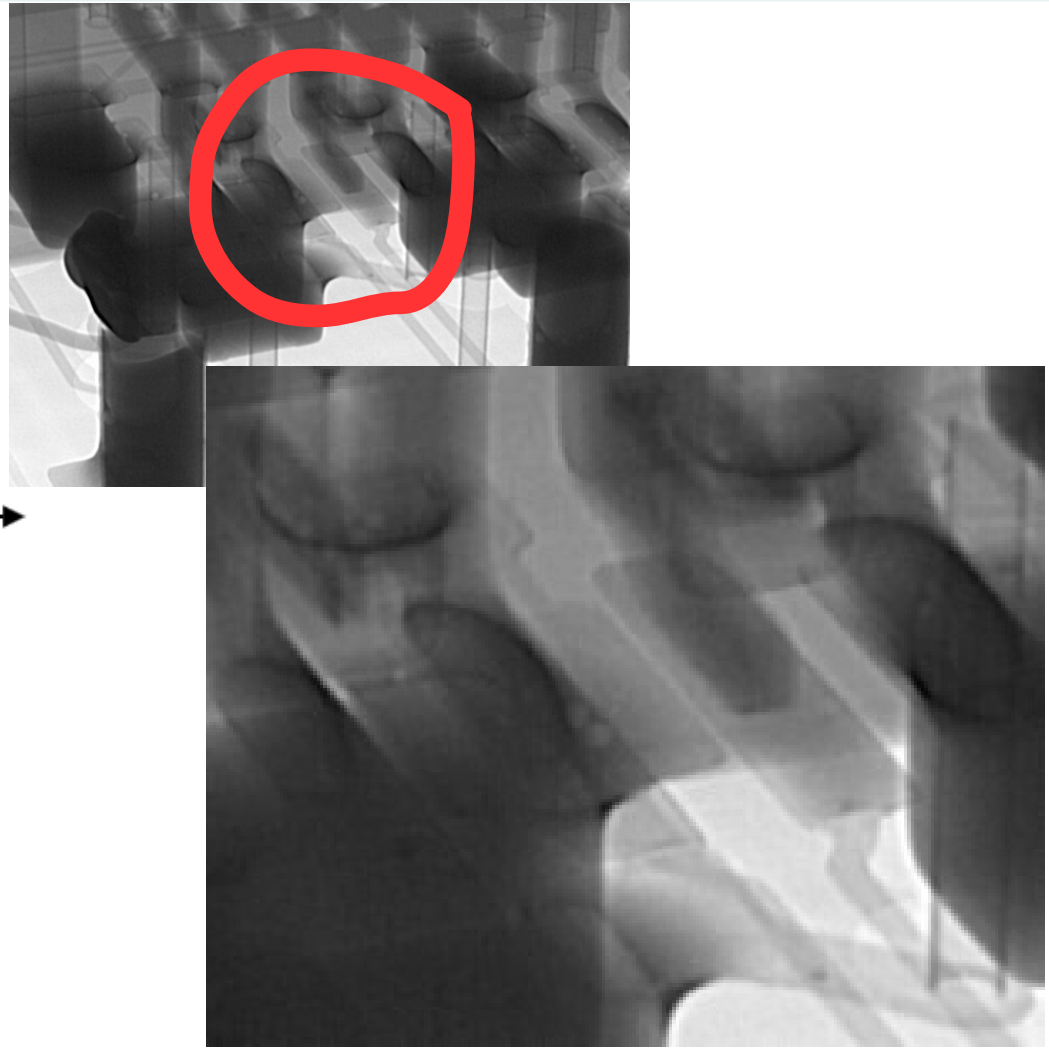




MSM#01

MSM 10G Rx line fault disclousure

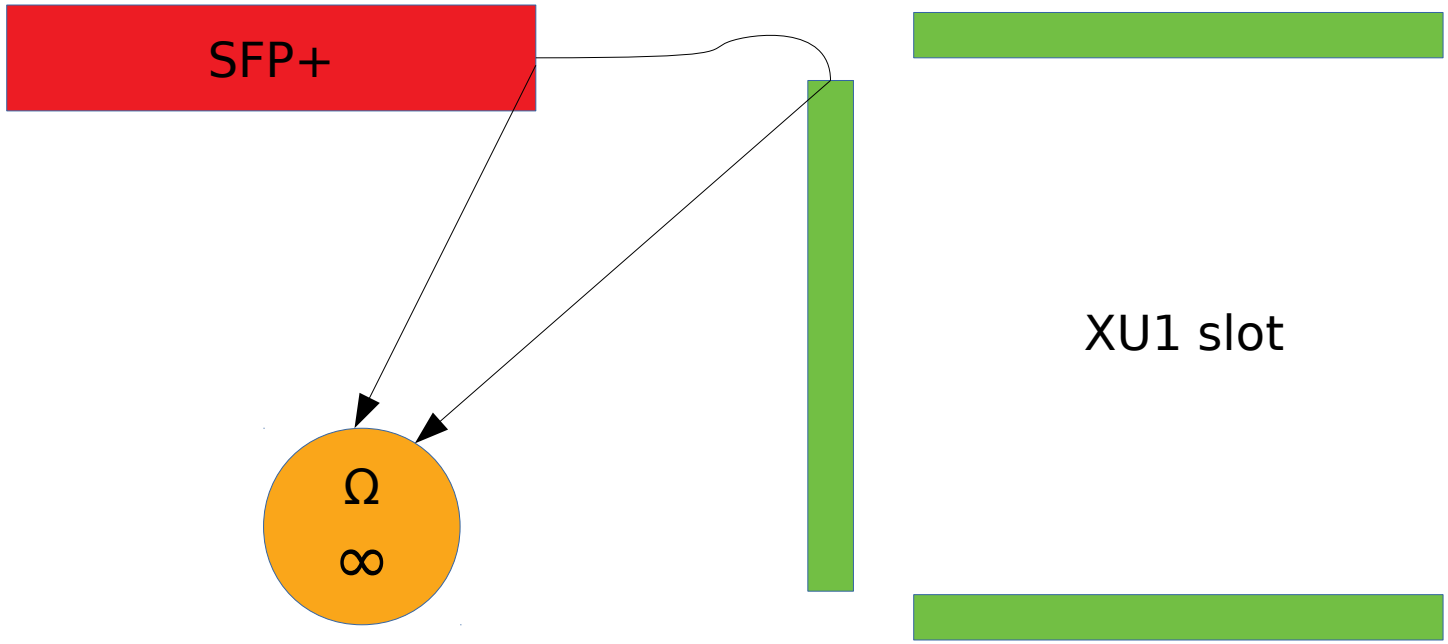




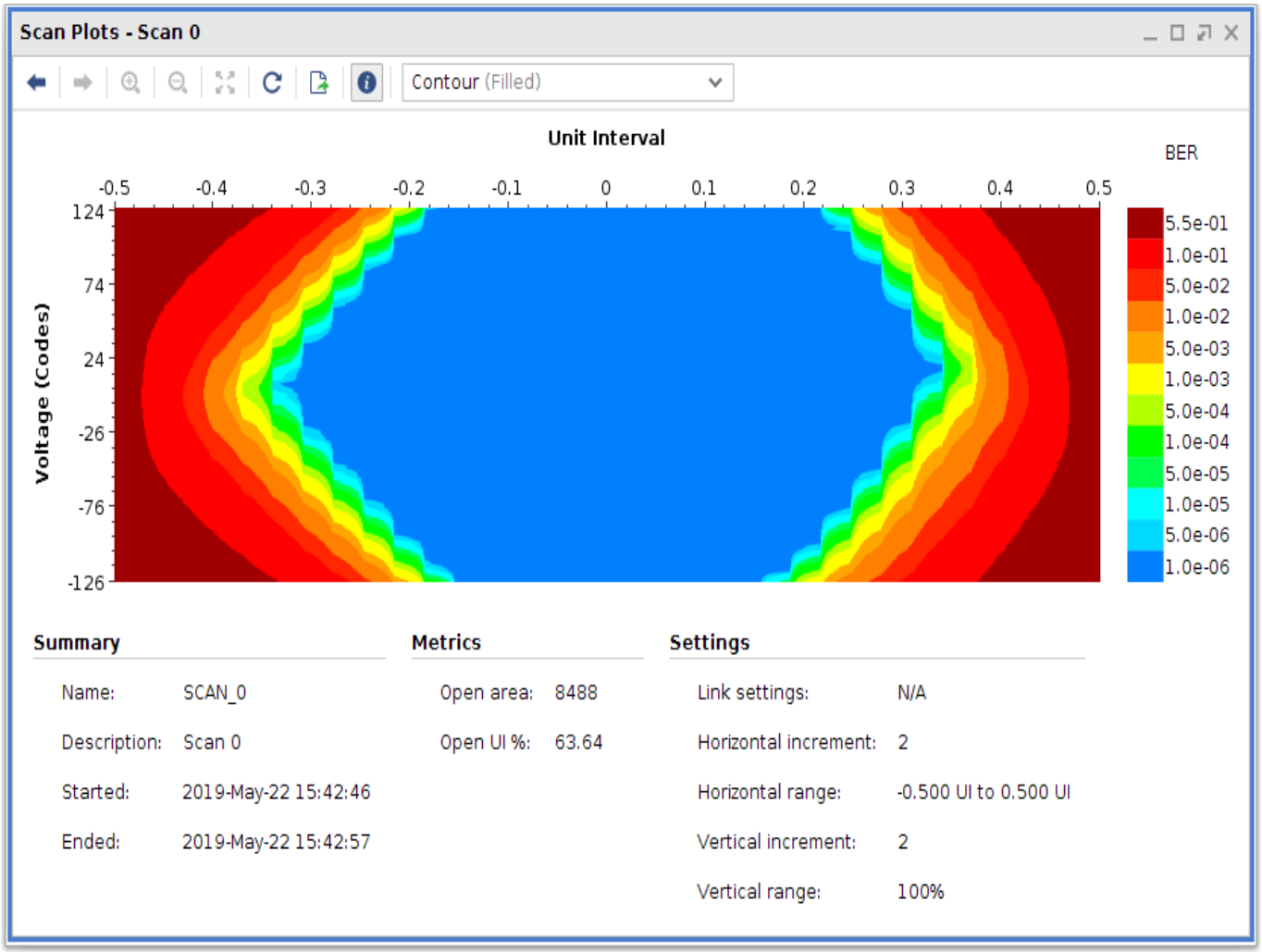
MSM#02

MSM 10G Rx line fault disclousure

Resistance between SFP+.Rx(p,n) pads and XU1 connector check.

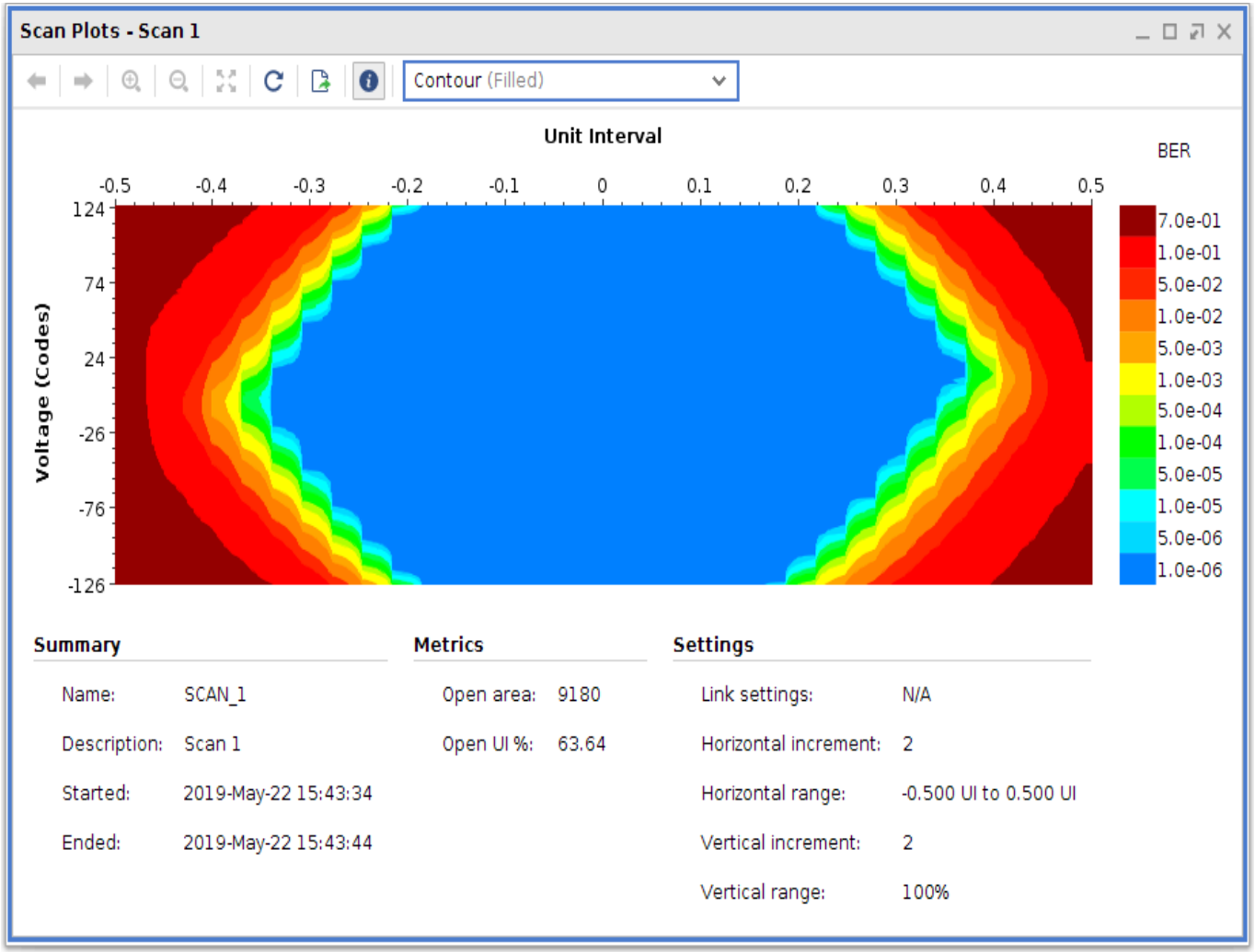


Migration to MSM. SI.



Local optical loopback. Optimal parameters. Simple EQ.

Migration to MSM. SI.



NIC fiber connection. Optimal parameters. Simple EQ.

DHPT link reliability.

Steps made to increase DHPT link stability:

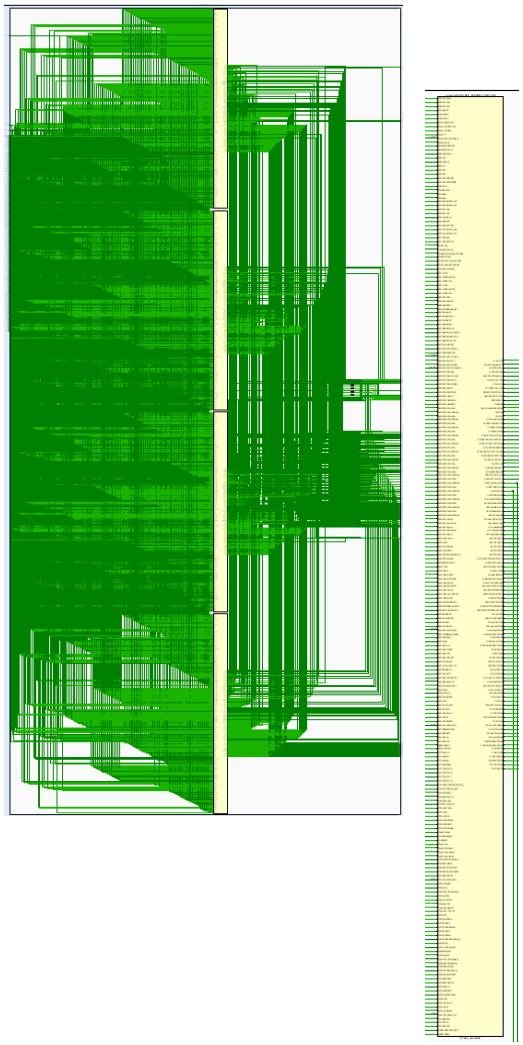
* GCK line coupling changed from AC to DC;
* Proper termination on DHPT side for GCK, TRG;
* GCK & TRG phase alignment 90°

Result gained:

No errors on the link for three days in a row.
Finger-touch test passed.

PL to PS

MGT quad
interconnect scheme



Challenge:

* Bring all the configuration wires into PS.

Strategy:

* manually: ok for prototyping, nightmare for scaling.
* semi-auto: more design time, less effort in future, less potential situations to shoot into the leg.

A library helping to solve the task designed.
AXI4lite slave interface connects to PS, regs and counters are to be connected to PL peripherals.
Configurable in top level. Support read, write regs, counters for statistics.

Sim. OK!

Further steps.

Firmware:

1. Define memory space and registers for the units need to be under control.
2. Interconnect
3. Test links.

Software:

Next presentation by Andrey Vostrukhin.

Firmware status update.

Thanks for your attention.

Questions?