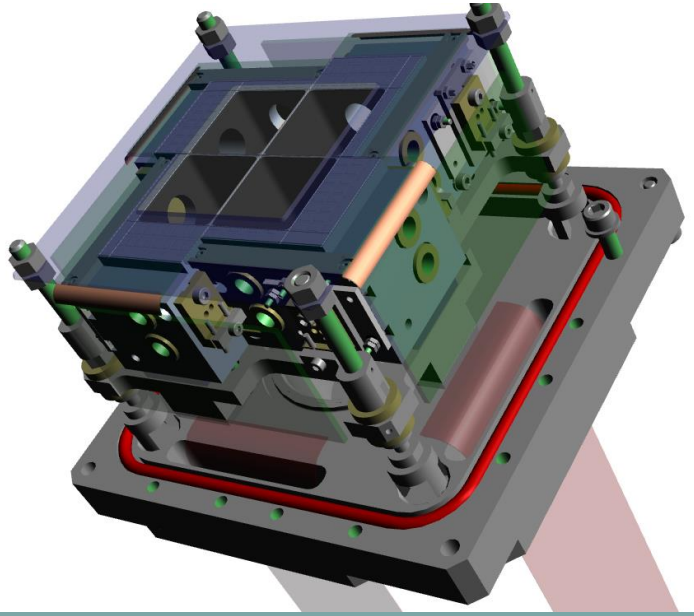
Hardware Development Status

Kloster Seeon

28.05.2019



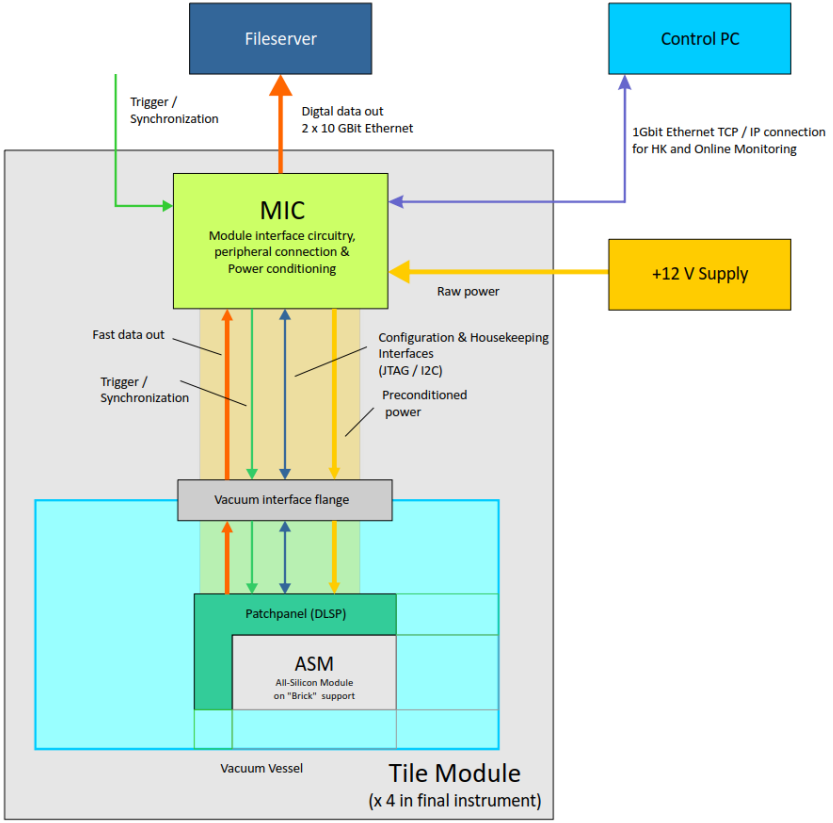
Contents

- *System components*
- Component development status
  - *Detector ASM*
  - DLSP
  - VIC
  - MIC (MSM/MBM/MPM)
  - DMC Probe Card

Module structure

Module components:

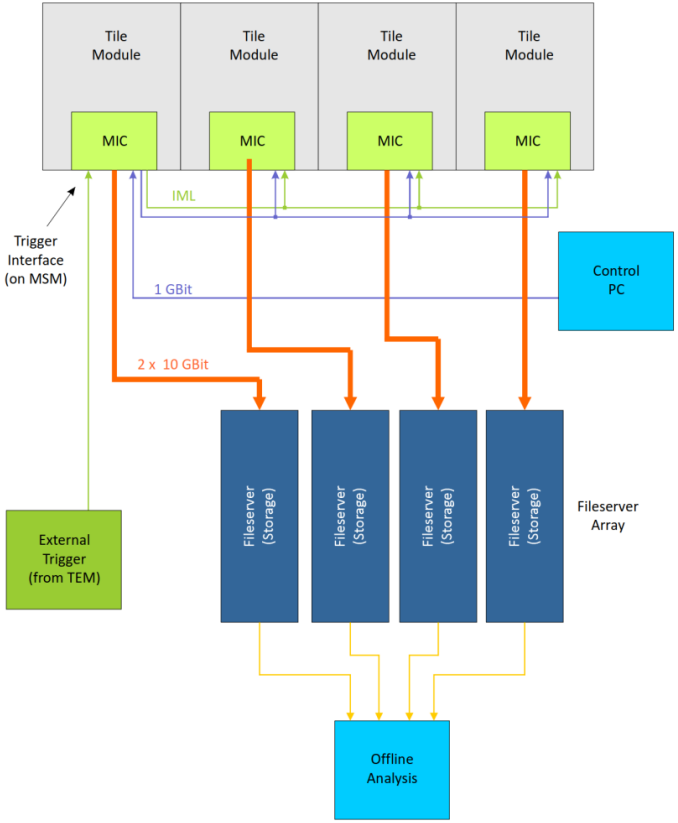
- ASM: All-Silicon module
- Brick support: Thermomechanical support and interface to main heatsink
- Patch panel: Wire bond adapter, local power conditioning and housekeeping circuitry
- Total of 4 tile modules on main heatsink in vacuum vessel
- Vacuum interface flange with flexible printed circuit for electrical connection
- Module Interface circuitry for peripheral connection
- Communication w/ control PC (housekeeping / online monitoring) using 1 GBit Ethernet interface
- Trigger input from TEM and synchronization clock
- Fileserver system for fast data storage, data transfer using 2 x 10 GBit optical interface (UDP stream)



System structure

DAQ Concept:

- Complete system is formed by 4 identical, independent tile modules
- Configuration of modules via individual standard 1Gb Ethernet link
- Control PC does configuration, housekeeping and online Monitoring
- Trigger from TEM is applied to one ("master") module
- Master distributes the trigger to slave modules using proprietary Inter-Module link (IML)
- Fast data is transferred to module-individual Fileserver storage using 2 optical 10 Gbit Ethernet connections
- Fileserver array makes data available for offline analysis
- Possible replacement of module-individual configuration link by IML based master-slave architecture in a later stage



Detector ASM

ASM:

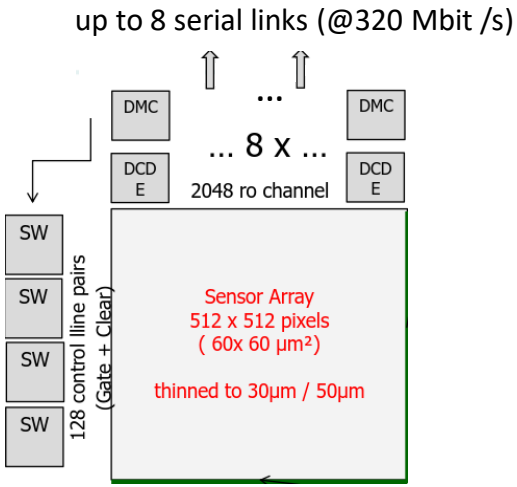
- High integration density requires integration of Detector matrix, front-end ASICs and supporting passives on common substrate
- "PCB on silicon" → All-Silicon module (ASM)
- Substrate thinned down to 50 -30 µm thickness in sensor region
- Supporting window bars

Direct Current Digitizer (DCD-E)

- UMC 130 nm technology
- 256 channels read in parallel
- 8 bit digitization, 100 ns conversion
- 64 parallel data output links @ 320 MBit/s

DEPFET Movie Chip (DMC)

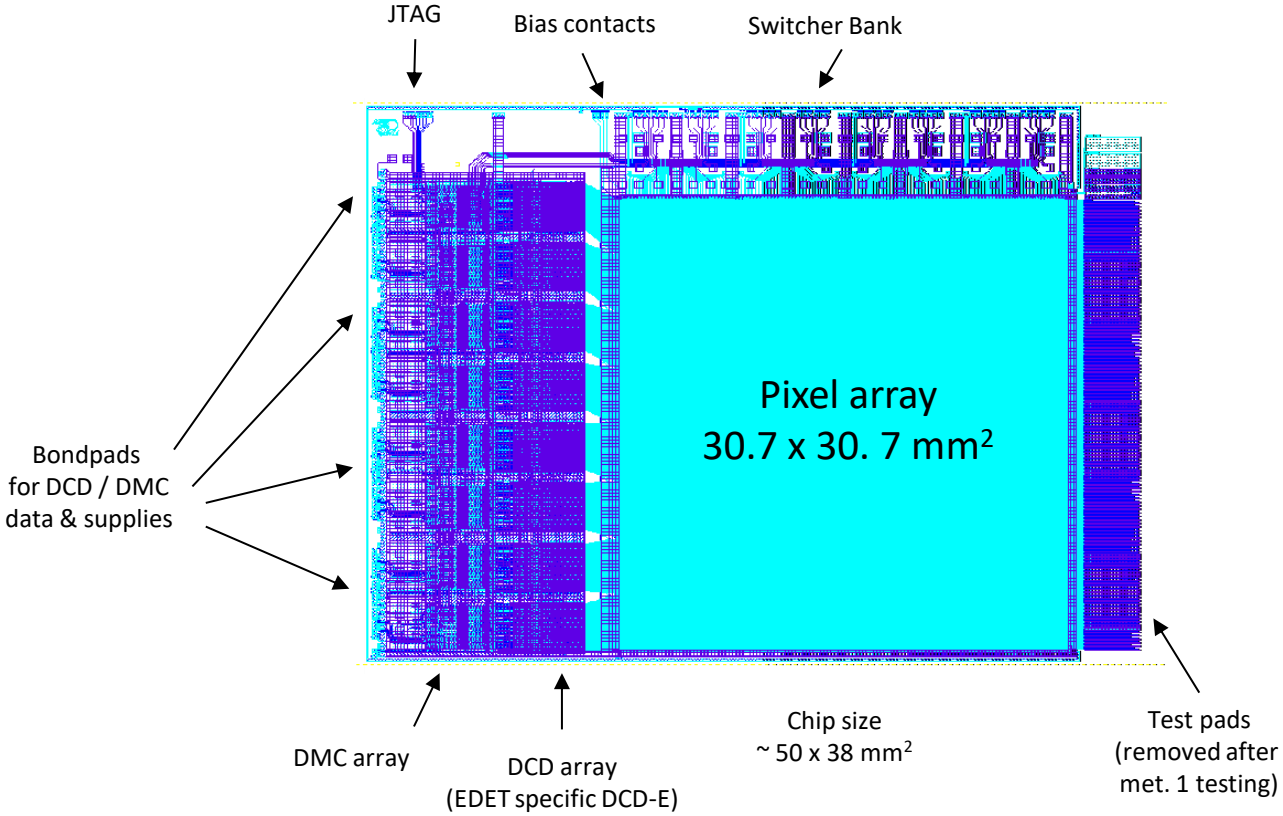
- TSMC 40 nm technology
- Data buffer, serializer & sequencer for all DCDs and Switchers
- Fast data transfer to periphery using 8 parallel 320 Mbit /s LVDS outputs



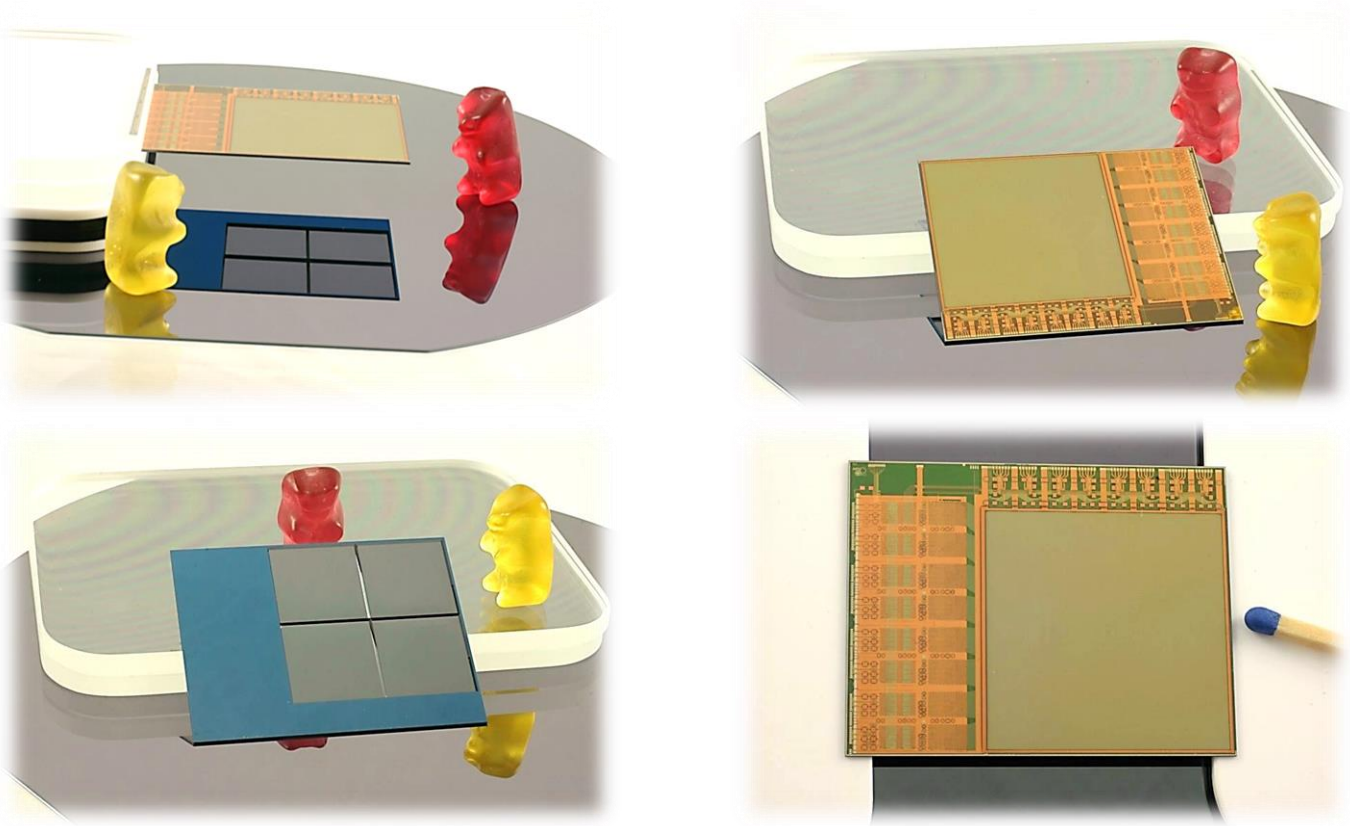
Switcher-B:

- AMS H18 HV technology
- Controller IC, 32 channels
- Each channel driving gate and clear lines of 4 ASM pixel matrix rows in parallel

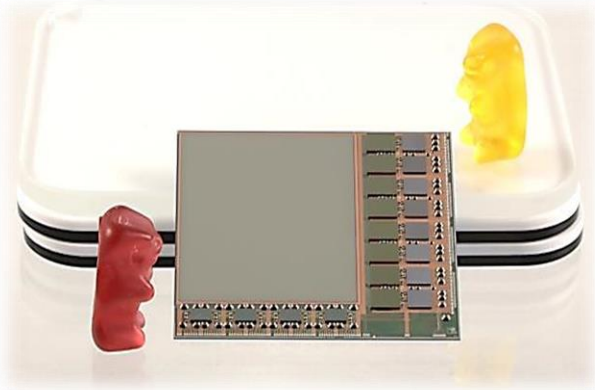
Detector ASM

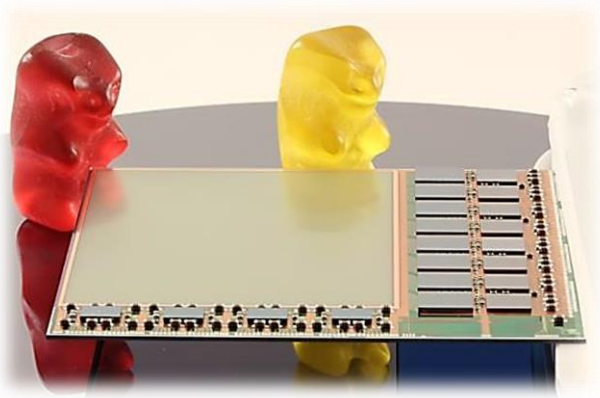


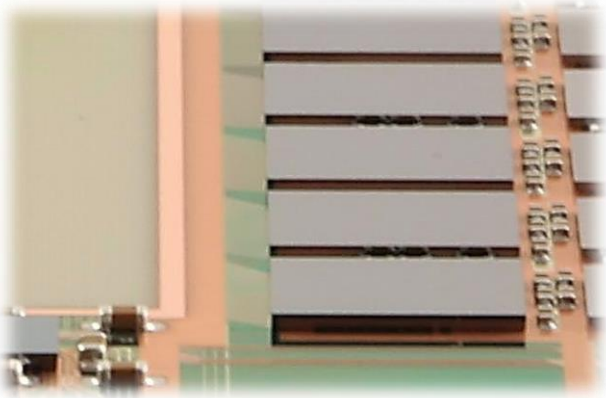
ASM – bare dies



ASM – populated dies

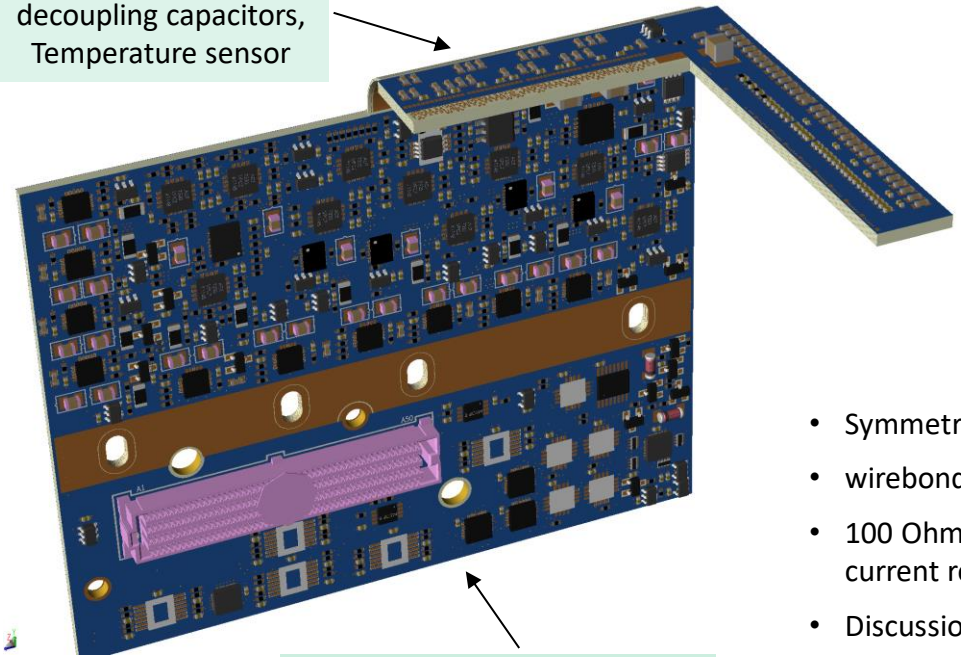




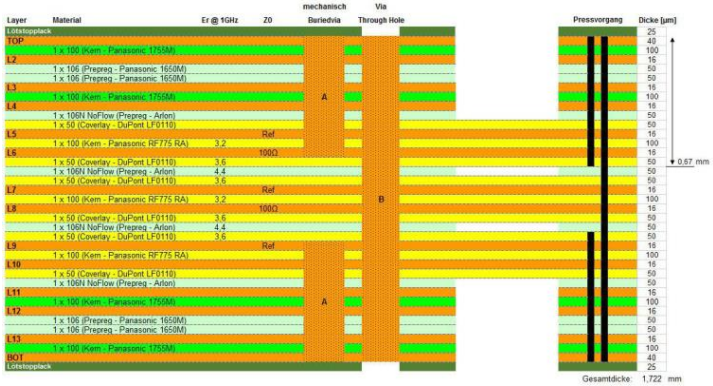


DLSP – Double L- shaped Patchpanel

wirebond pads, decoupling capacitors, Temperature sensor



LDO voltage regulators for ASICs, housekeeping, SEAF8 connector



- Symmetric layer stack up: 6 flex layers, 8 rigid layers
- wirebond fan-out by through-hole and blind vias
- 100 Ohm differential impedance on L6 and L8 with dedicated current return layers (no split plane)
- Discussion with several PCB manufactures…
- Quotation received from CONTAG, purchase order was done last week (costs 1.4kEuro per FPC, lead time 3 weeks)
- Preparation of the assembly (stencil, BOM, placement file) started

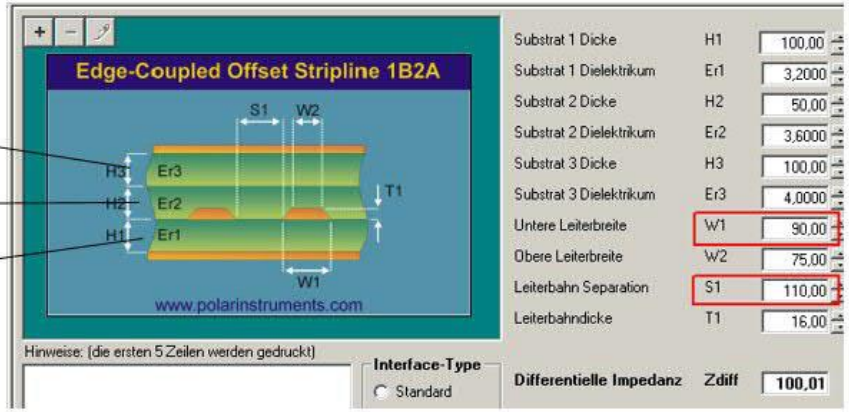
DLSP – Double L- shaped Patchpanel

100 Ohm in rigid section

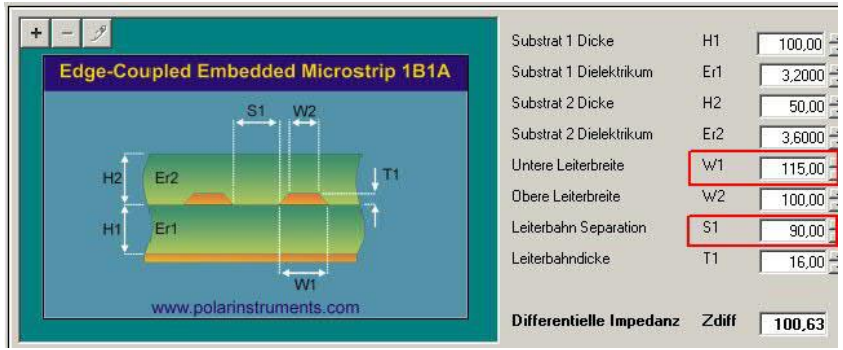
Coverlay LF0110 und NoFlow
Er = 3,6@ 1GHz und 4,4 @ 1GHz

Coverlay LF0110 / Er = 3,6@ 1GHz

Flexkern

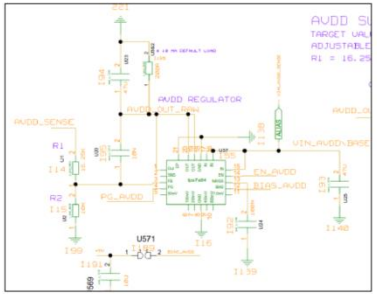


100 Ohm in flex section

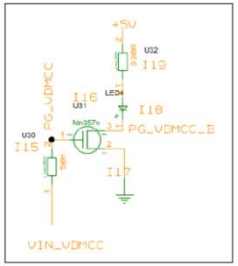


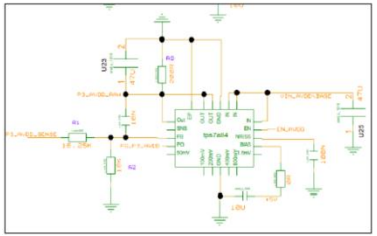
DLSP – Double L- shaped Patchpanel

Voltage	Regulator	# ICs	# ASICs	Case	Area
AVDD	TPS7A85	4	2	3.5 x 3.5 mm^2 VQFN Package	49 mm^2
AMP_LO	LT3091	4	2	3 x 4 mm^2 DFN Package	48 mm^2
VREF_IN[1]	LT3086	1	all	5 x 4 mm^2 DFN Package	20 mm^2
DVDD	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
VDMC_IO	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
VDMC_CORE	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
Switcher_VDD[2]	TVL705	1	all	0.8 x 0.8 mm^2 DSBGA Package	0.64 mm^2
Sum		16			192 mm^2

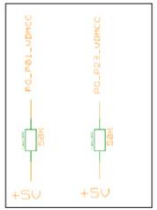


PSP





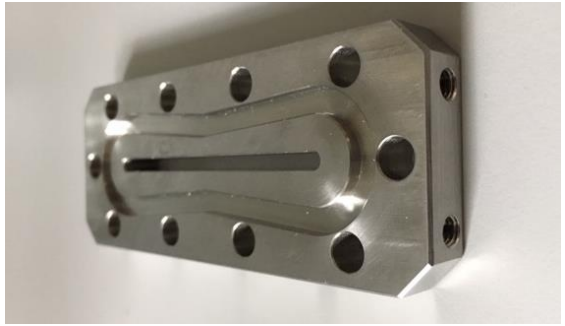
DLSP

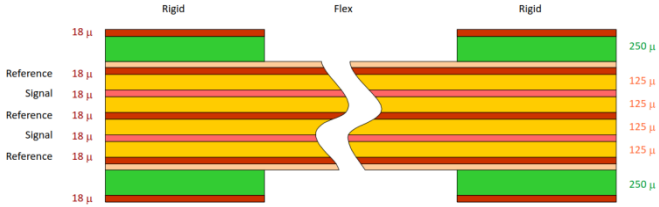


- All circuits prototyped on breadboard and PSP
- **PSP test w/ detector still to be done**

VIC

- layer stack up: 5 flex layers, 2 rigid layers
- 10 pcs ordered for ~5k @ IV Schaltungen
- delivery was scheduled for last week, then re-scheduled for today, probably next week
- status yesterday: all layers structured and pressed, solder mask is currently applied, electrical test not yet done
- Assembly needs to be further discussed and tested



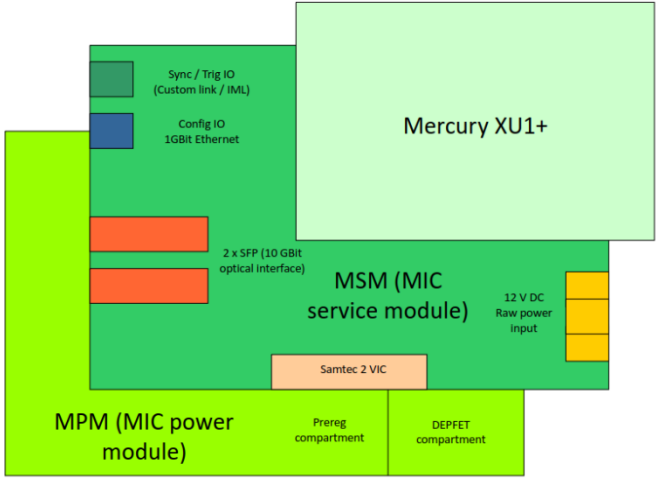


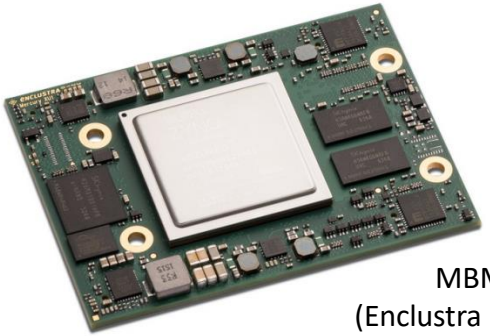
Module structure

Module Interface circuitry (MIC) :

- Peripheral interconnect based on modular stack of 3 modules
- MSM: Service module hosting physical interfaces & interconnects
  - Housekeeping & configuration
  - Fast data transfer
  - Trigger inputs
  - Connectors for Mezzanine cards
- MPM: Power module hosting pre-regulators and biasing circuits for ASM
- Provides for supply of entire module w/ a single 12 V DC poser supply
- MBM: Brain module based on powerful Zynq UltraScale FPGA from Xilinx
- Service functions, fast data transfer using MGBTs and potential data compression and preprocessing

News on MSM in Mikhail's talk

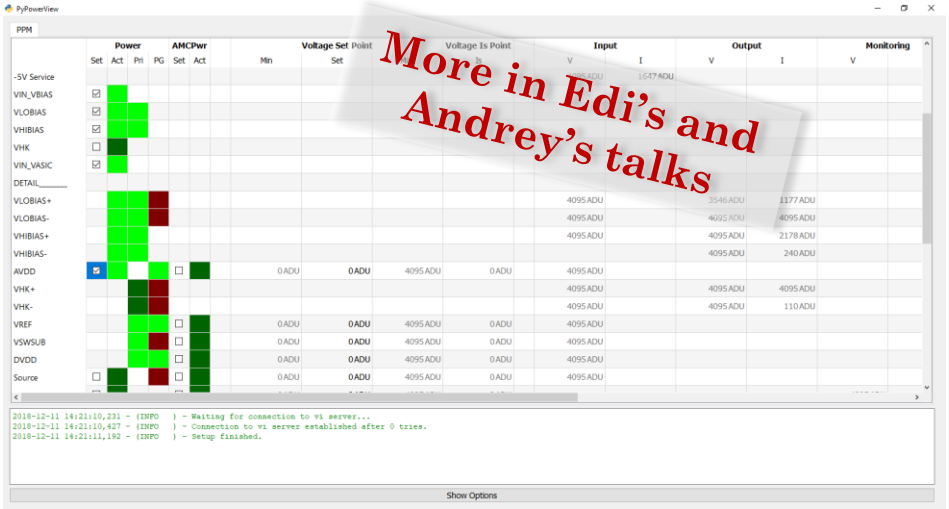




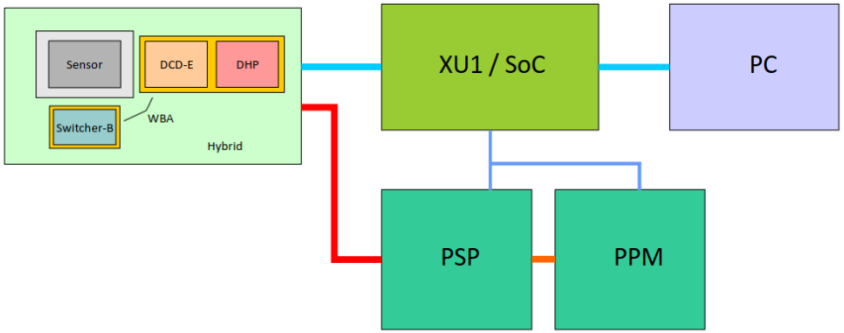
MBM module
(Enclustra Mercury + XU1)

Small-size prototypes

- Rollout of small-size prototypes in DHP/DMC configuration for representative tests
- Uses qualified EDET component prototypes (PSP, PPM)
- PyPowerControl software (PPC)
  - Modular software to control PSP, PMP via I2C
  - GUIs for ASIC configuration, Power supply control and sequence implemented



More in Edi's and Andrey's talks



Thanks for your attention