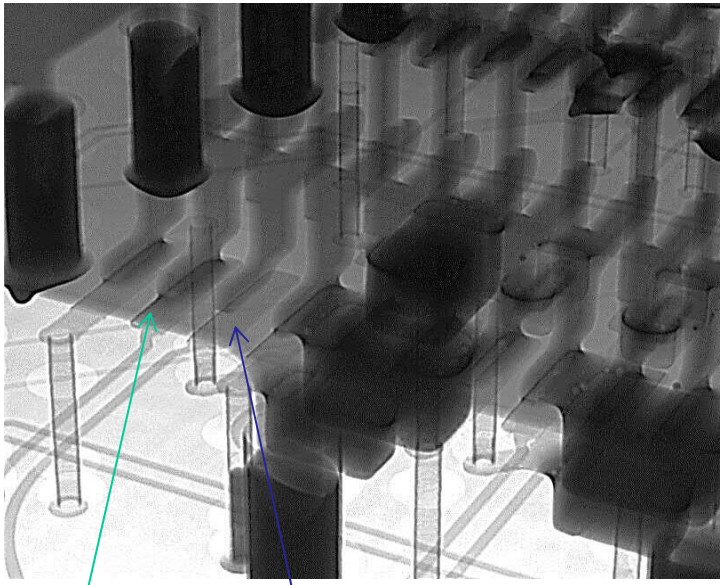
Hardware development status overview

EDET splinter meeting
Kloster Seeon, 28.5.2019

Component development: MSM

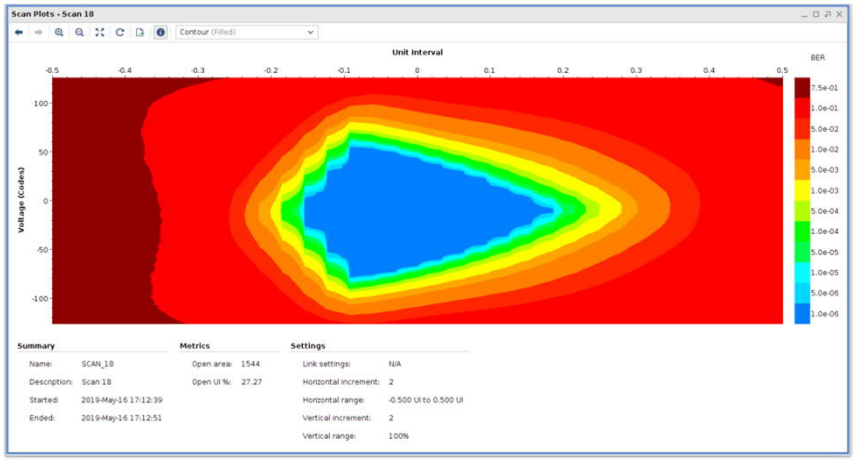
Status (details see subsequent presentations):

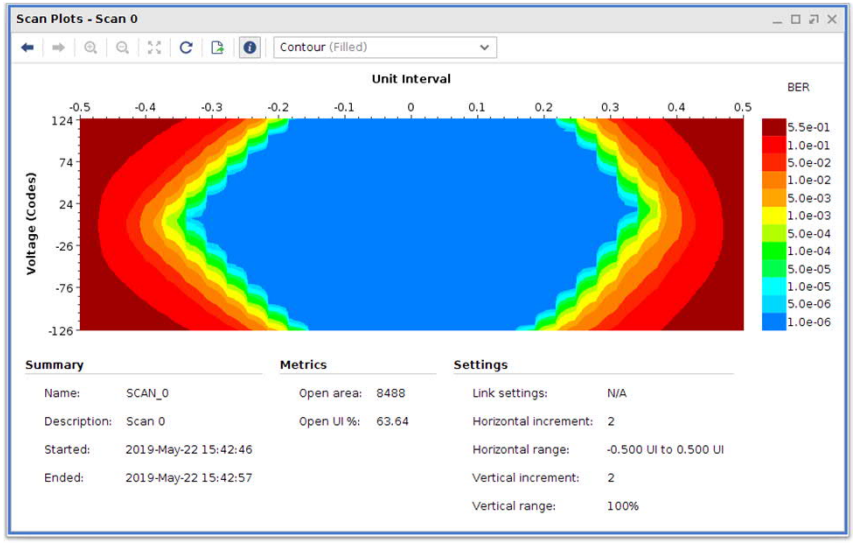
- MSM issues w/ eye diagram solved (see talk by M. Polovykh)
- Traced back to faulty solder joint
- Problem w/ board population
- All units will be screened



Good connection

Bad connection





Component development: VIC & DLSP

Status (details see talk by C. Koffmane):

- VIC still in production
- Delivery scheduled today (but will take probably until next week)
- Arrange population / define procedure
- DLSP: Changes in layout (Fanout)
- Layout assessment completed (Contag)
- Quote received / order to be placed

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AUFTRAGSBESTÄTIGUNG 63014 **Lieferdatum ab Werk: 28.05.19**
Datum: 15.05.2019

Bestellnr: 4404874/K4005

Pos.	Artikel-Nr.	LP-Bezeichnung Art.Nummer Kunde	Menge	Einheit	Preis	Rabatt	Summe	
Lieferverzug - wir bitten um Verständnis !								
1	190114 SF	VIC_20190304 RoHS konform IPC A 600 aktuelle Version Klasse II	10	Stk	412,78		4.127,80 EUR	1
		Impedanzprüfung	1		350,00		350,00 EUR	1
		Einmalkosten LP	1		1.200,00		1.200,00 EUR	1

Eine Überlieferung im Rahmen unserer AGBs ist zulässig.

Zahlungsbeding.: **30 Tage rein netto**
Versandart: **UPS Standard**
Lieferbedingung: **ab Werk**

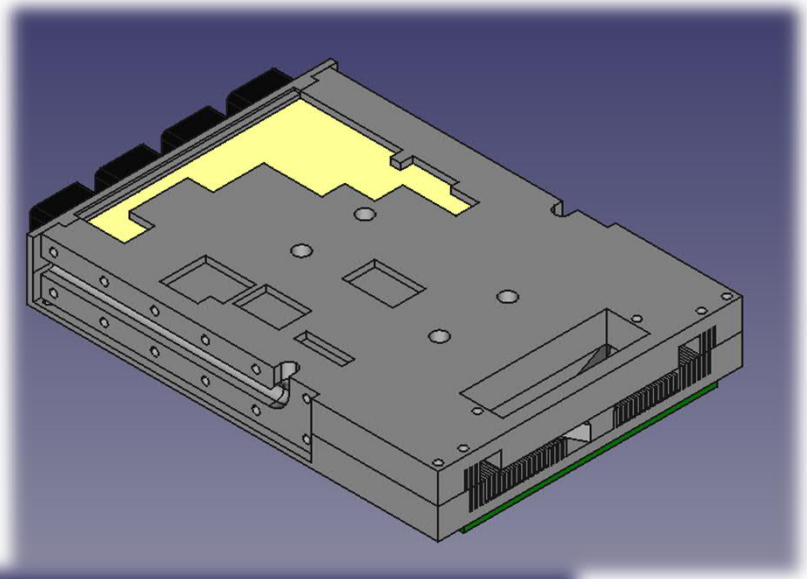
BITTE BEACHTEN SIE, DASS UNSER BETRIEB WEGEN BETRIEBSURLAUB vom 12.8. bis 16.8.19. geschlossen bleibt. Wir bitten um entsprechende Disposition !

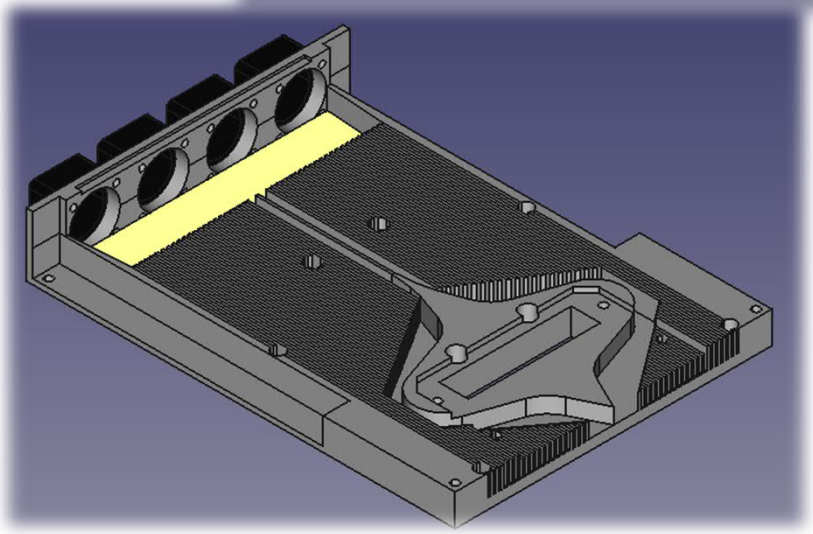
Netto:	5.677,80 EUR
MwSt: 19 %	1.078,78 EUR
Summe:	**6.756,58 EUR**

Component development: MPM & Stack

Status:

- MPM development not yet resumed
- PPM results promising
- Waiting for results of DEPFET supply test
- No challenging design work
- Rearrangement of existing pieces
- Draft design of mechanical stack for MSM / MPM
- Available for Djordje

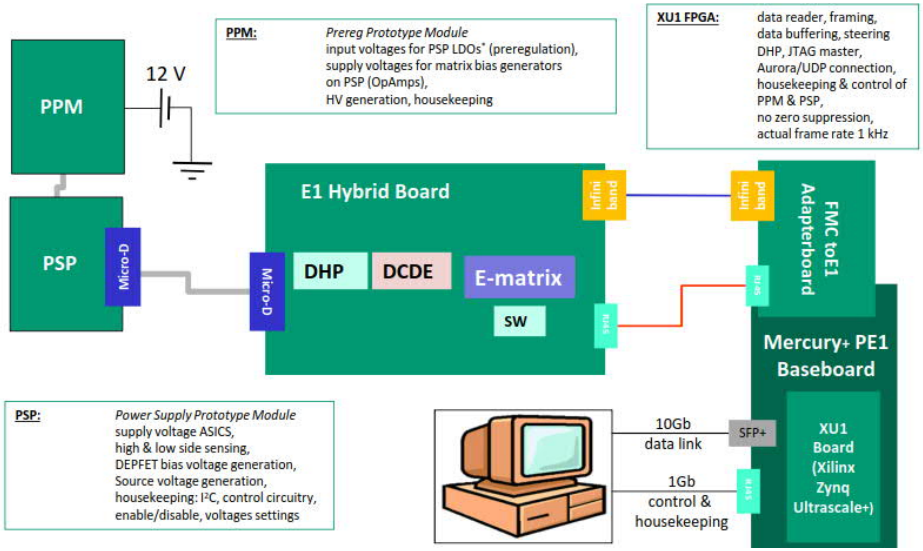


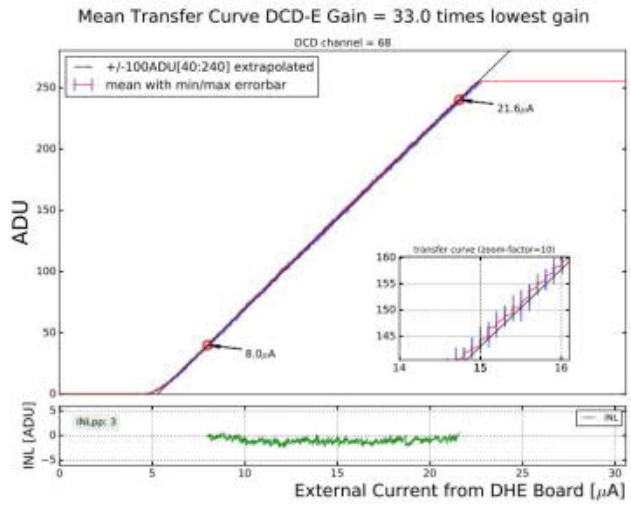


Prototype system & Software

Status (details see talks by E. Prinker & A. Vostrukin):

- System is operational
- Large variety of capabilities & measurements
- Measurements on noise and analog part of DCD show good performance
- Final test still pending: Connection of Matrix
- Also: Switch to MSM as digital platform
- Discuss transfer to Hamburg

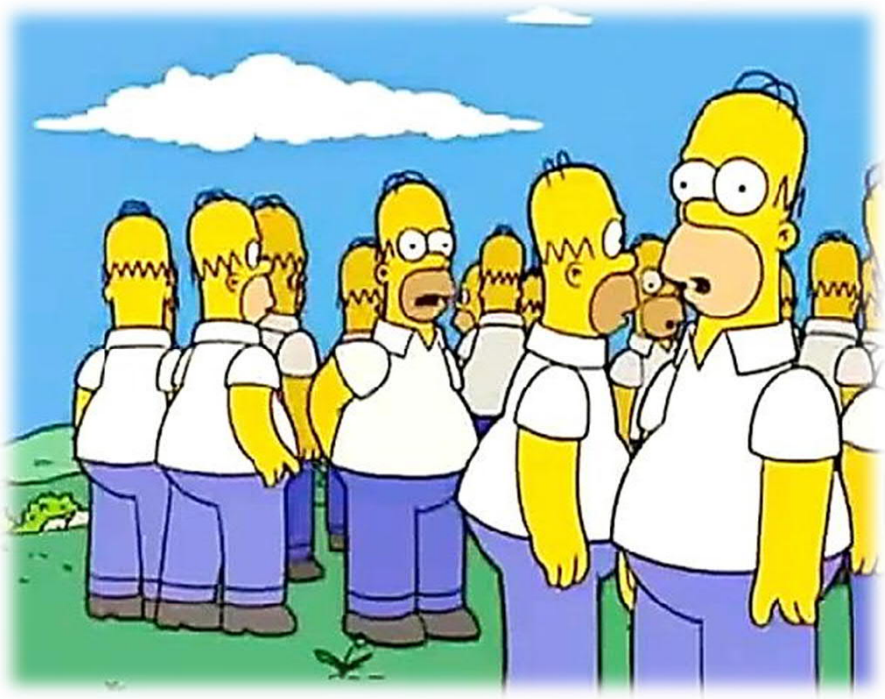




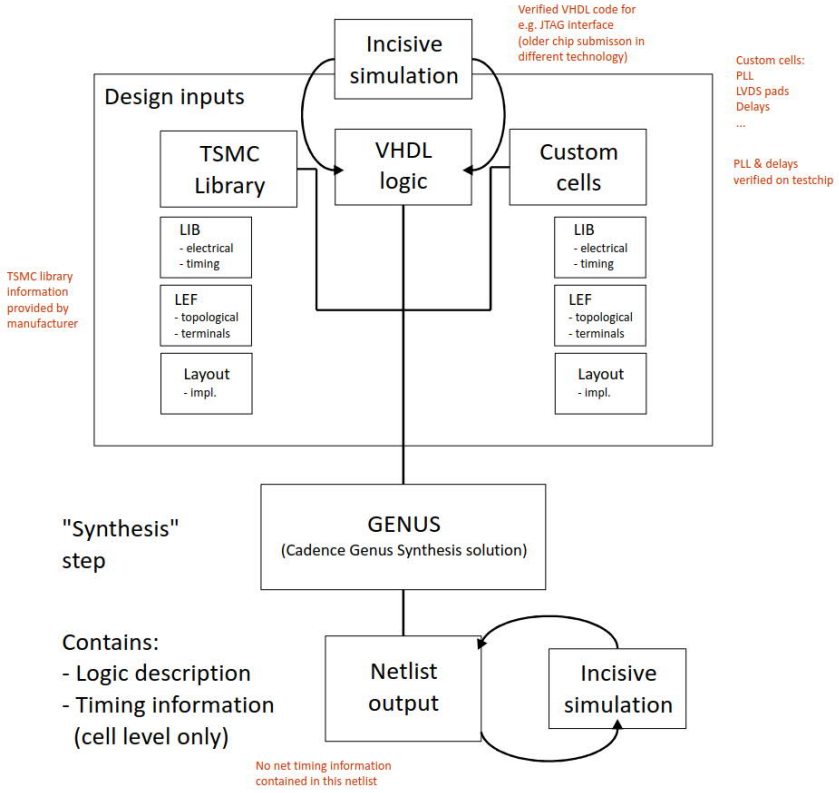
Firmware

Status (details see talk by M. Polovykh):

- Current tasks:
  - Transfer to MSM platform
  - Enable second 10G port
  - Expand to 8 DHP inputs (preparation for large module)
- Not just "more of the same"...



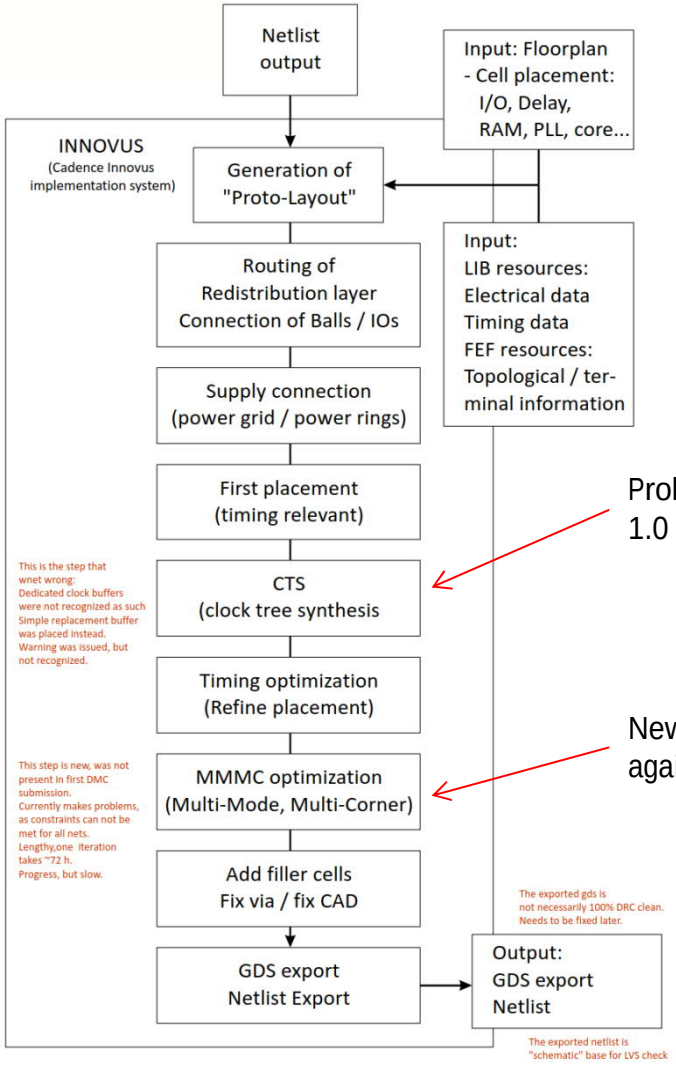
Component development: DMC



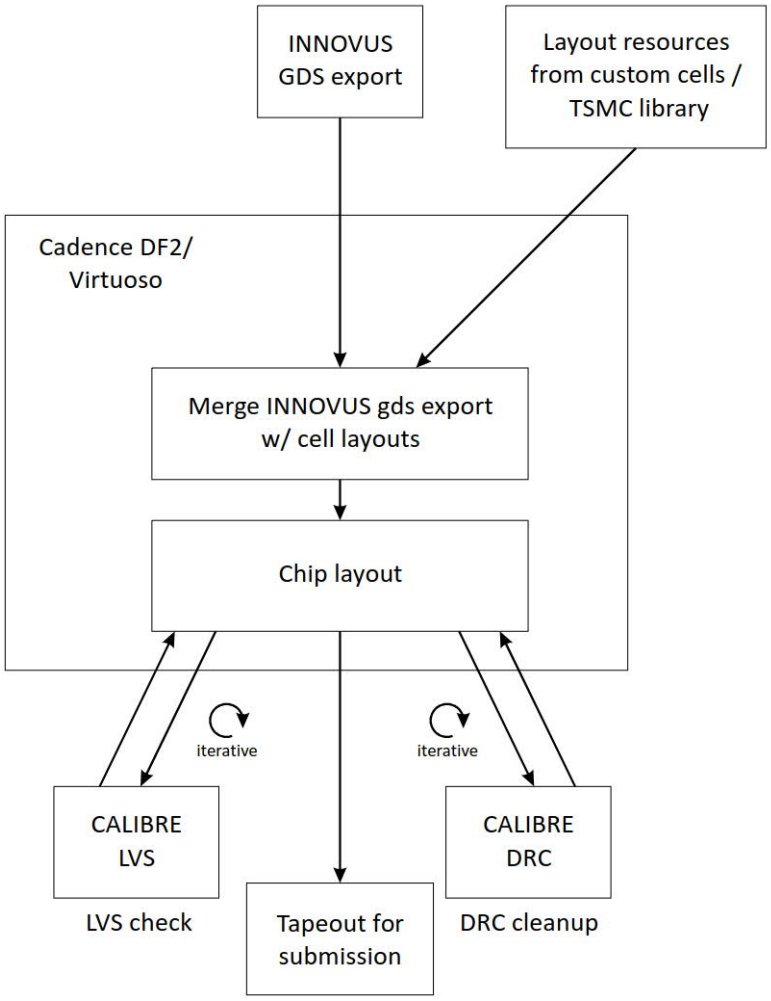
Status (see talk by A. Wassatsch):

- Understanding ill-fated DMC 1.0
- Indications that also JTAG problems are related to clock-tree issue / too slow risetime of JTAG clock
- New, improved layout on the way:
  - Fixed clock tree issues
  - New step: MMMC optimization
- In addition:
  - Setting up process flow for post-layout verification
  - Timing annotated digital simulation
  - Power verification
  - Suitable workbench
- External reviewer(s)
- Back on track

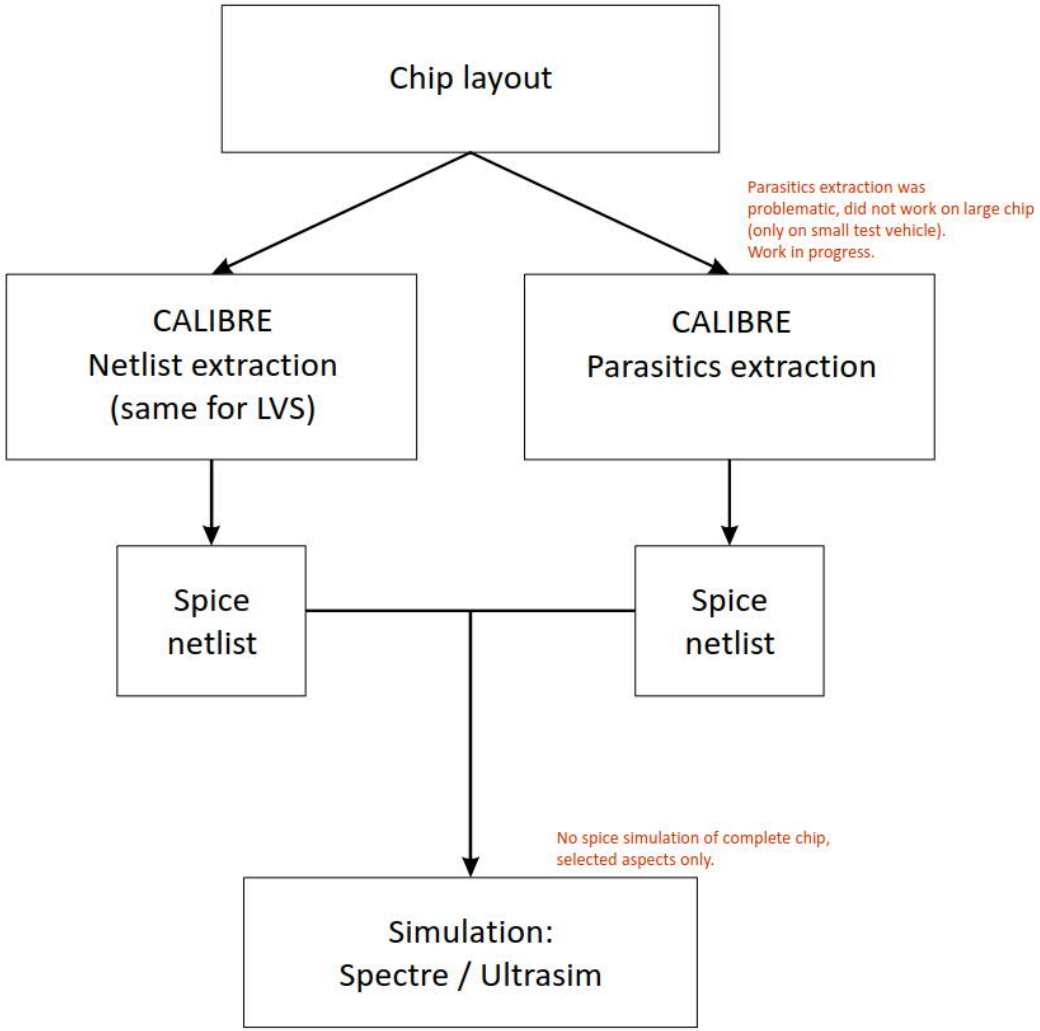
Component development: DMC



Component development: DMC



Component development: DMC



Plan B / Upgrade

Status (see talks by A. Vostrukin and M. Polovykh):

- Setback on DMC 1.0 triggered investigation of backup options
- Variety of options were considered, most of which were dismissed due to incalculable risks and technological problems
- 2 remaining options, which appear challenging, yet feasible
- Data capturing / data handling using FPGA modules directly connected to DCD output
- Requires variety of demonstrator developments / feasibility studies w/ focus on advanced interconnection technique and fast data transmission
- DMC development is back on track, but still "Plan B" related developments are continued with lower intensity
- 2 Reasons:
    - Technologies relevant for later follow-up developments
    - "Plan B" module could work w/ full 80k framerate

"*Back up?!* ... That's your backup plan?! Excuse me for saying so, but your backup plan could really use a backup plan."

Summary

Next pending topics:

- Primary objectives:
  - Operate Prototype w/ matrix
  - Populate and test VIC & DLSP
- Large module operation w/ DHP comes within reach
- Must discuss handling and mounting procedures to be prepared.