DMC status update

Edet Meeting @ Kloster Seeon

25 May 2019

DMC timing optimization

- MMMC (Multi-mode Multi-Corner) optimization
  - Goal: make the final circuit more robust (also @ the corners)
  - Check against different combination of voltage, temperature, corners and parasitic load
    - → increased effort for the P&R tool to find a possible solution for all conditions
    - → currently not a 100% solution for all combination found
  - Introduction of MMMC optimization also requires different naming scheme for the io-voltage signals
    - → adapted parts for the bump assignment und power RDL routing
- Final placement oriented reordering of JTAG chains (delay, boundary-scan) to optimize the routing
  - Implemented in VHDL and BSDL description

Cutting edges

- Bumped chips arrived begin 2019
  - dimensions slightly bigger as designed

→ TSMC/IMEC will provide for the next submission precise cutting (must be remarked on the ordering form)