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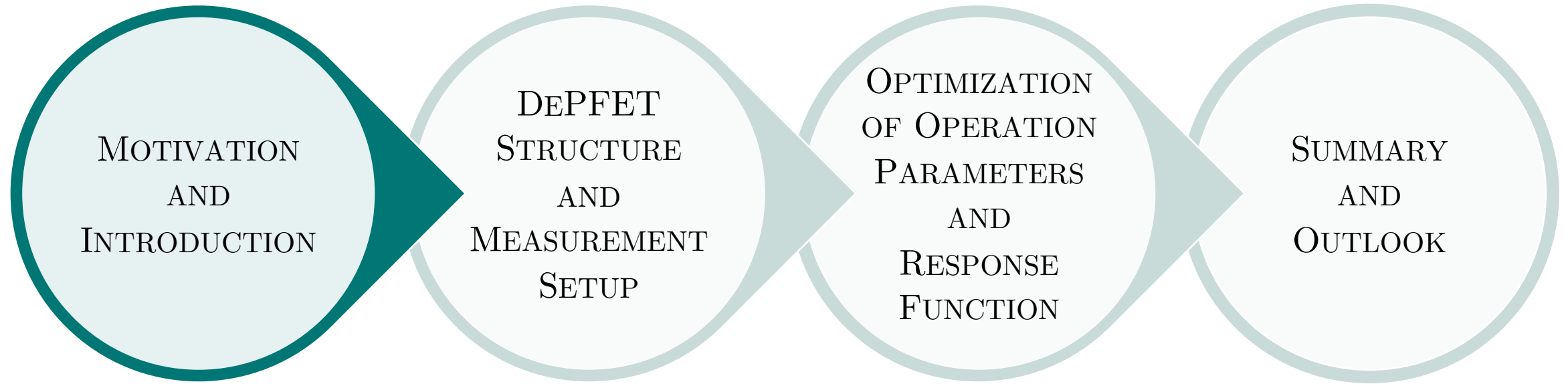
# EDET DH80k – Characterization of the sensors with low noise setup

23<sup>rd</sup> International Workshop on DePFET Detectors and Applications

12/03/2019

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MOTIVATION  
AND  
INTRODUCTION

DEPFET  
STRUCTURE  
AND  
MEASUREMENT  
SETUP

OPTIMIZATION  
OF OPERATION  
PARAMETERS  
AND  
RESPONSE  
FUNCTION

SUMMARY  
AND  
OUTLOOK

# Motivation

for the project

Stroboscopic imaging provides insights to the dynamics of processes:

- short, discrete illumination periods with high intensity
- decouples exposure time, image contrast and motion blur
- pulse intensity defines the image contrast
- frequency of illumination defines time resolution
- pulse duration defines impact of motion blur

Challenges of stroboscopic imaging in TEM world:

- real space imaging → high granularity
- high intensity → high dynamic range
- direct electron detection → thin substrate
- high pulse frequency → high framerate
- “grey scale” image → no data reduction possible



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# Introduction

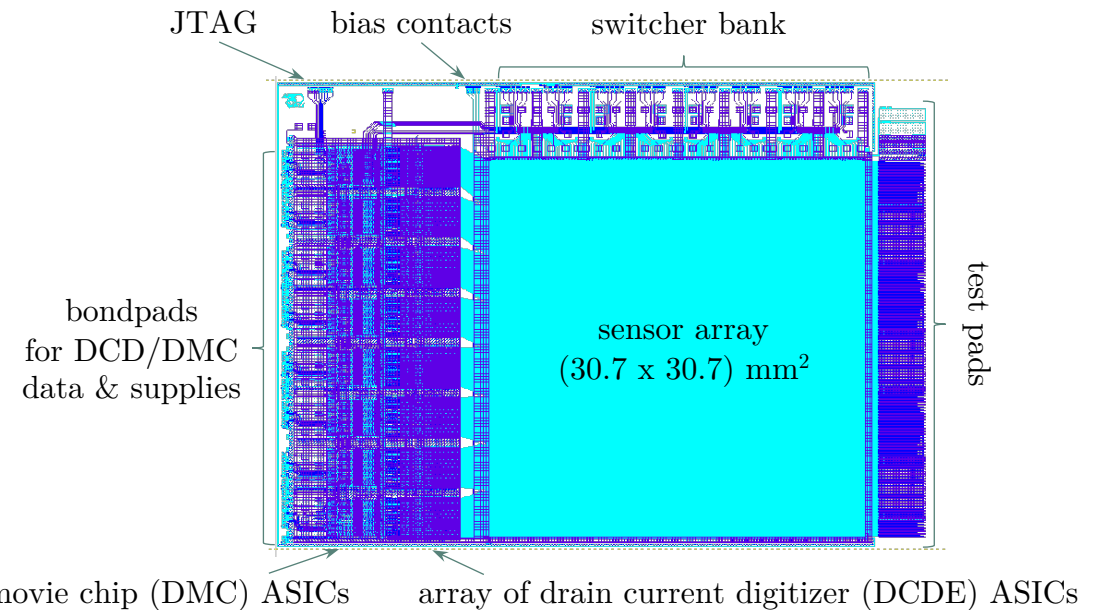
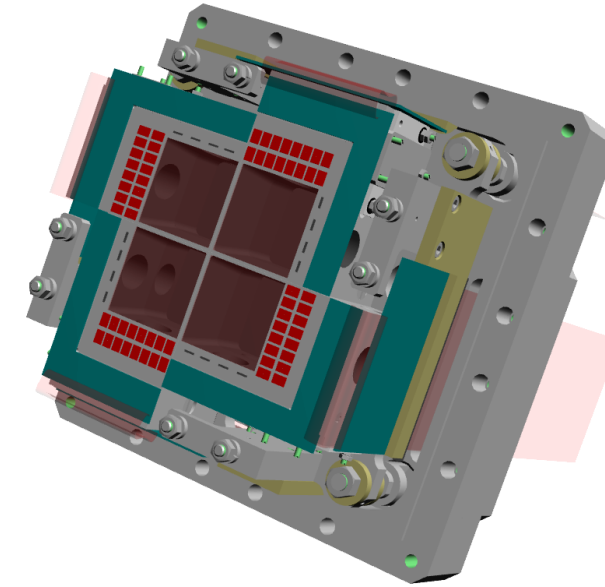
to the camera system and its challenges

## Camera system:

- focal plane area (FPA) consists of 4 individual and independent modules (“tiles”), each capable of stand-alone operation
- small sensitivity gap between tiles (1.2 mm)
- All Silicon Module (ASM)
- readout in rolling shutter mode, 100 ns/row, 4 rows in parallel
- maximum framerate of 80 kHz or 12.8  $\mu$ s/frame
- front end electronics (FEE) buffers bursts (movies) with 100 frames
- maximum burst rate 100 Hz

## Data rate:

- 8 bit digitization resolution:
  - tile module data rate of  $\sim 3$  GB/s
  - total data rate of  $\sim 12$  GB/s
- data reduction difficult if not impossible



# Introduction

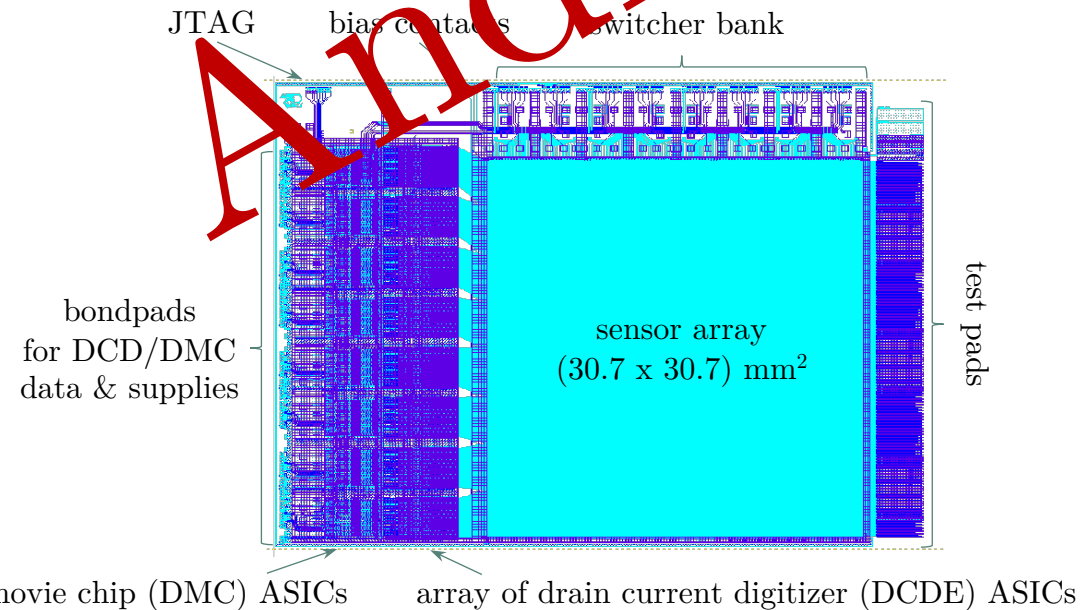
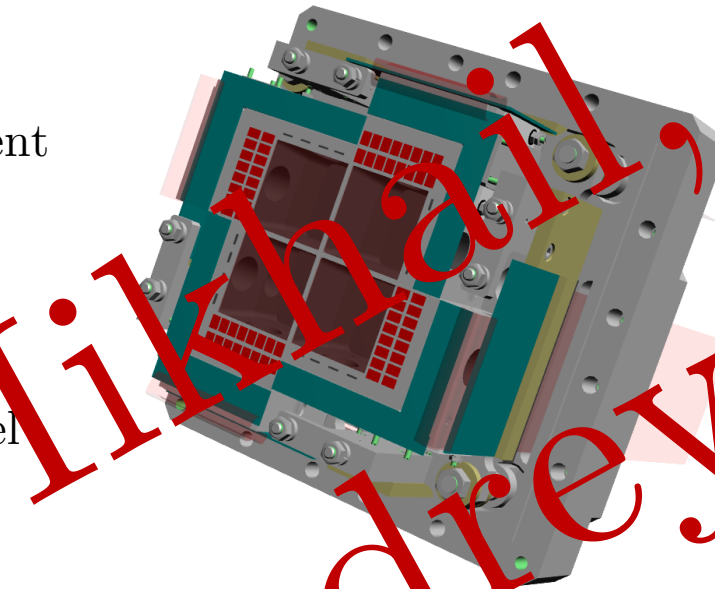
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## Data rate:

- 8 bit digitization resolution:
  - tile module data rate of ~3 GB/s
  - total data rate of ~12 GB/s
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# Introduction

to the camera system and its challenges

## Sensor array

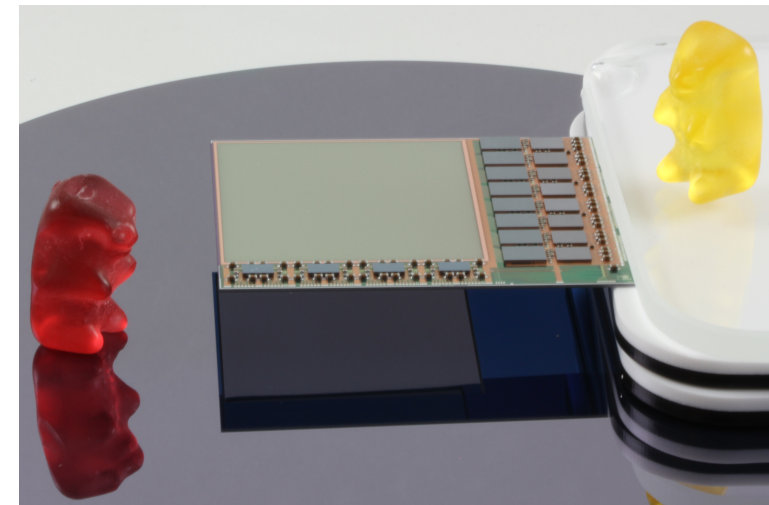
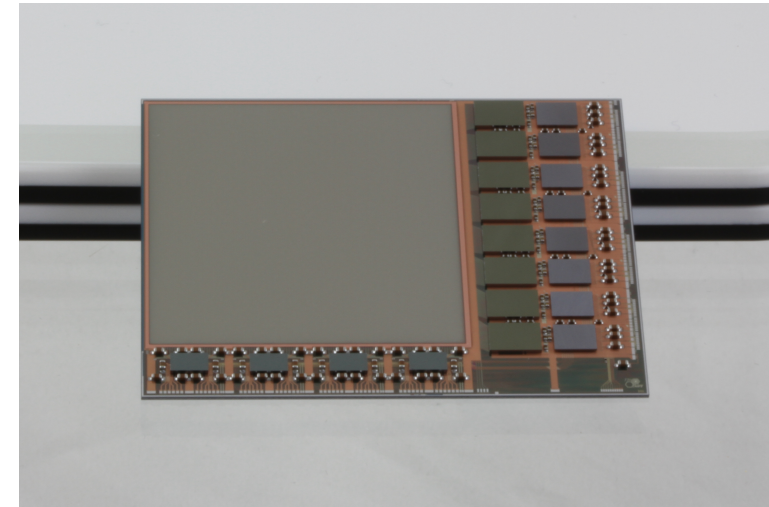
- 1 MPixel for the complete FPA
- 512 x 512 pixels per tile
- (60 x 60)  $\mu\text{m}^2$  pixel size

## Dynamic range of pixels:

- single primary  $e^-$  sensitivity
- capable of storing the signal from 100 primary  $e^-$  at 300 keV ( $\sim 800\text{k}$  signal  $e^-$ )

## Spatial resolution improvements:

- reduce  $e^-$  multiple scattering
  - thin sensitive detector substrate (50  $\mu\text{m}$  and 30  $\mu\text{m}$ )
- reduce  $e^-$  back scattering
  - no support layer
  - highly effective beam dump



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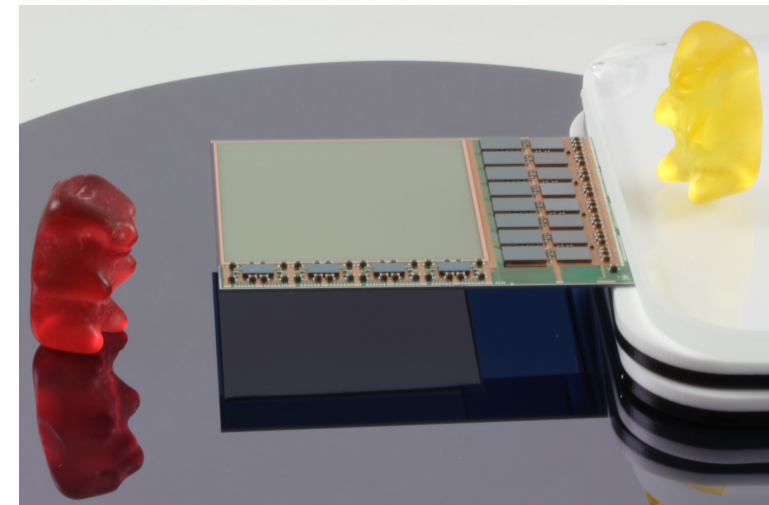
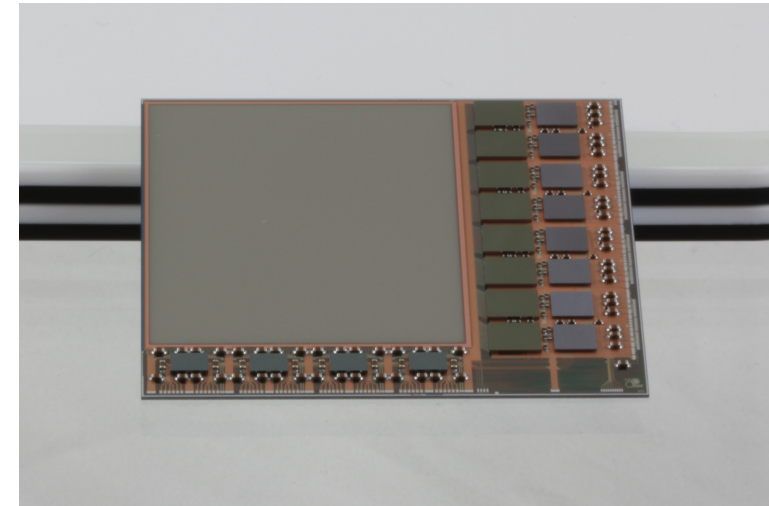
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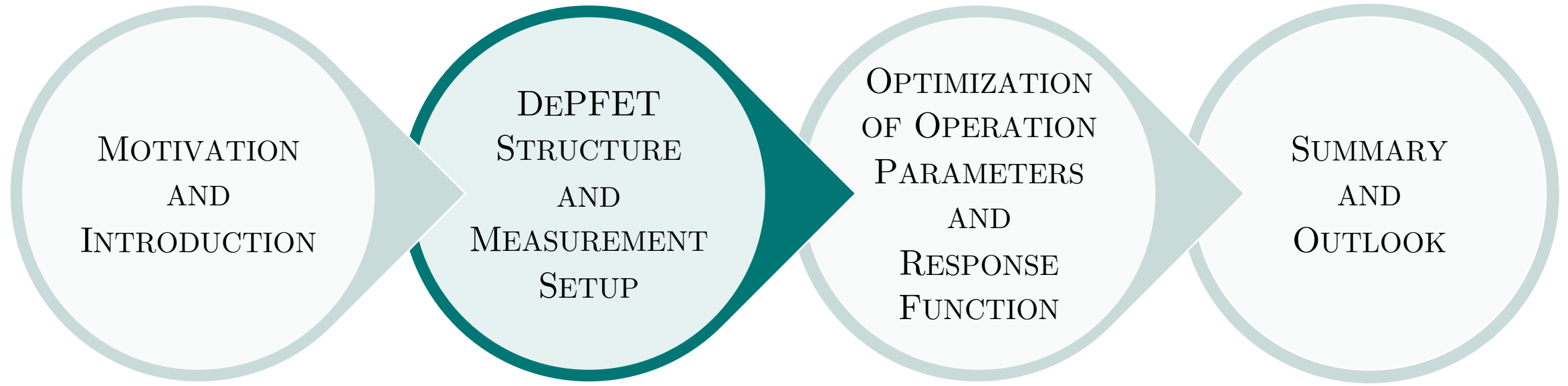
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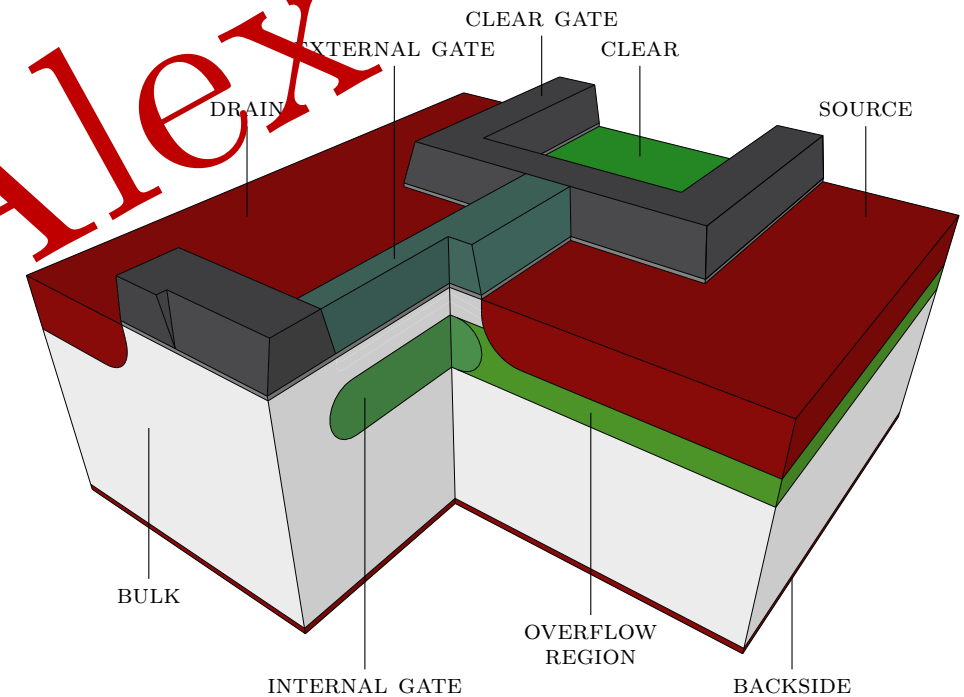


# The DePFET structure

and its positive sides

Depleted p-channel Field Effect Transistor on high resistive n-doped bulk

- integrated 1<sup>st</sup> stage amplification ( $g_q$ )
- charge storage capability
  - readout on demand
  - rolling shutter mode
- small capacitance and low noise
- high quantum efficiency and fill factor
- fully depleted bulk
  - optionally thinned
- front- or back-side illumination possible
- easily scalable
- adjustable dynamic range
- signal compression
  - achieved by overflow charge storage regions with different  $g_q$



# The DePFET structure

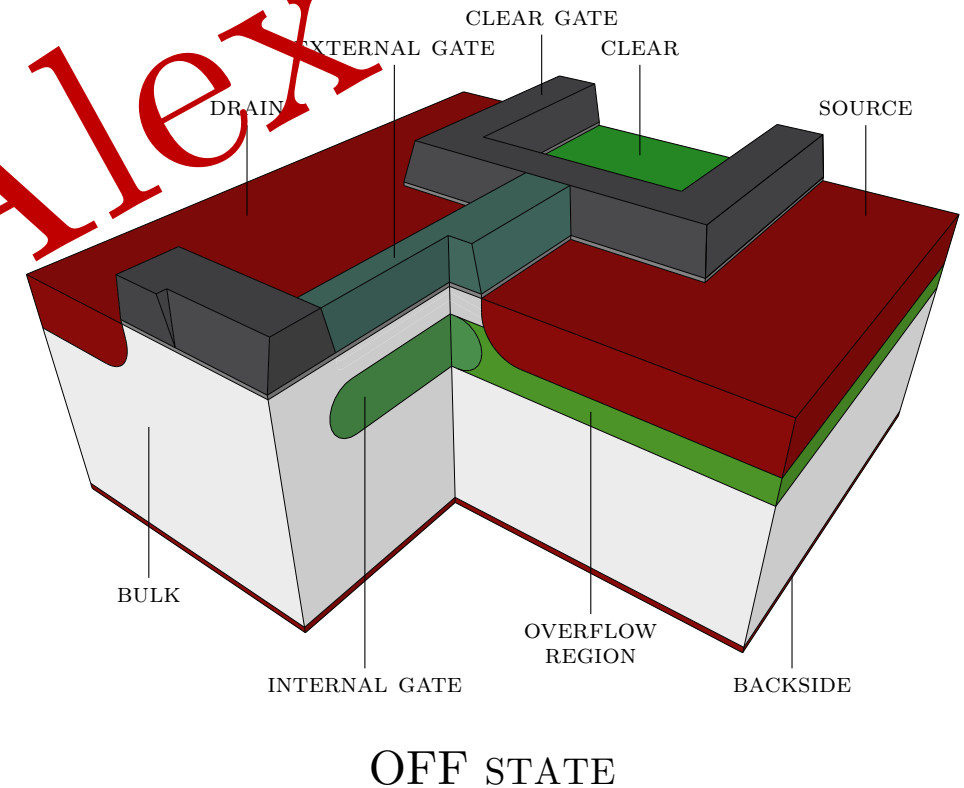
and its operation principle

Two states of operation:

- OFF state:
  - idle state, no power dissipation, but collecting signal charge
- ON state:
  - transistor current depending on signal change in internal gate

presented by  
Johannes,

Alex

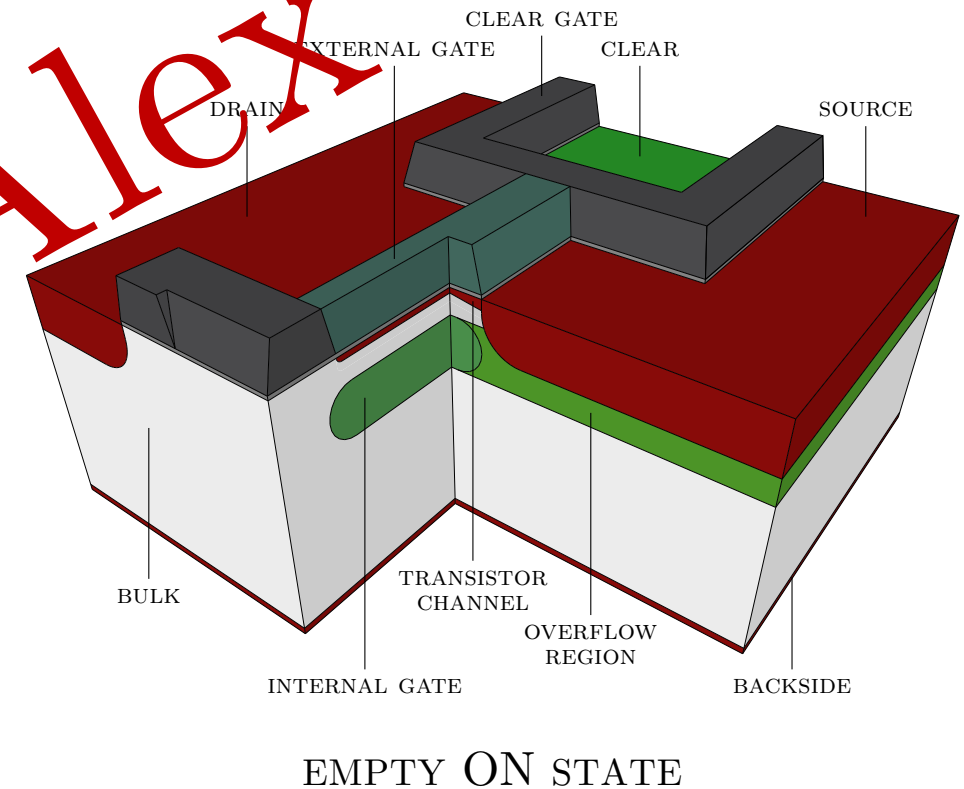
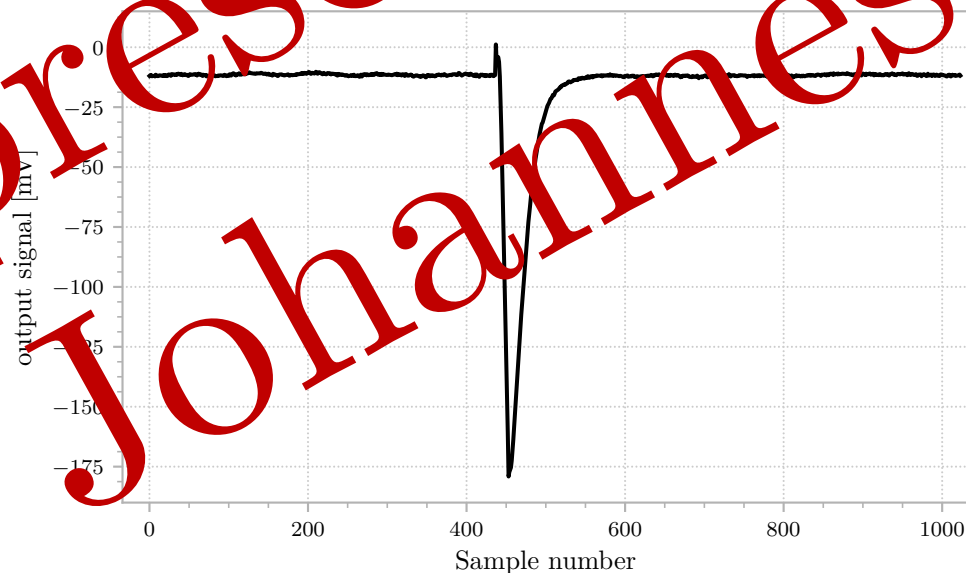


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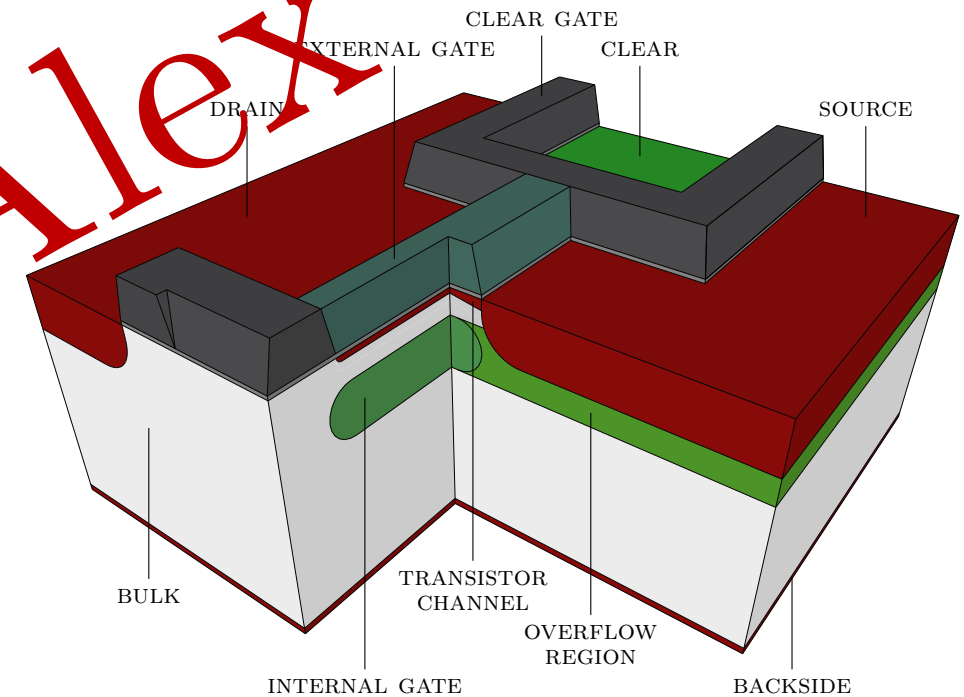
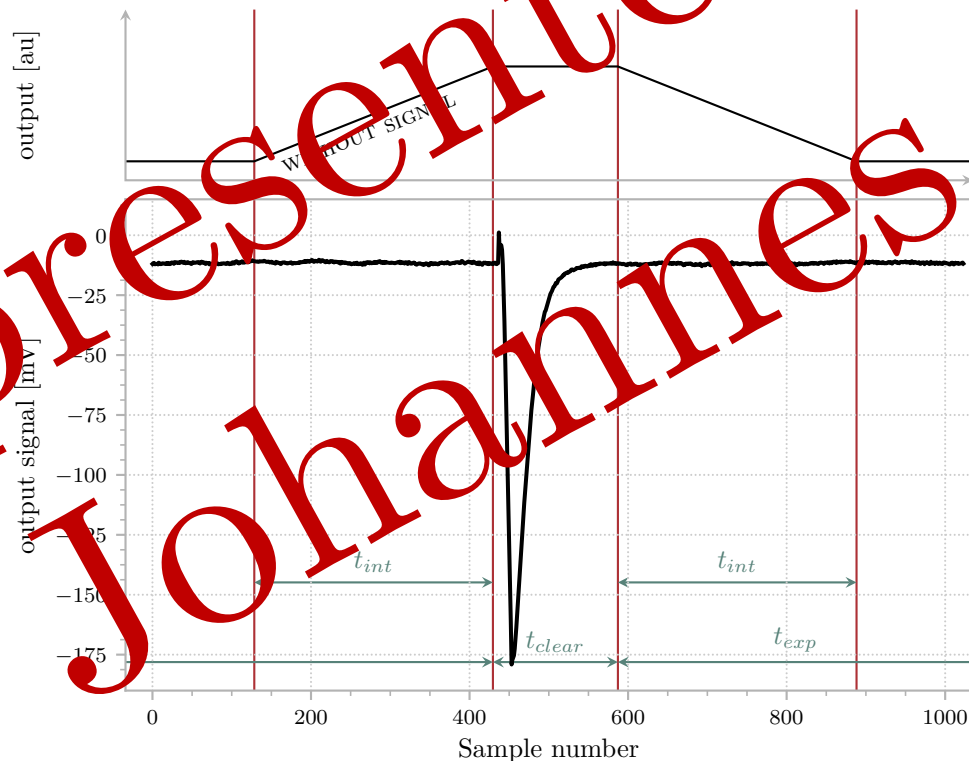


# The DePFET structure

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Two states of operation:

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- ON state – correlated double sampling:
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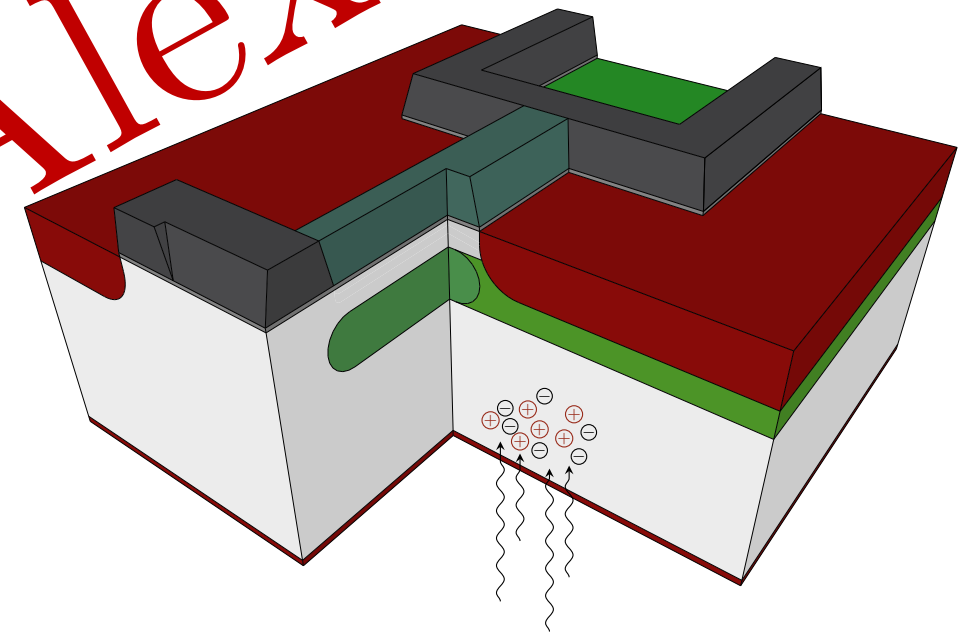
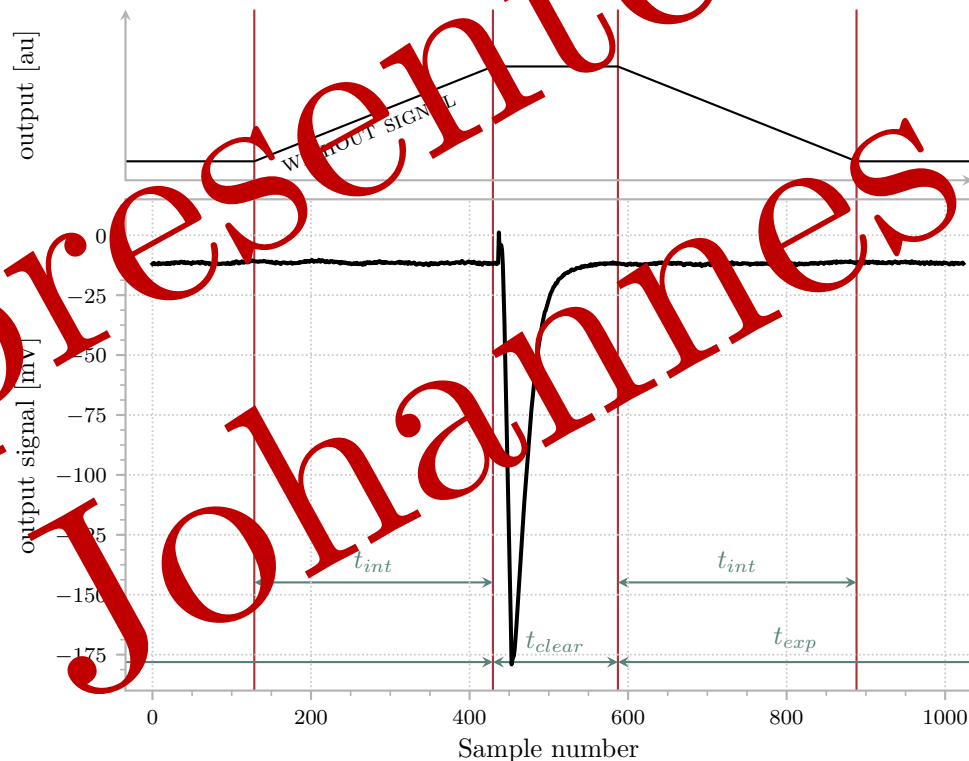
EMPTY ON STATE

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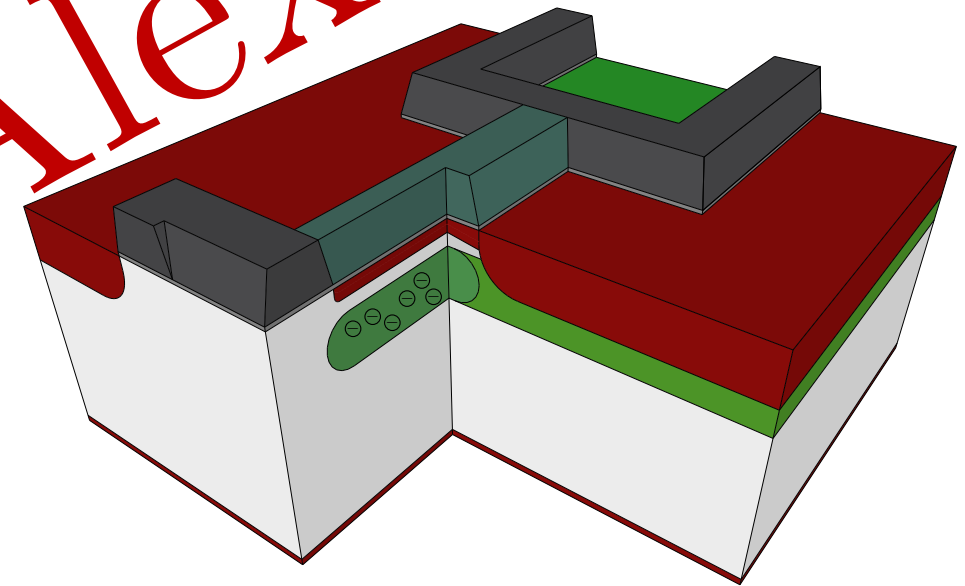
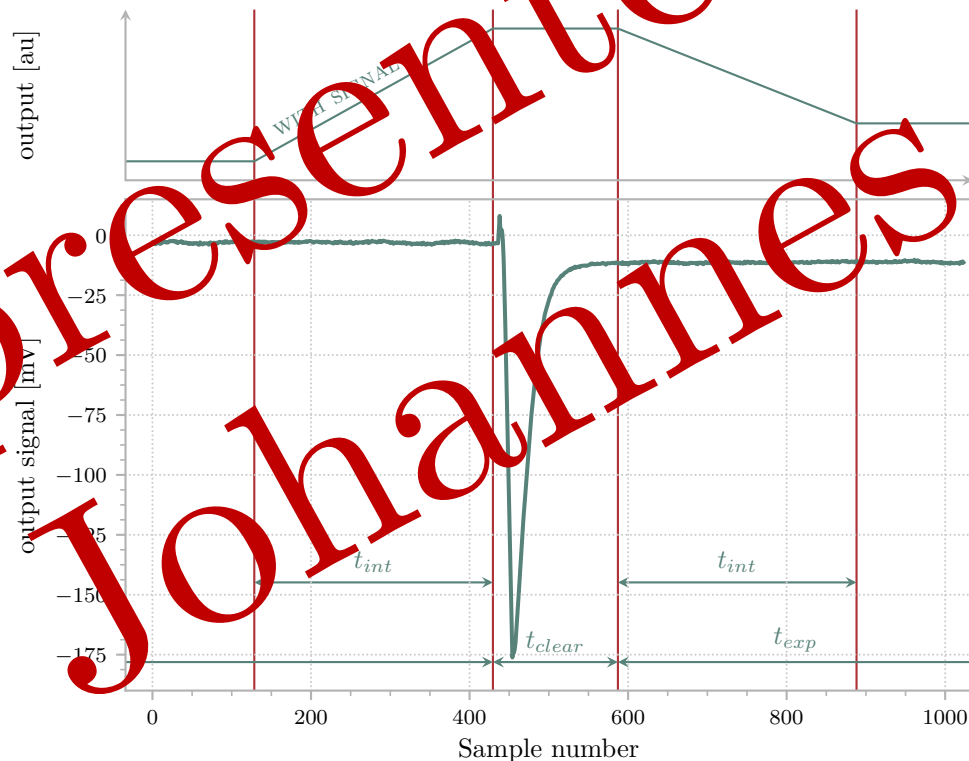
OFF STATE

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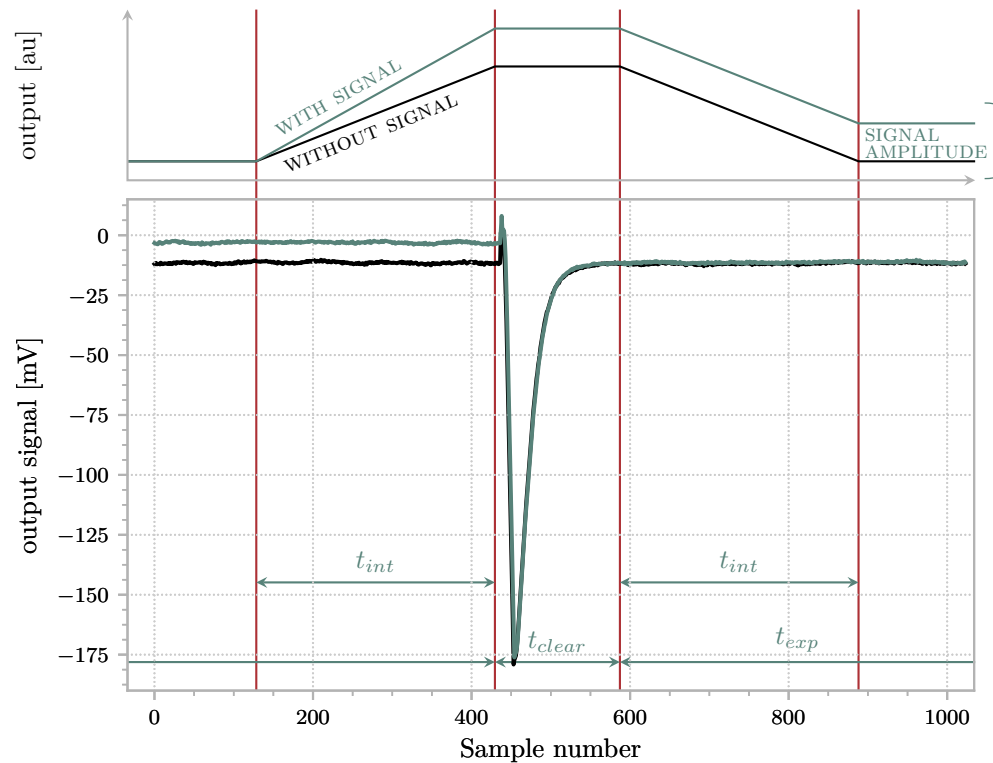
FILLED ON STATE

# The DePFET structure

and its operation principle



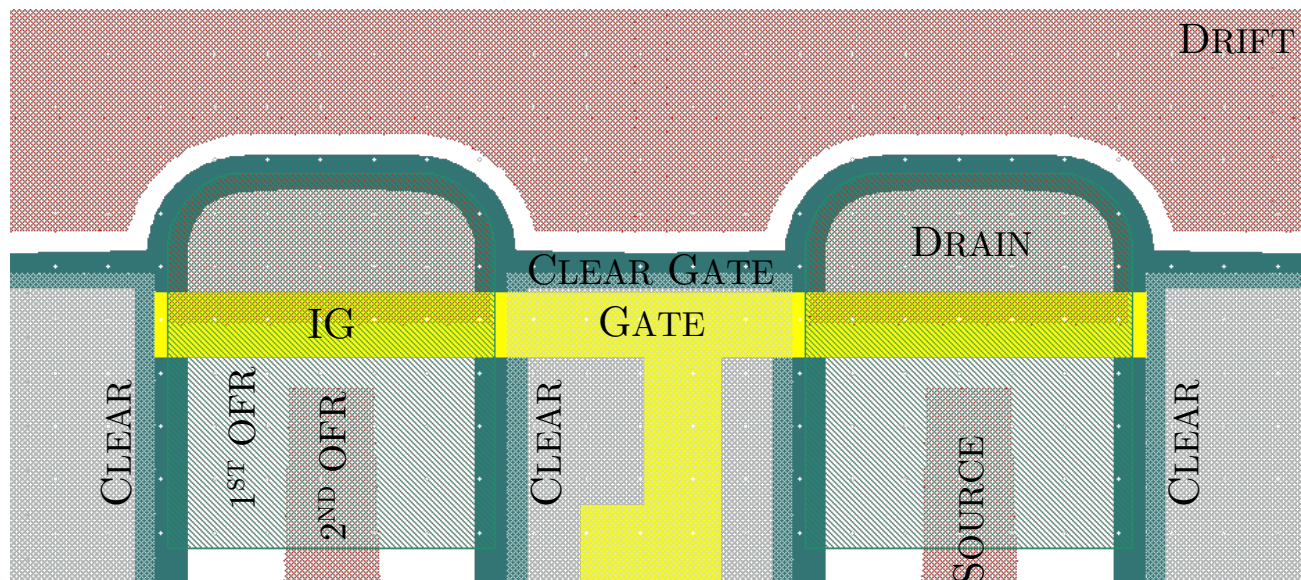
INITIAL STATE VS. FILLED STATE



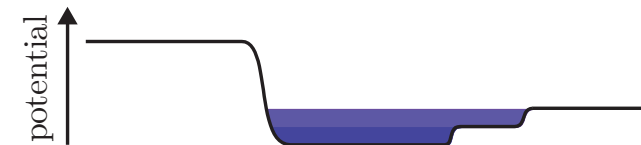
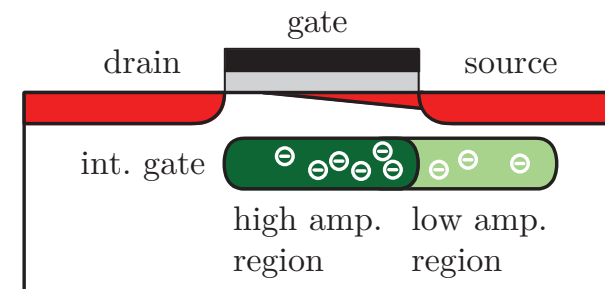
INITIAL DEPFET RESPONSE IS LINEAR  
CALIBRATION WITH A KNOWN RADIOACTIVE SOURCE



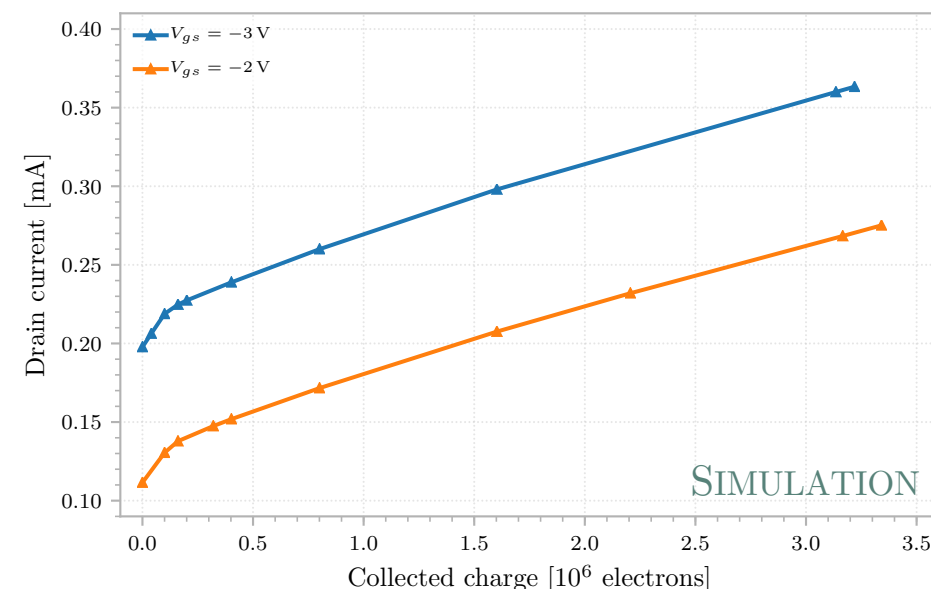
# The EDET DePFET structure and its operation principle



INTERNAL GATE is under the GATE  
 1<sup>ST</sup> OVERFLOW REGION is around the SOURCE  
 2<sup>ND</sup> OVERFLOW REGION is under the SOURCE



Response curve  $V_{ds} = -5\text{ V}$

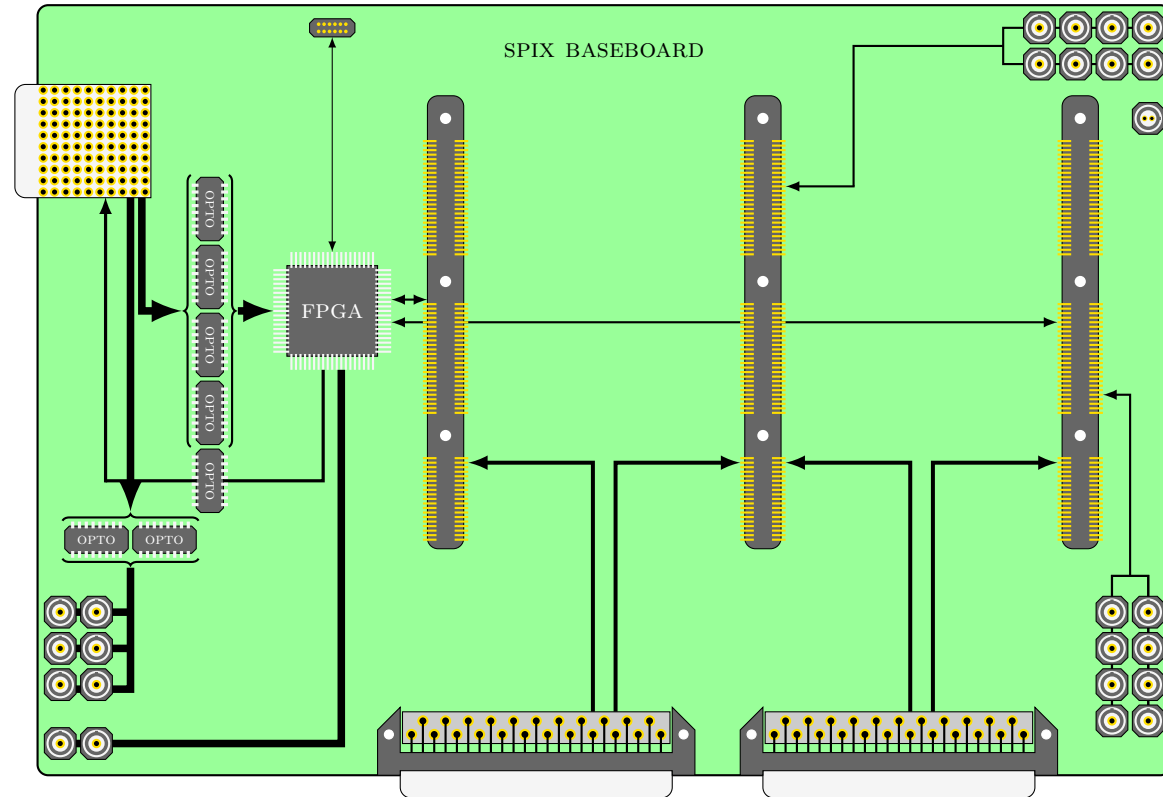


SIMULATION

# Measurement setup

operating principle

Design concept:  
MODULARITY

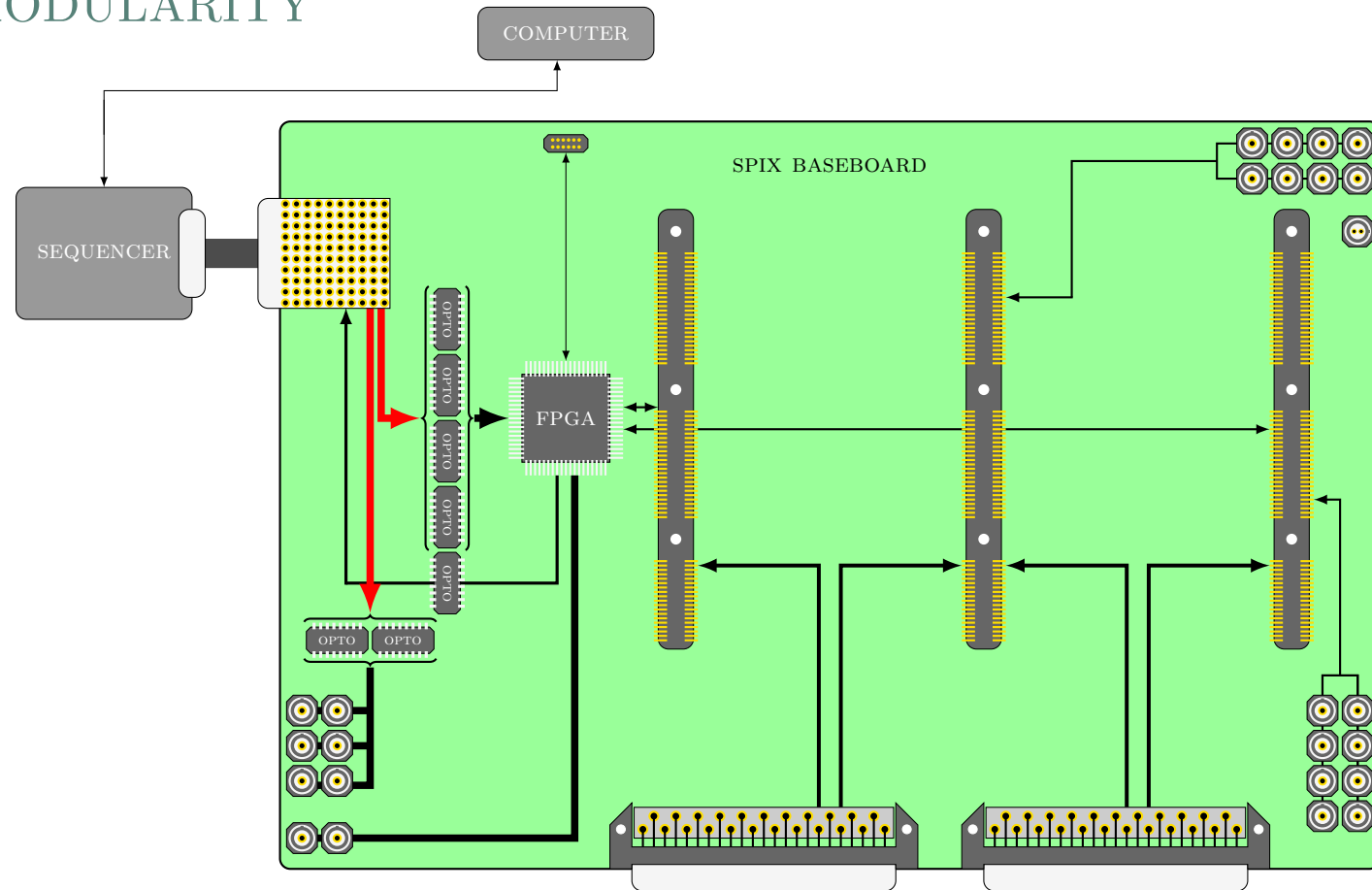


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operating principle

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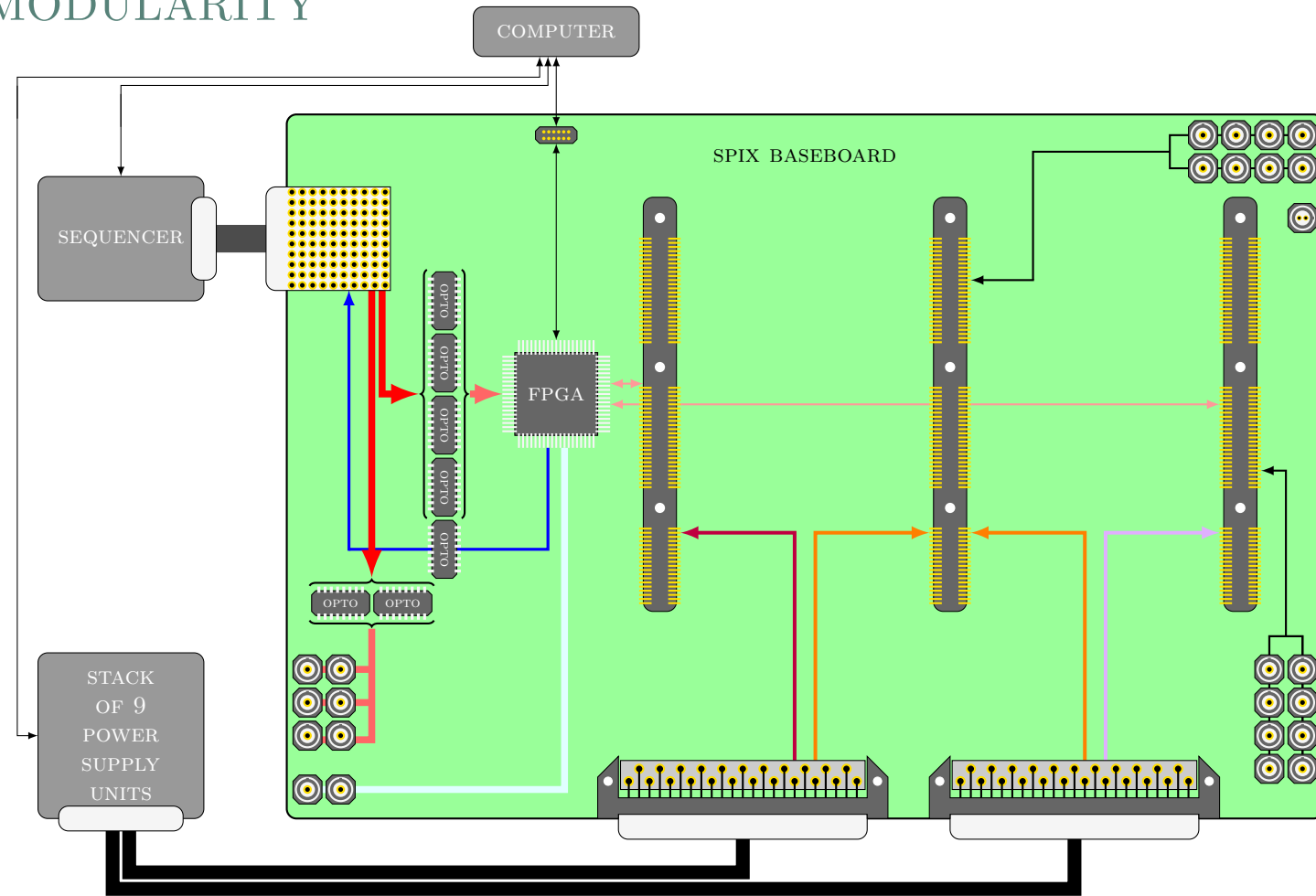


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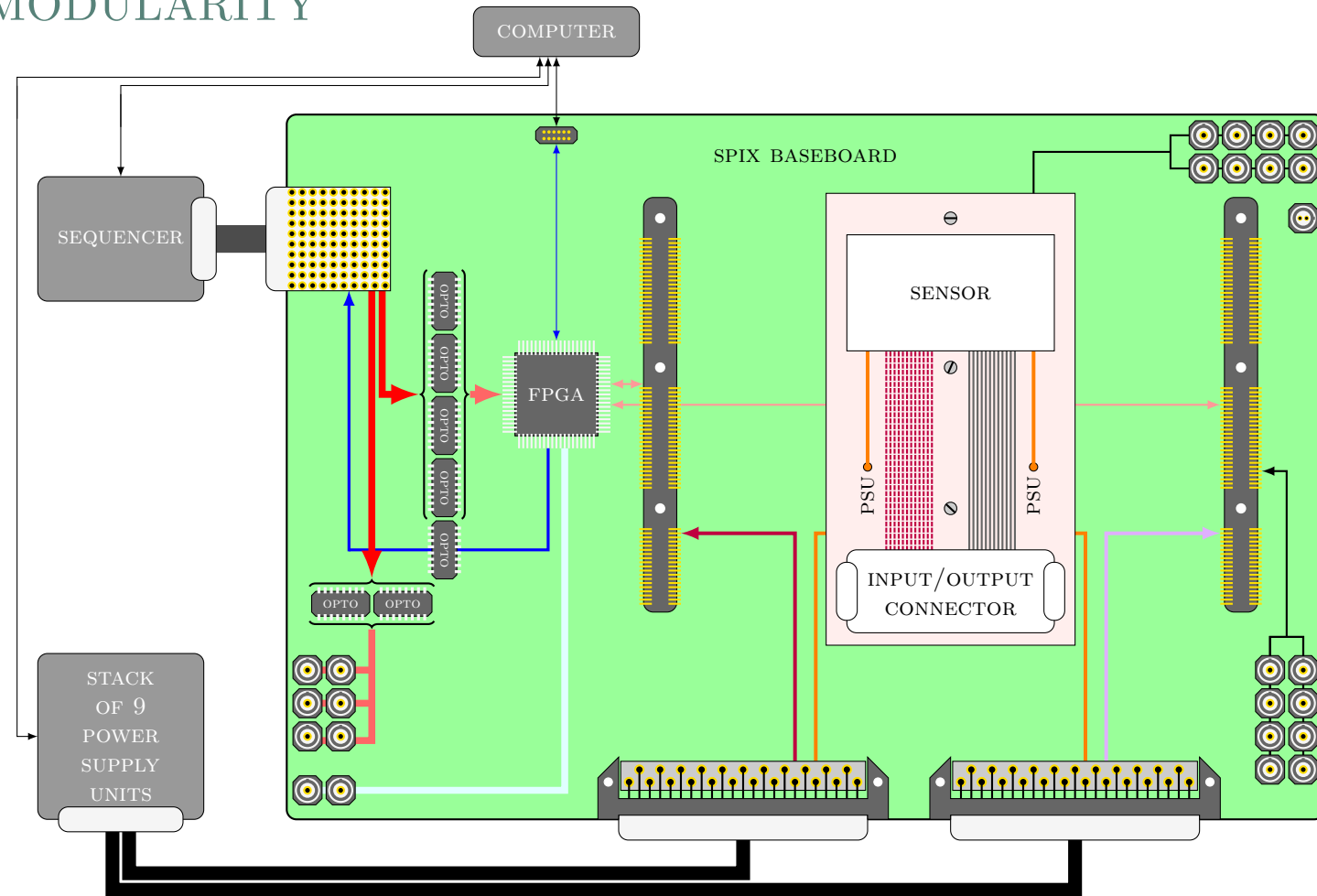


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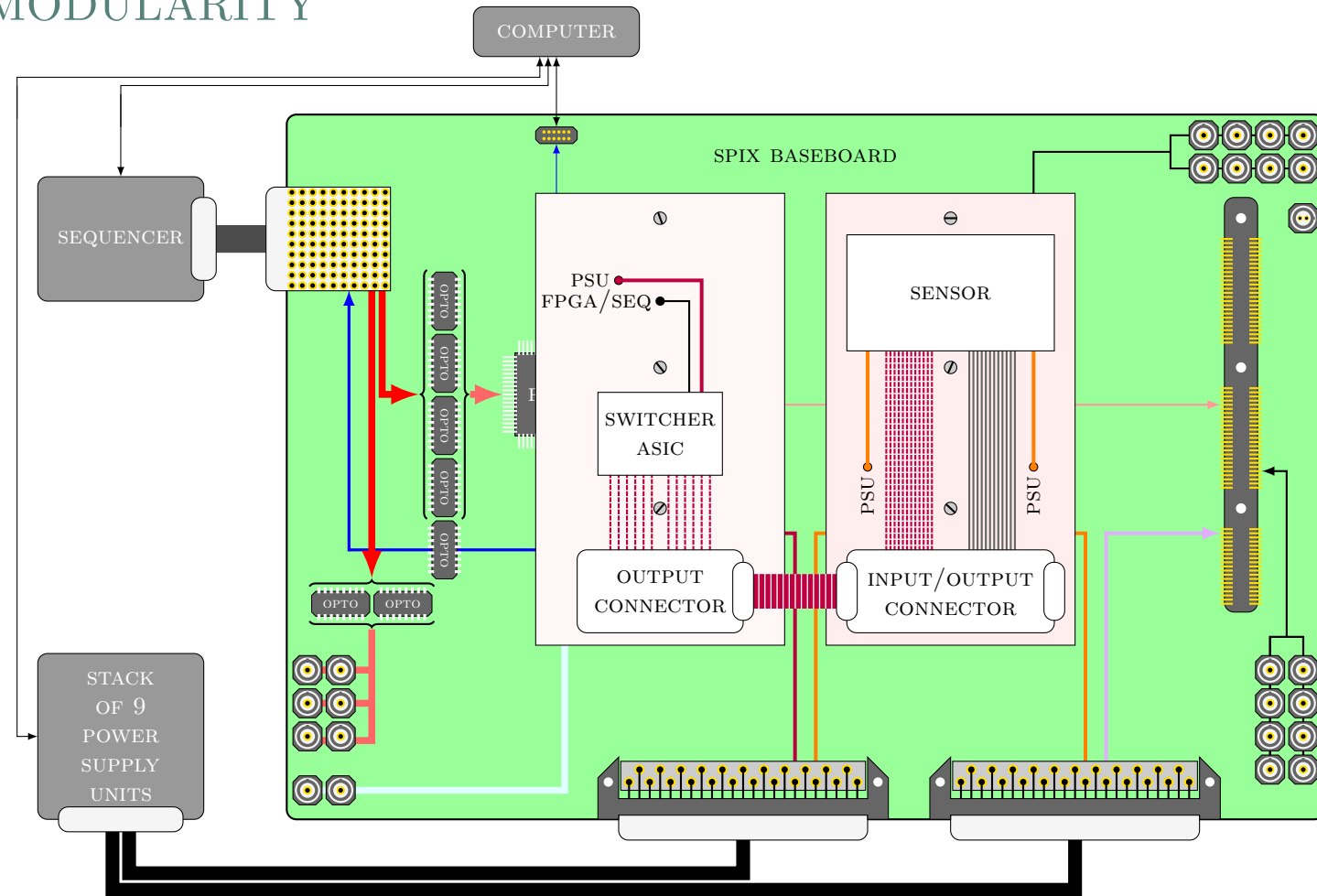


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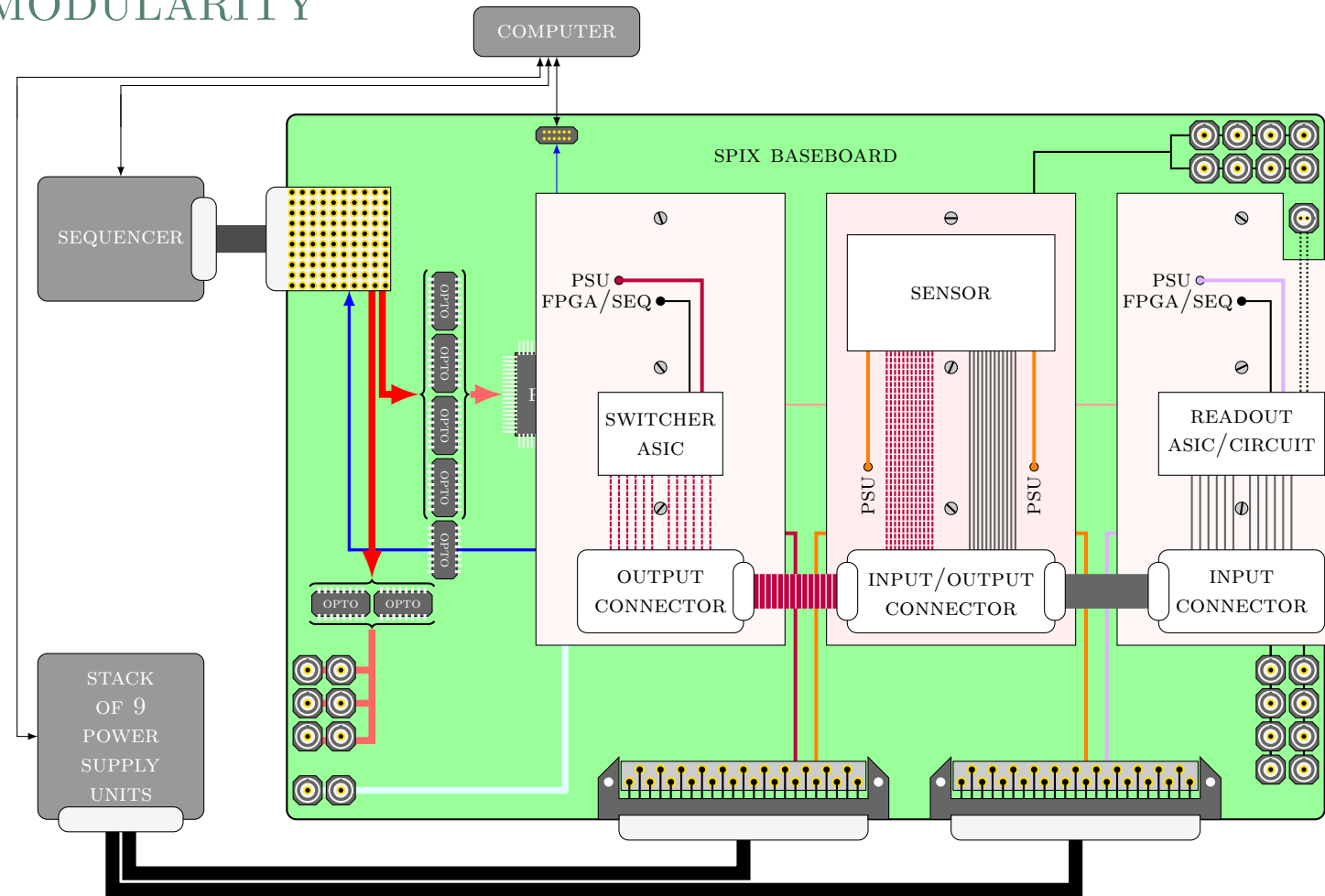


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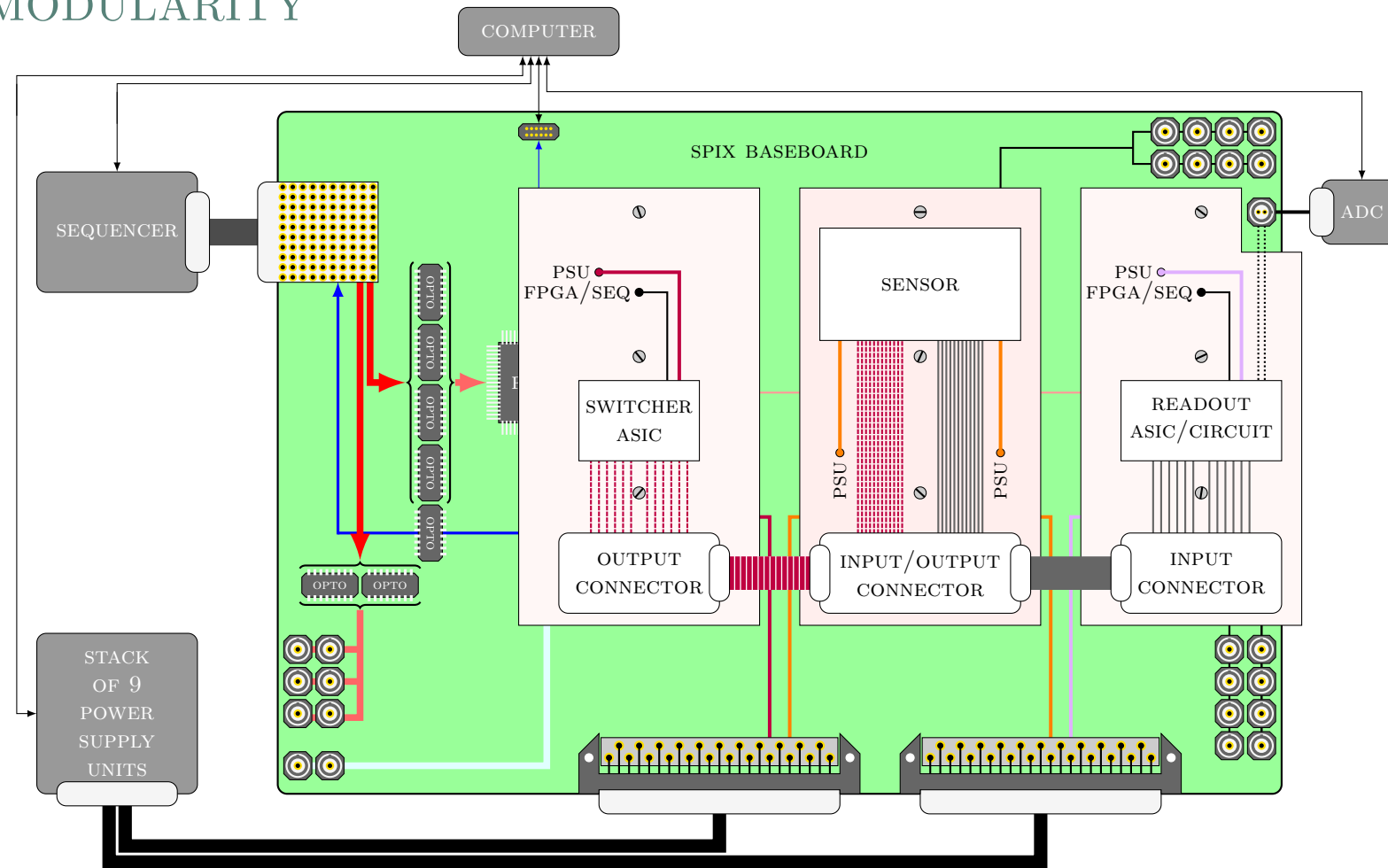


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operating principle

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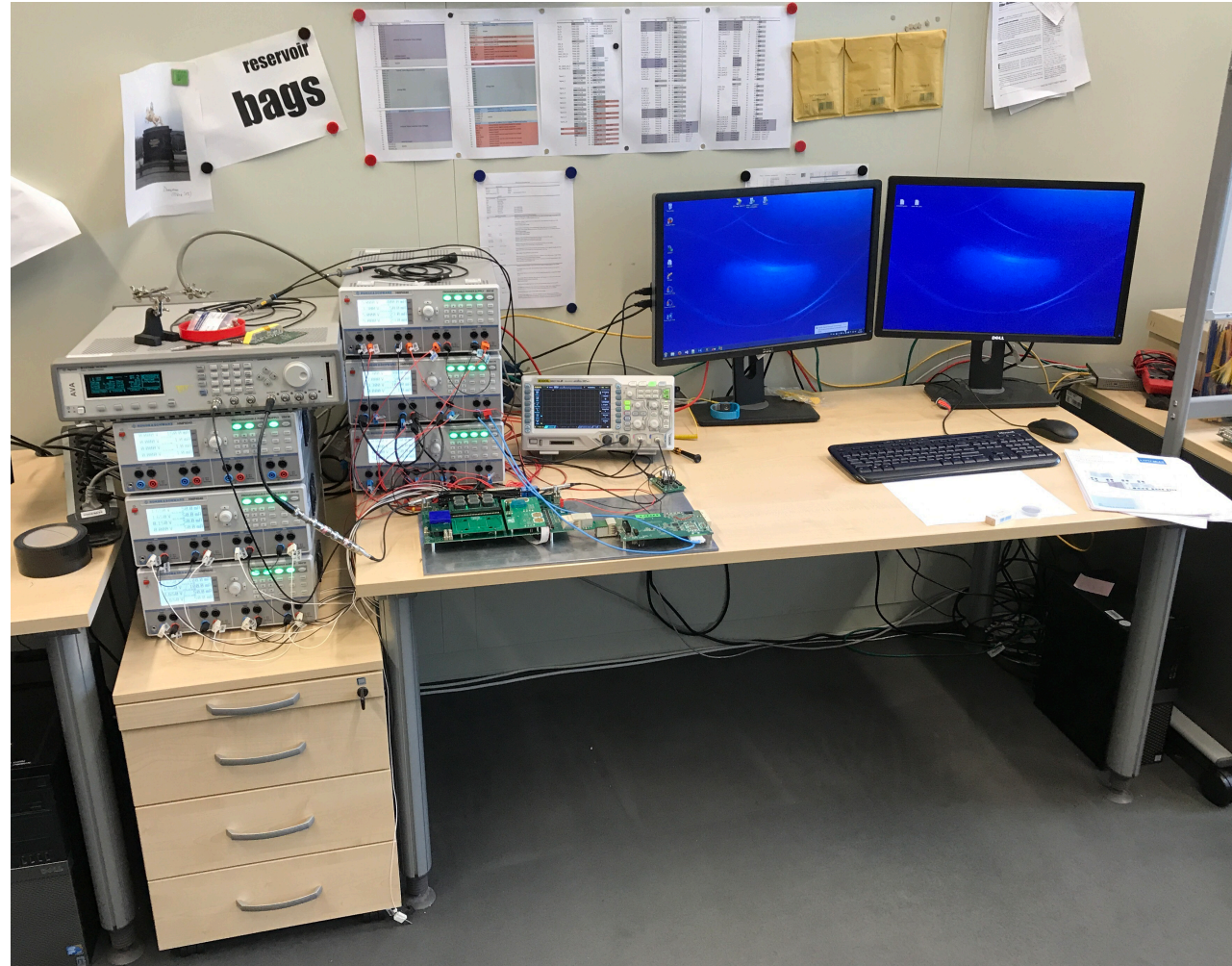


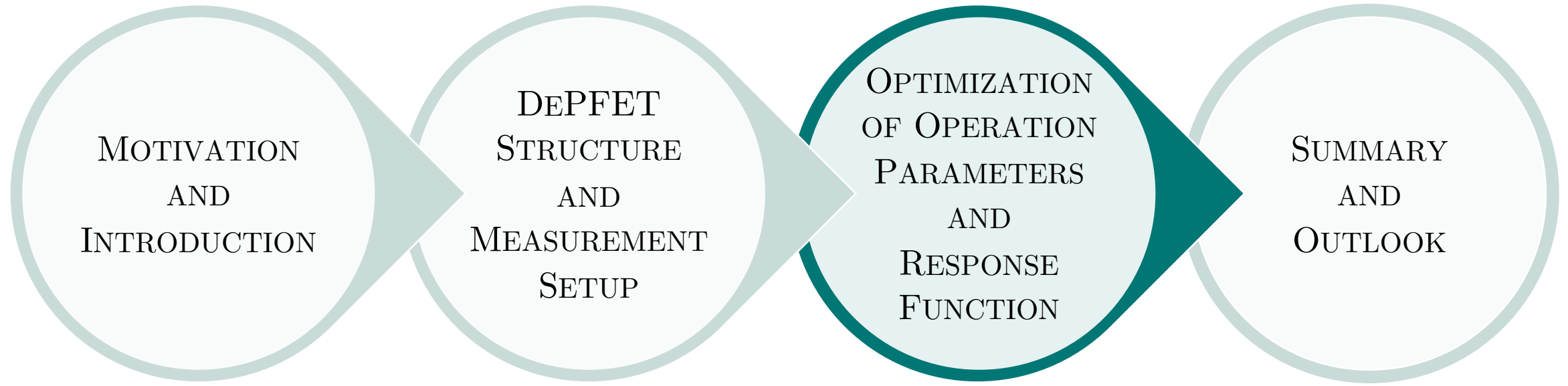


# Single PIXle setup

actual setup

Design concept:  
MODULARITY



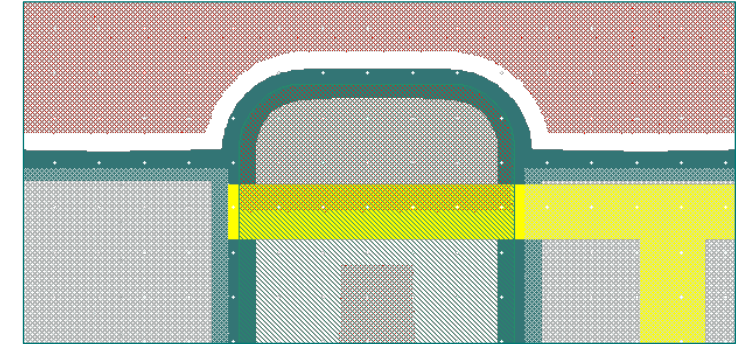


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

Clear Gate and Clear low voltage influence

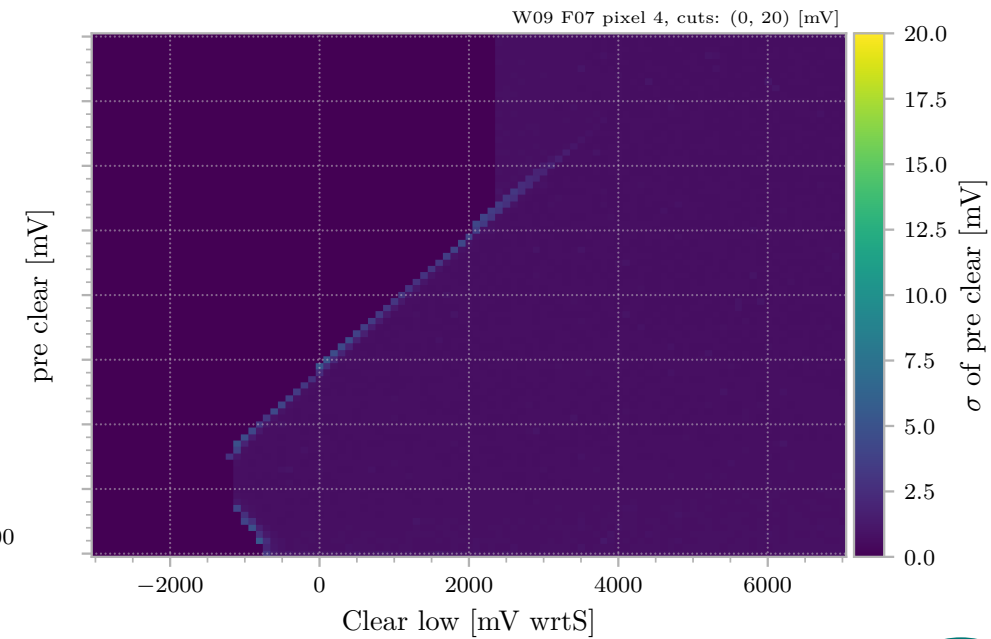
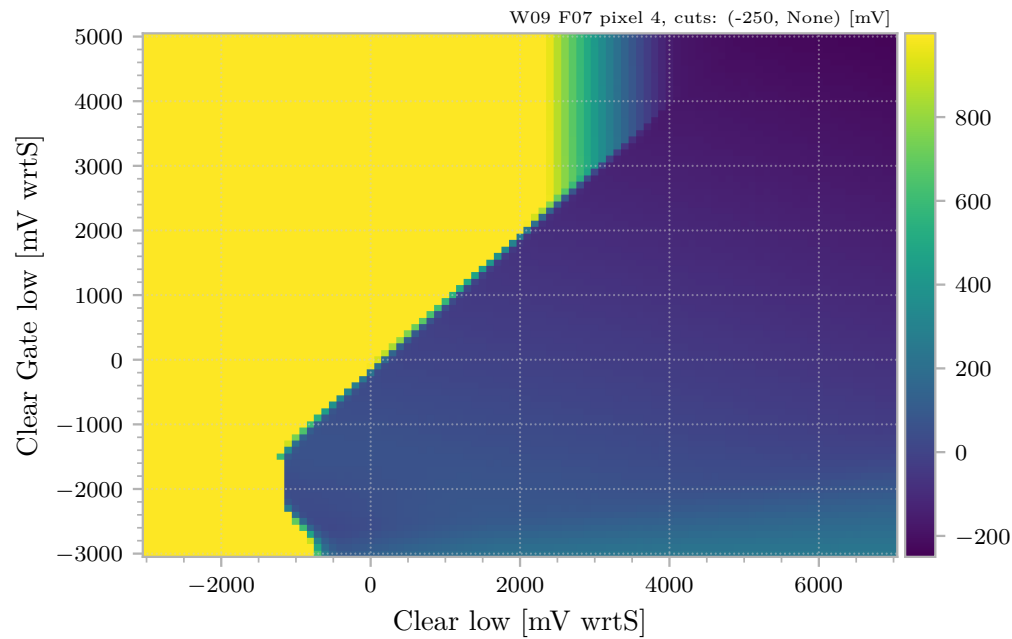
- back-emission of  $e^-$  from clear contact,
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- charge loss to clear contact.



W09 F07

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Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
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Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

NO EXTERNAL ILLUMINATION; OBSERVING ONLY THE INITIAL STATE

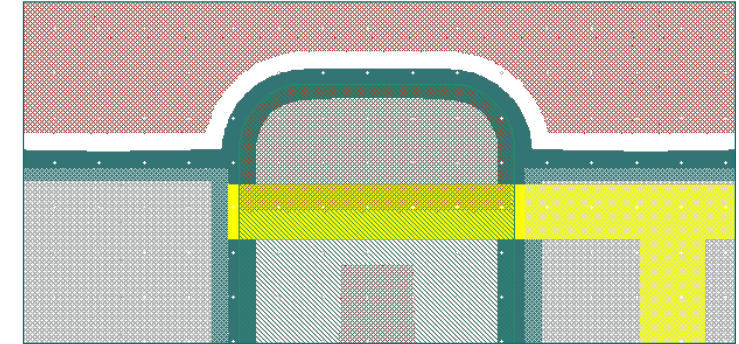


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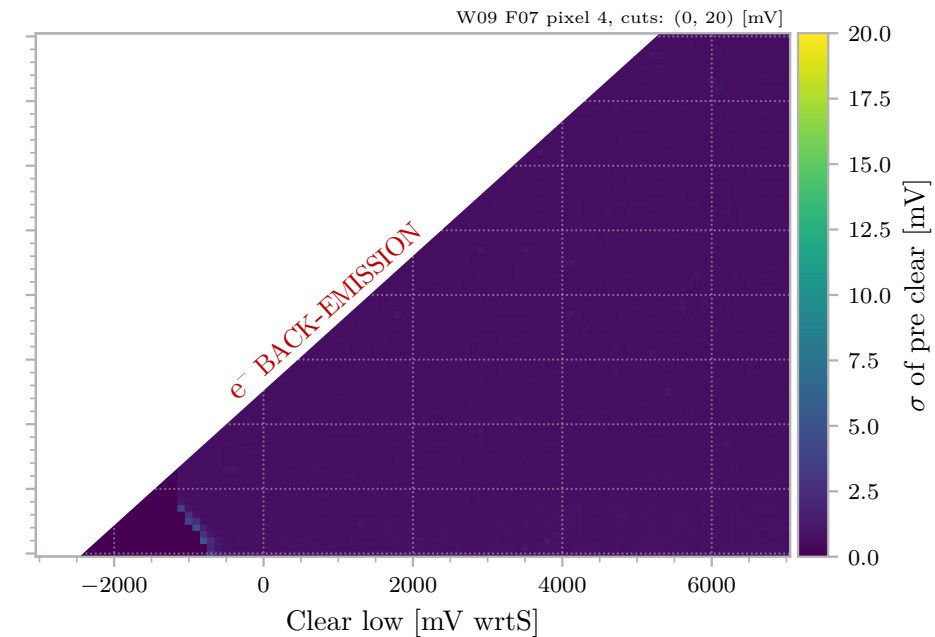
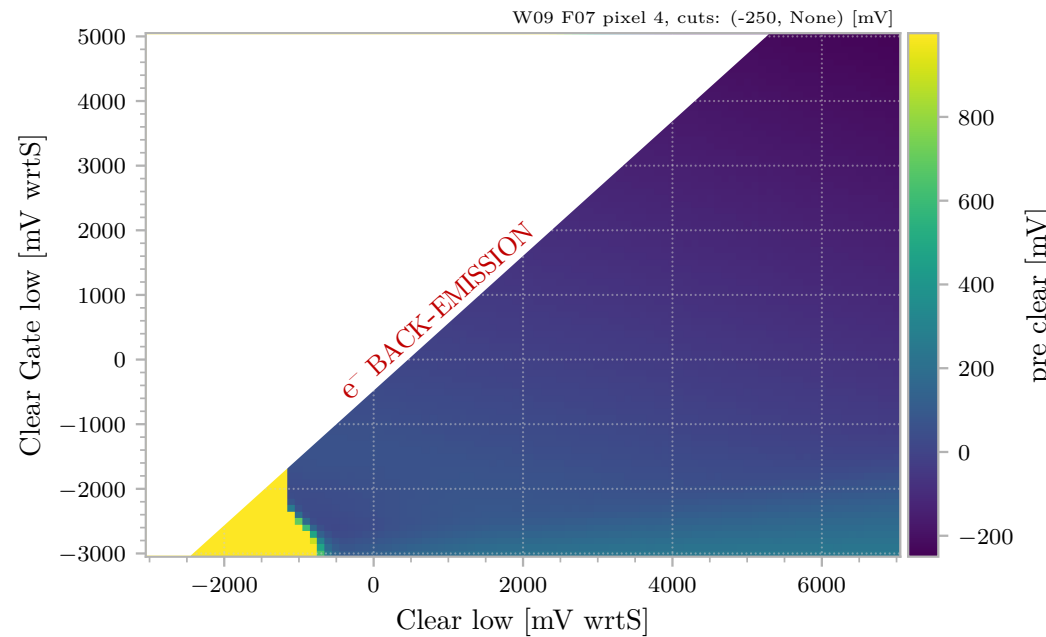
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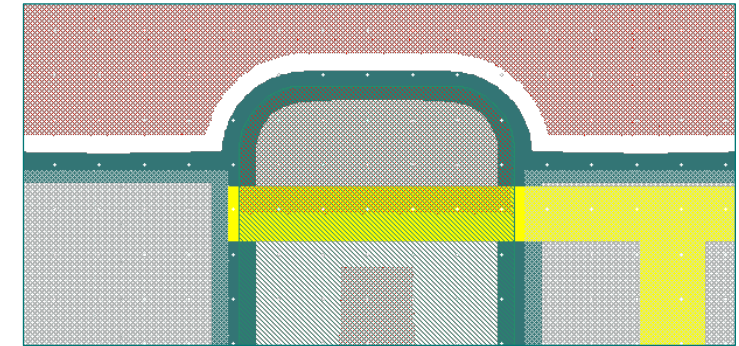


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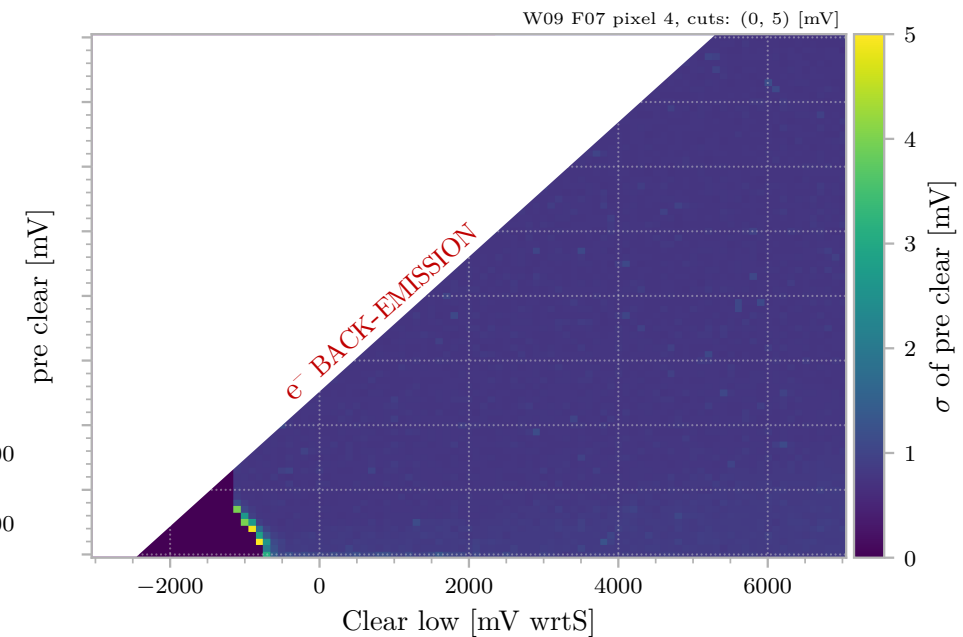
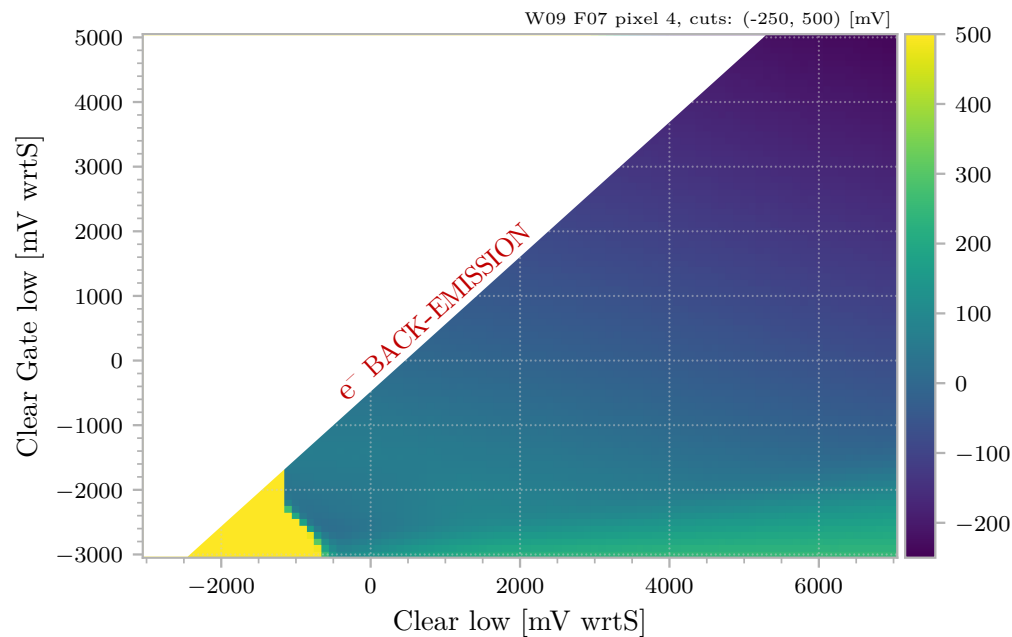
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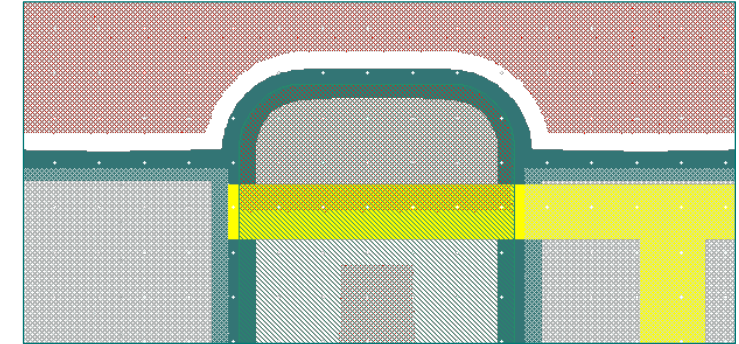


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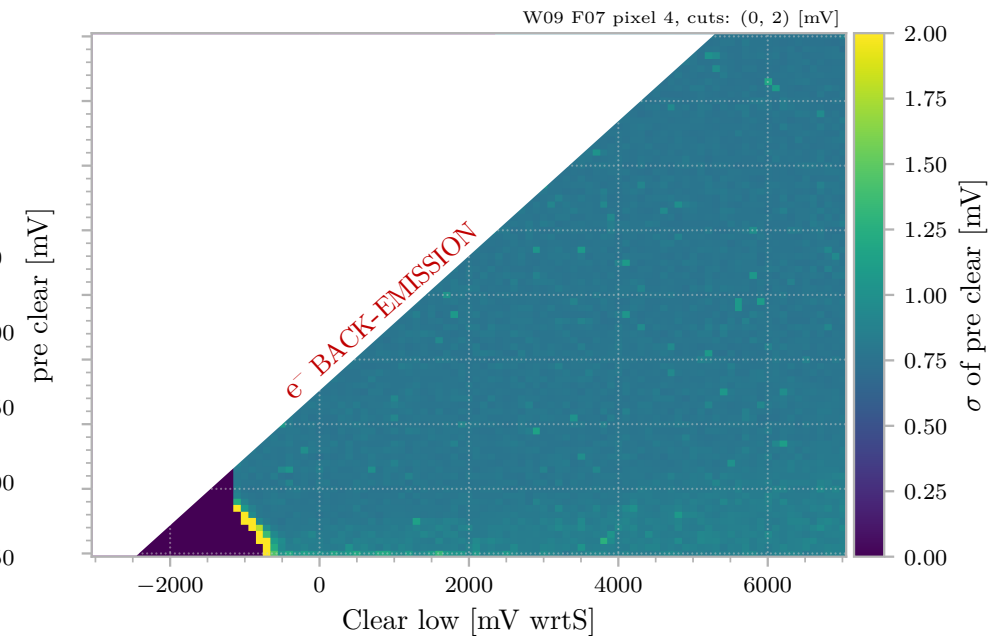
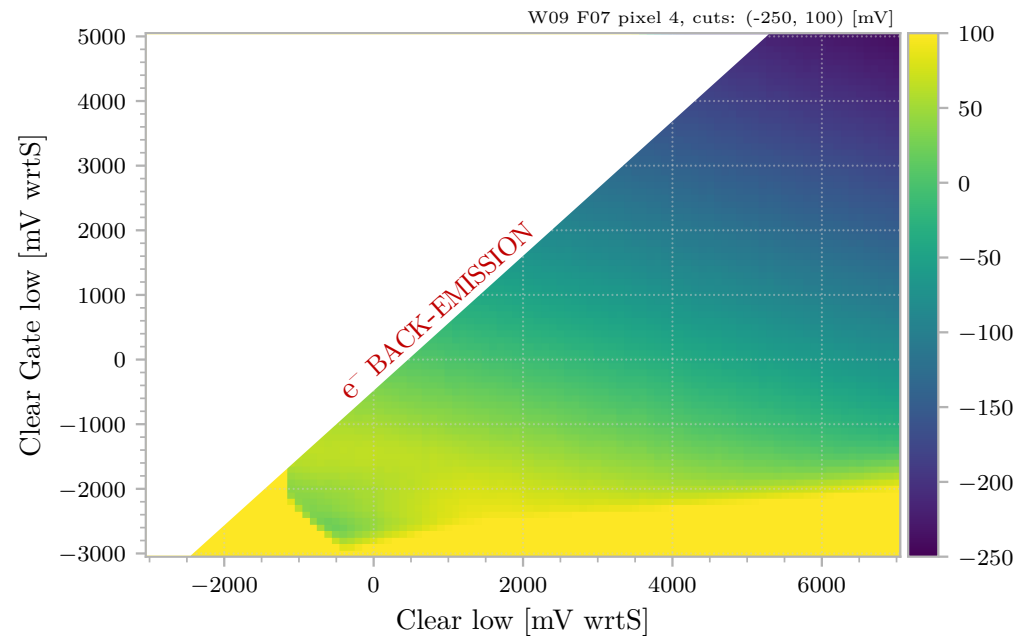
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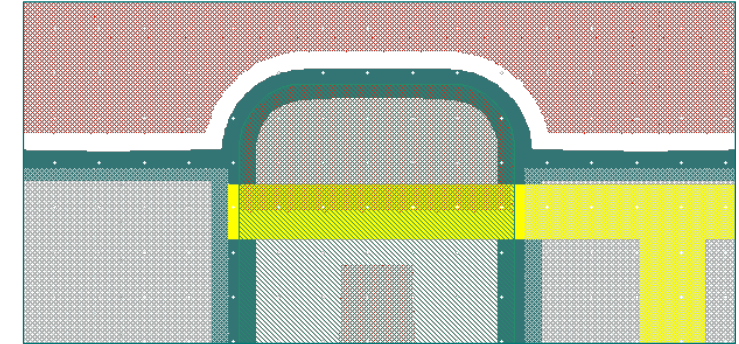


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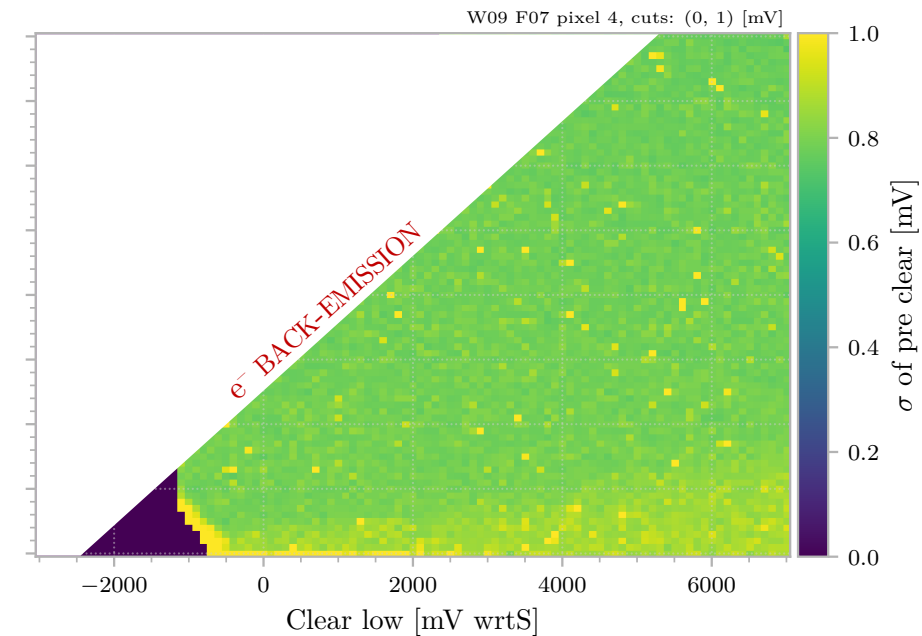
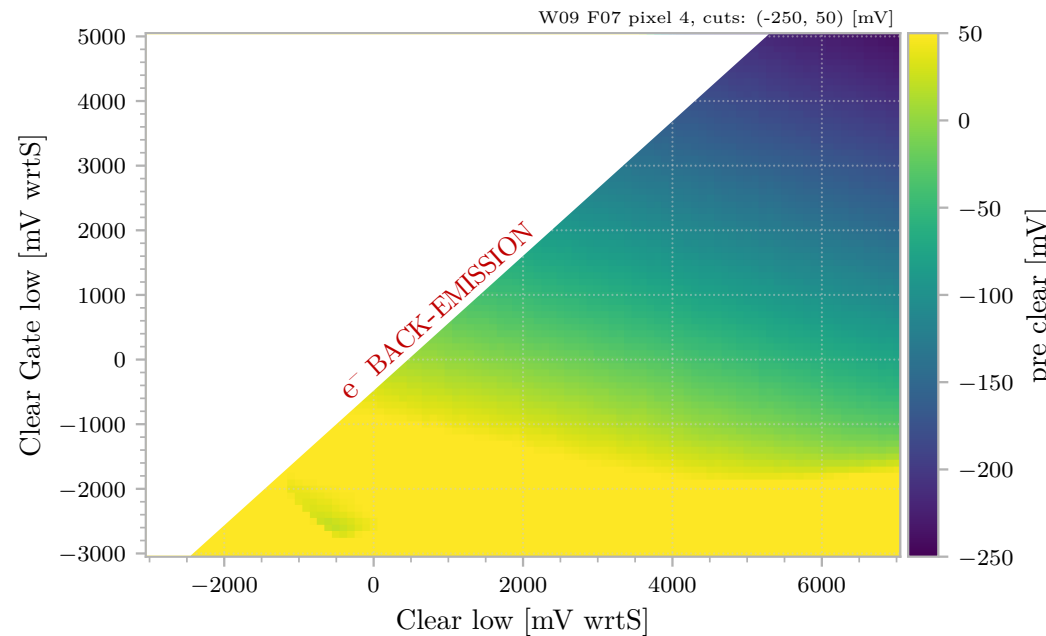
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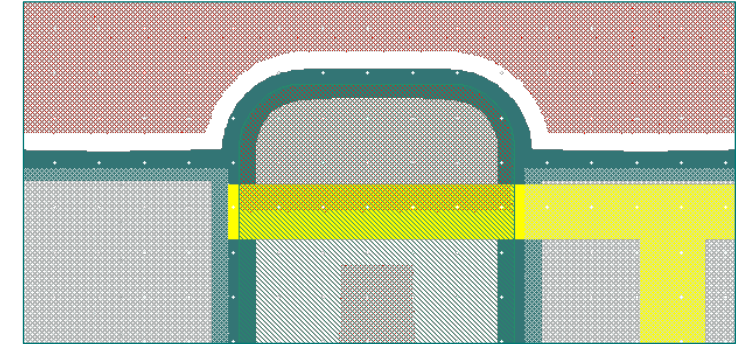


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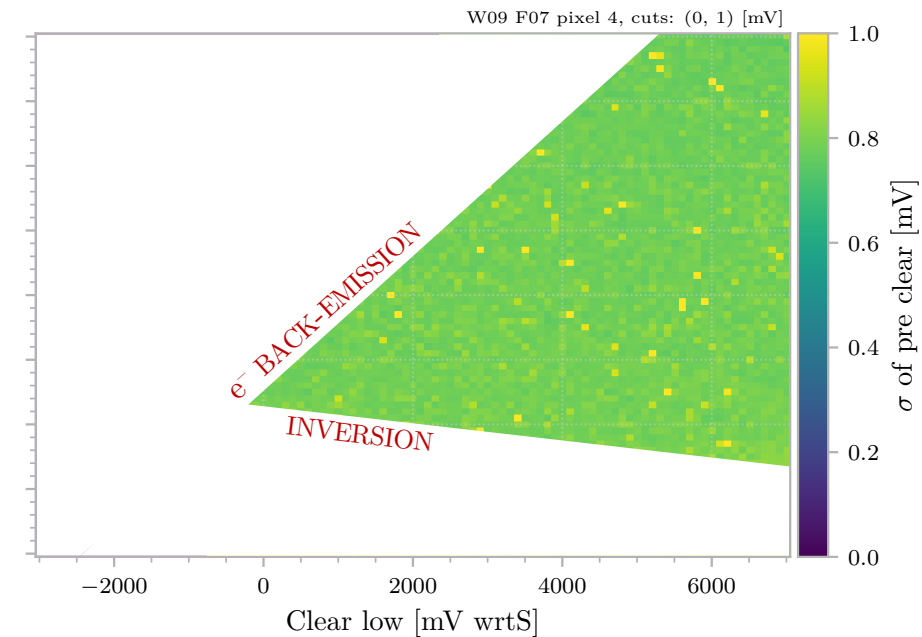
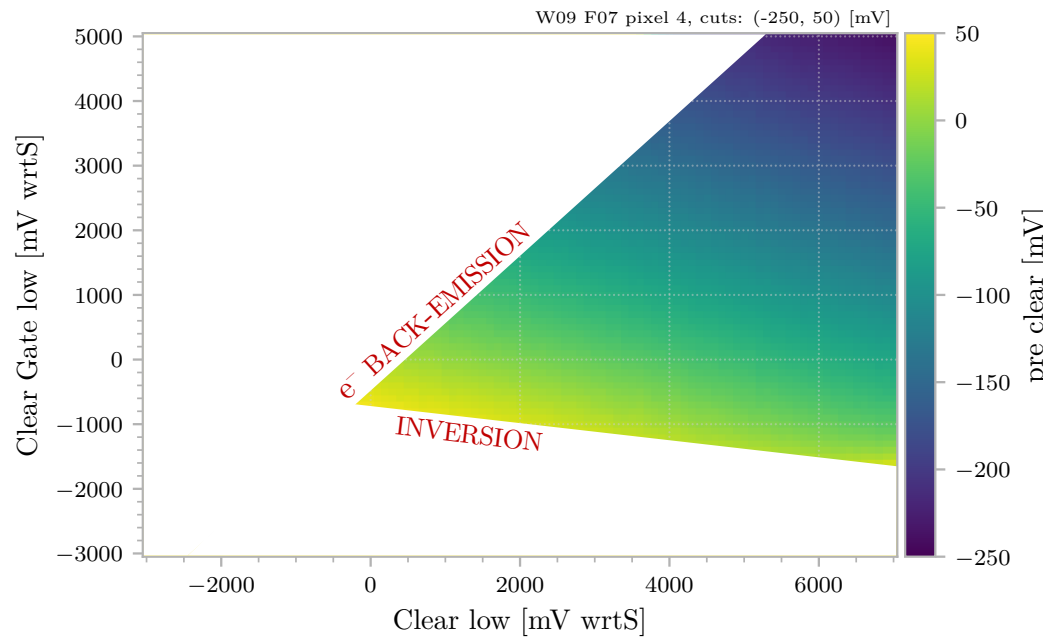
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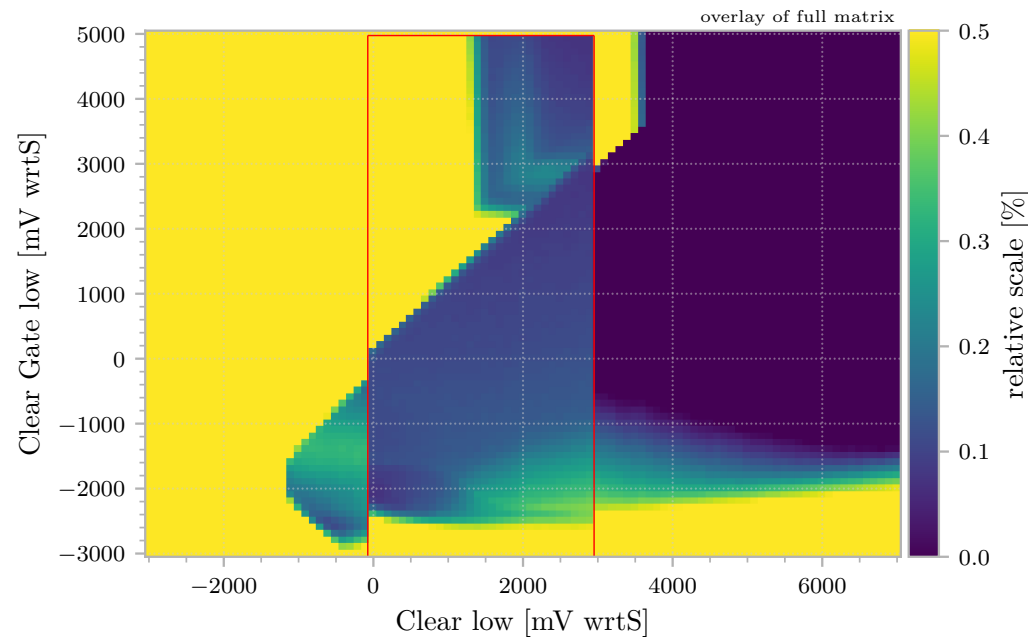
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NO EXTERNAL ILLUMINATION; OBSERVING ONLY THE INITIAL STATE



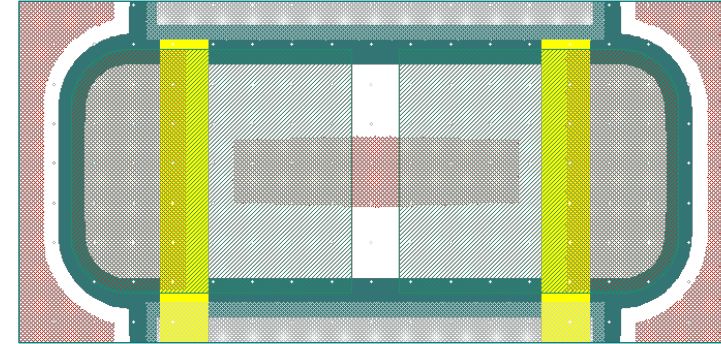
OVERLAY (RED BOX) OF AN IDENTICAL MEASUREMENT DONE WITH THE SMALLER VERSION OF THE FINAL CAMERA SETUP.

# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

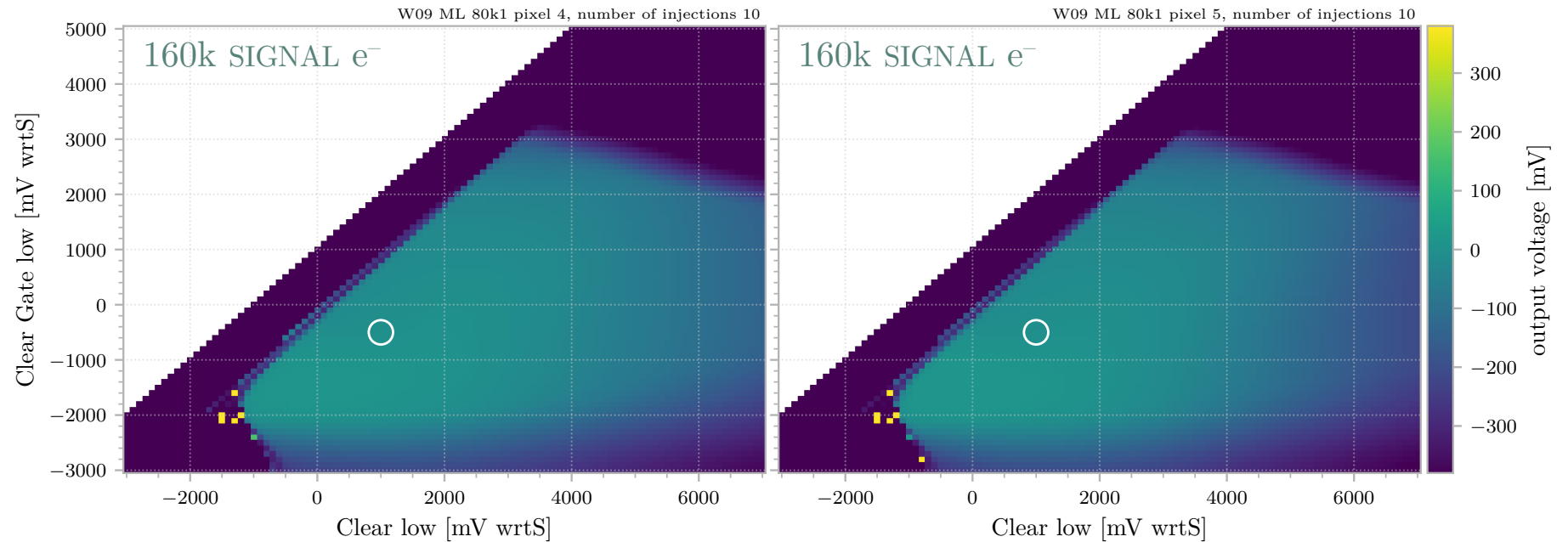
Clear Gate and Clear low voltage influence

- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

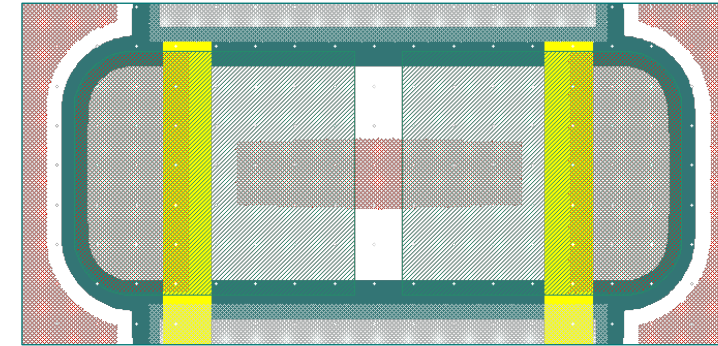


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

Clear Gate and Clear low voltage influence

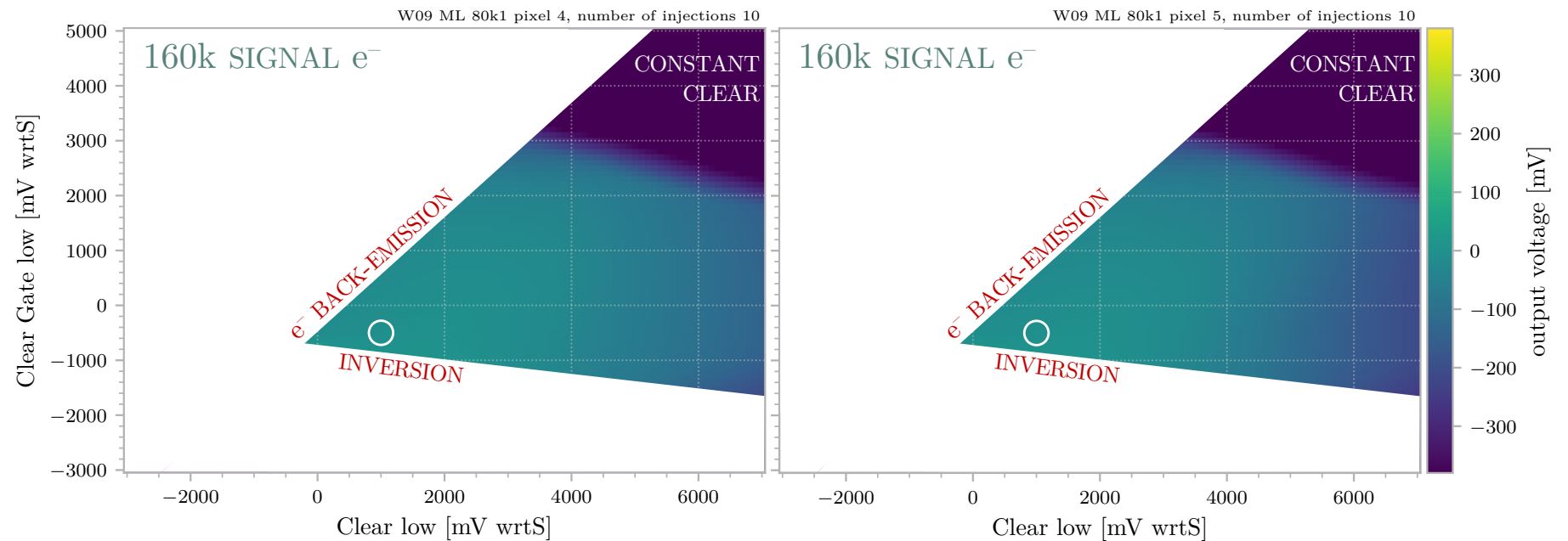
- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

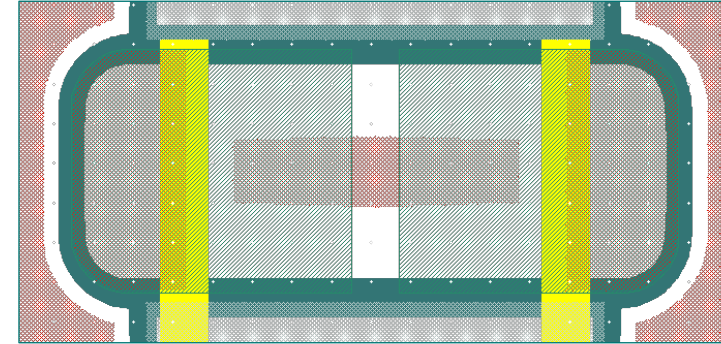


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

Clear Gate and Clear low voltage influence

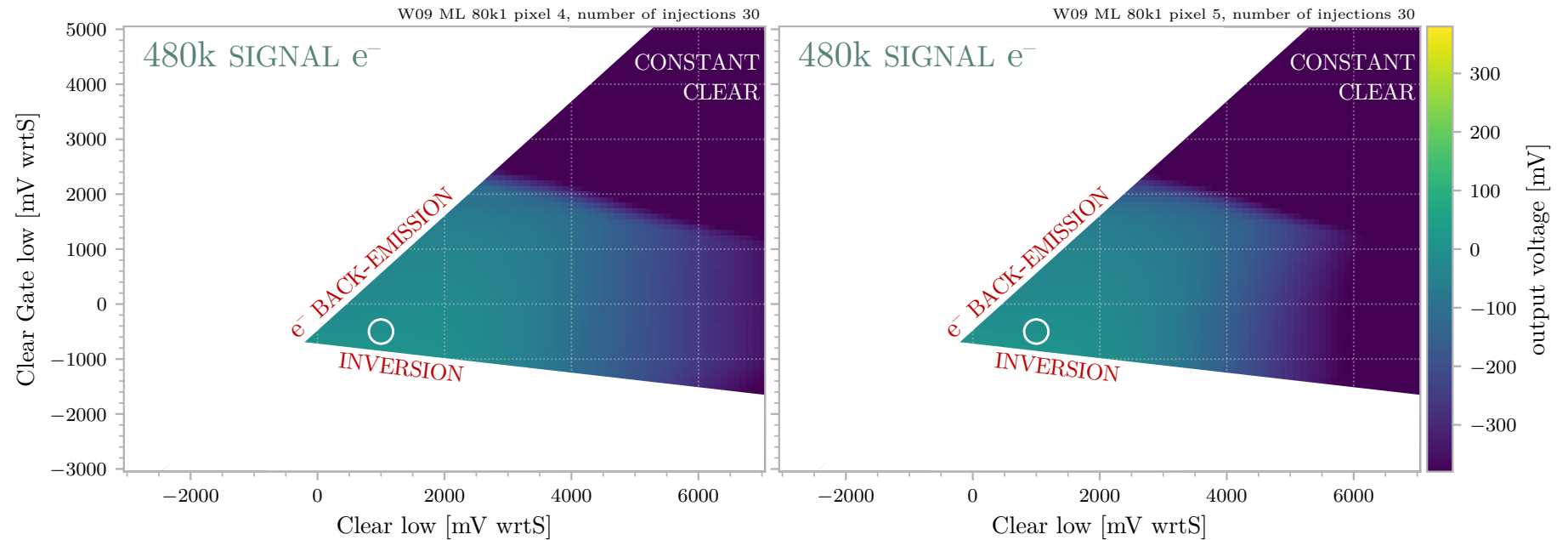
- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

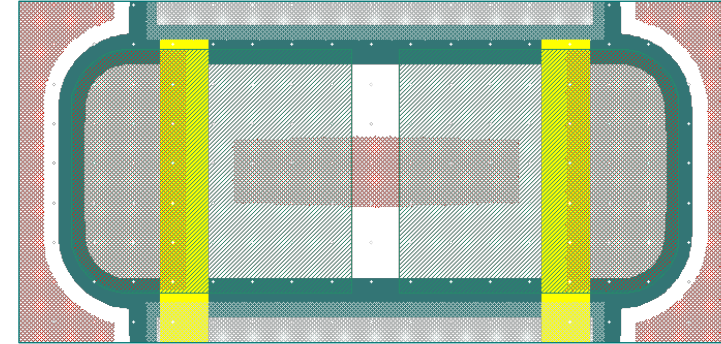


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

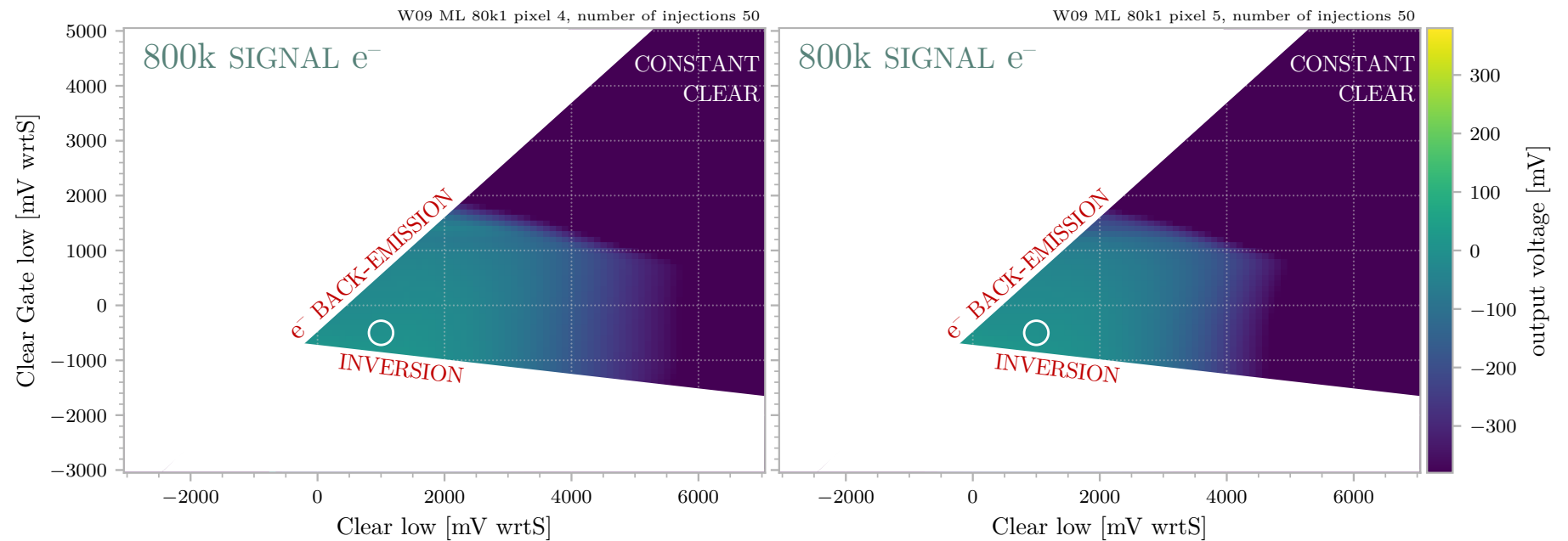
Clear Gate and Clear low voltage influence

- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

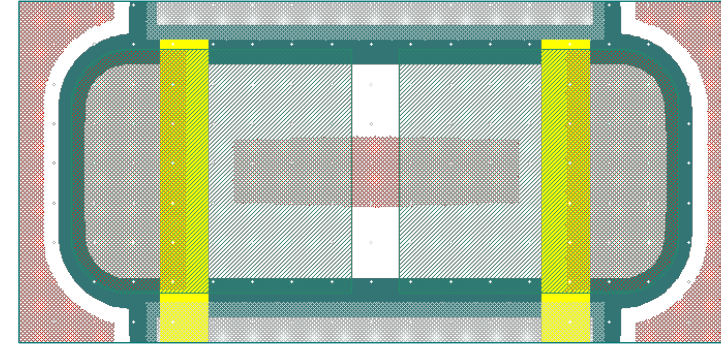


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

Clear Gate and Clear low voltage influence

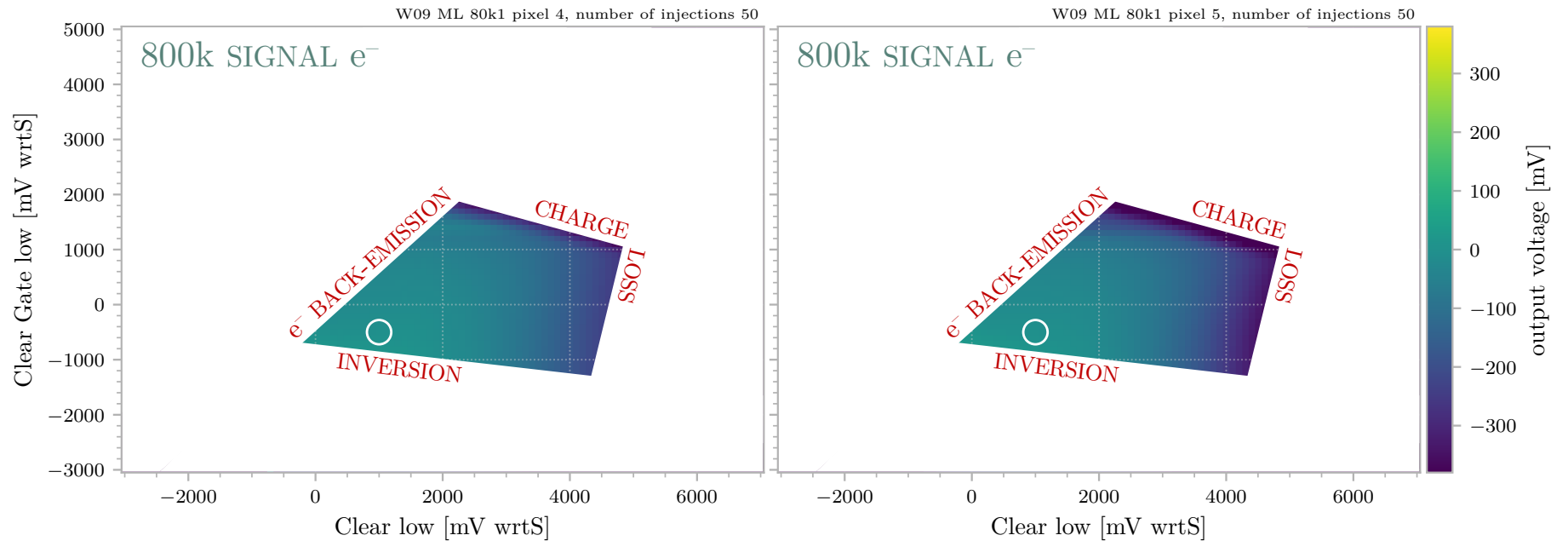
- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
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Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

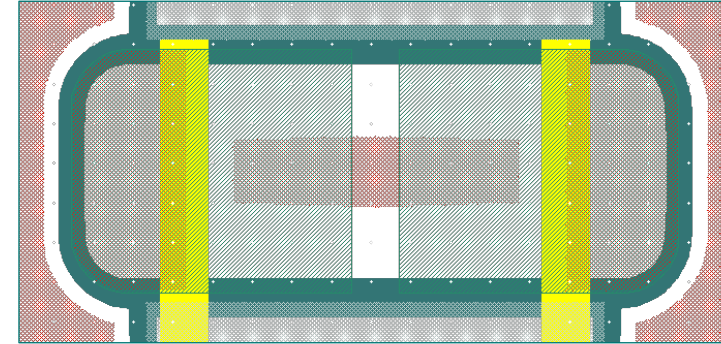


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

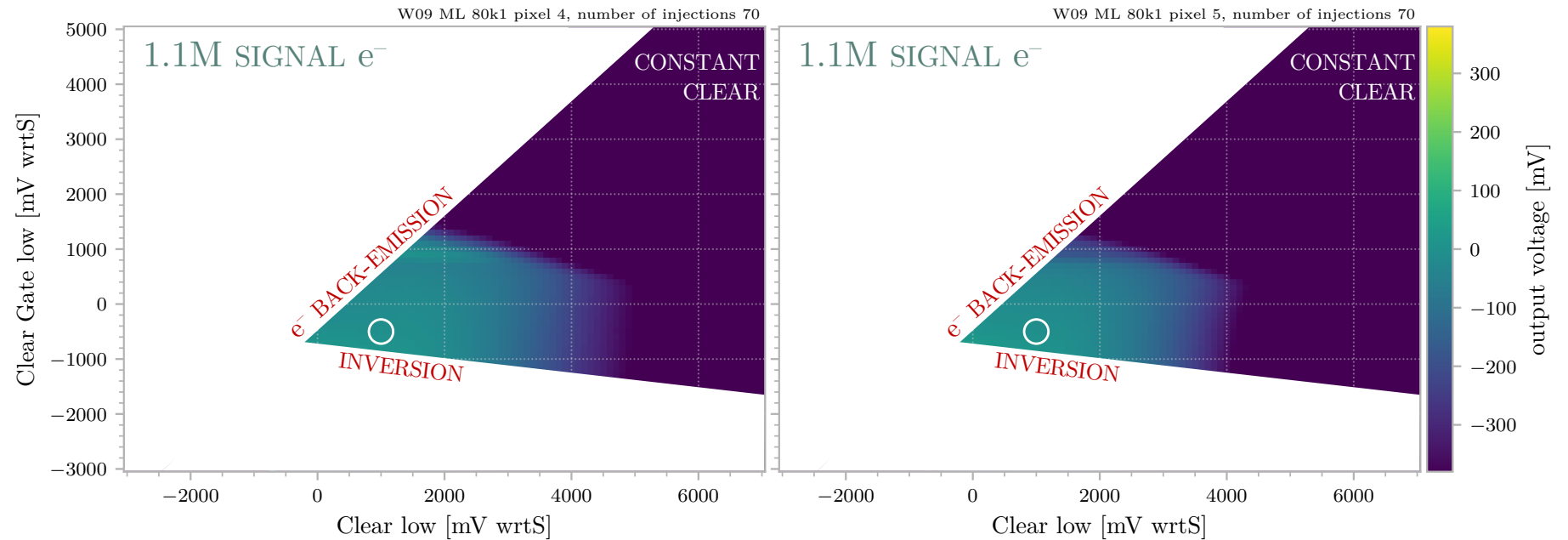
Clear Gate and Clear low voltage influence

- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$

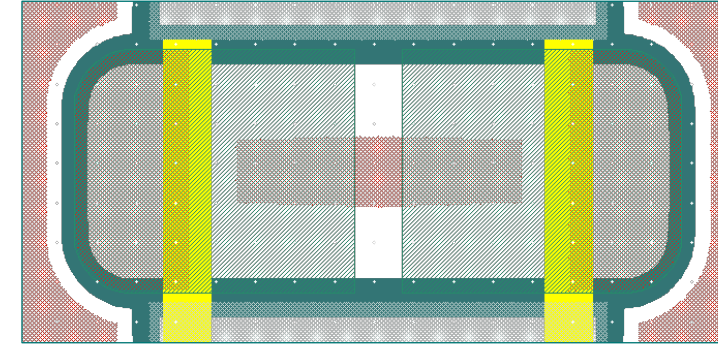


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

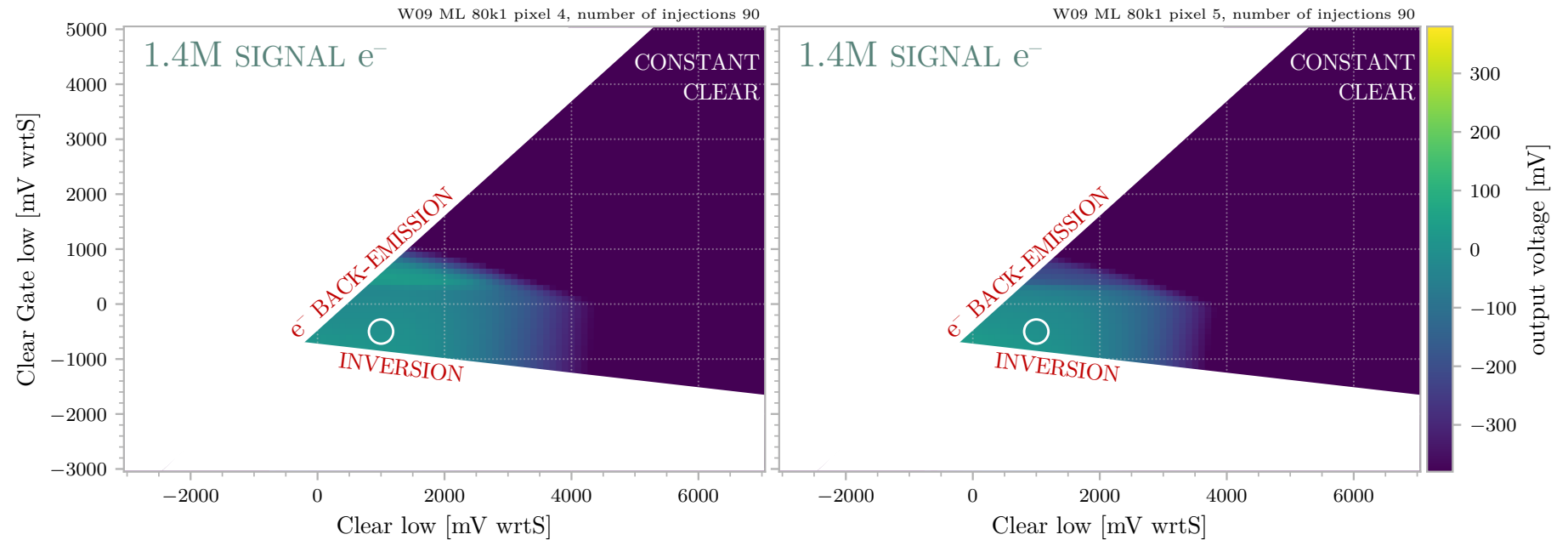
Clear Gate and Clear low voltage influence

- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$



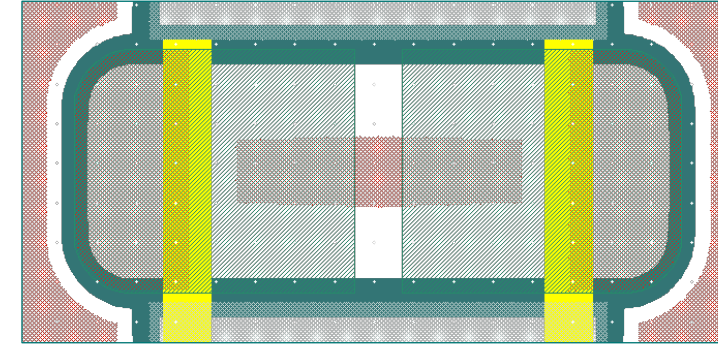


# Measurements – operation window

on depleted 50  $\mu\text{m}$  thick EDET structures

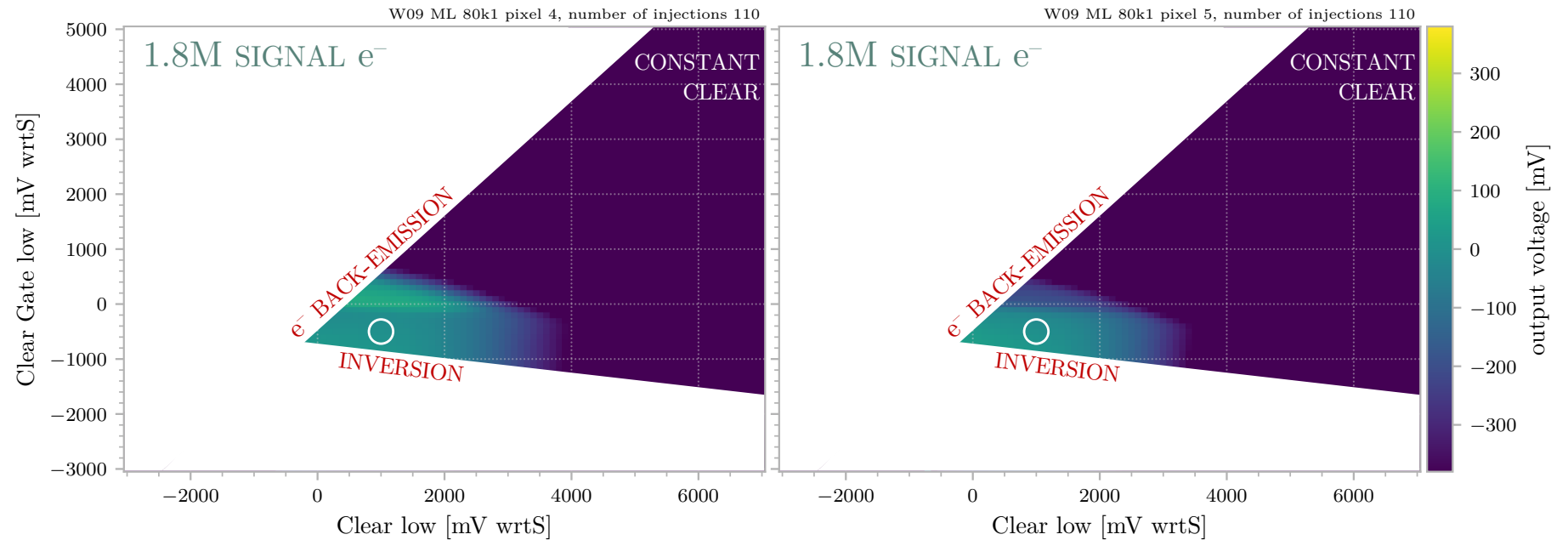
Clear Gate and Clear low voltage influence

- back-emission of  $e^-$  from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO  $\sim 10 \times {}^{55}\text{Fe } K_{\alpha}$



# Measurements – incomplete clear

on depleted 50  $\mu\text{m}$  thick EDET structures



Clear high voltage and clear pulse length ( $t_c$ ) influence

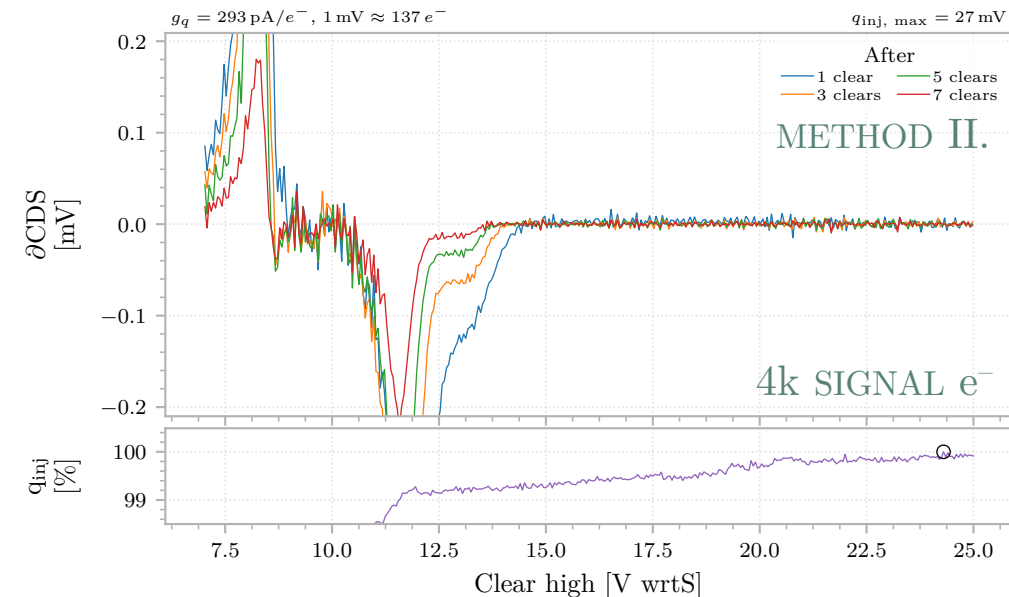
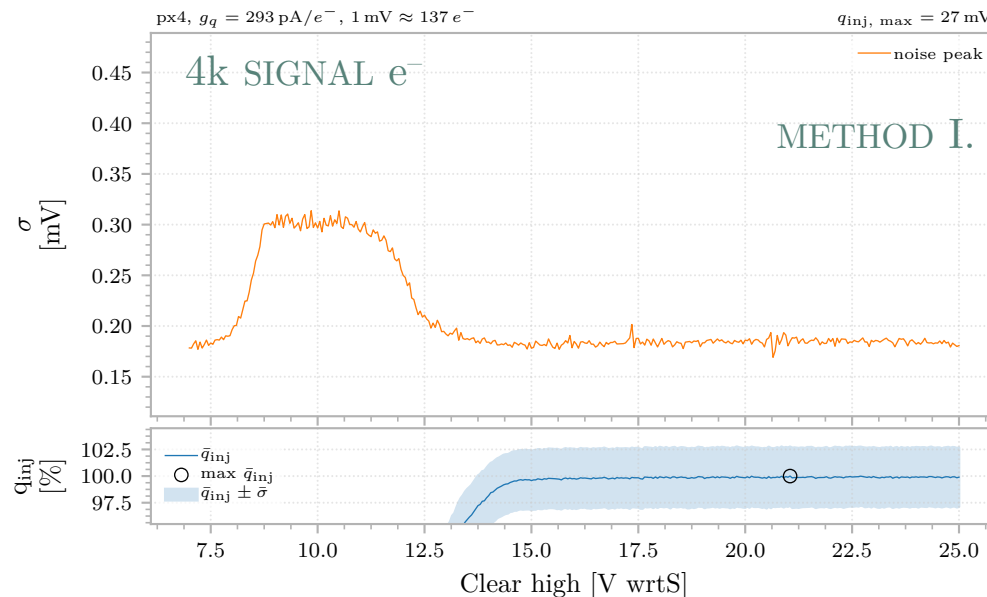
- efficiency of complete charge removal from internal gate and overflow regions.

Slow switching stage of SwitcherS ASIC limits  $t_c > 70$  ns. Final camera setup  $t_c \sim 20$  ns achieved with SwitcherB ASIC.

W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; SMALL SIGNAL CHARGE  $\sim 2.5 \times {}^{55}\text{Fe } K_{\alpha}$ ; HARDEST TO REMOVE



# Measurements – incomplete clear

on depleted 50  $\mu\text{m}$  thick EDET structures



Clear high voltage and clear pulse length ( $t_c$ ) influence

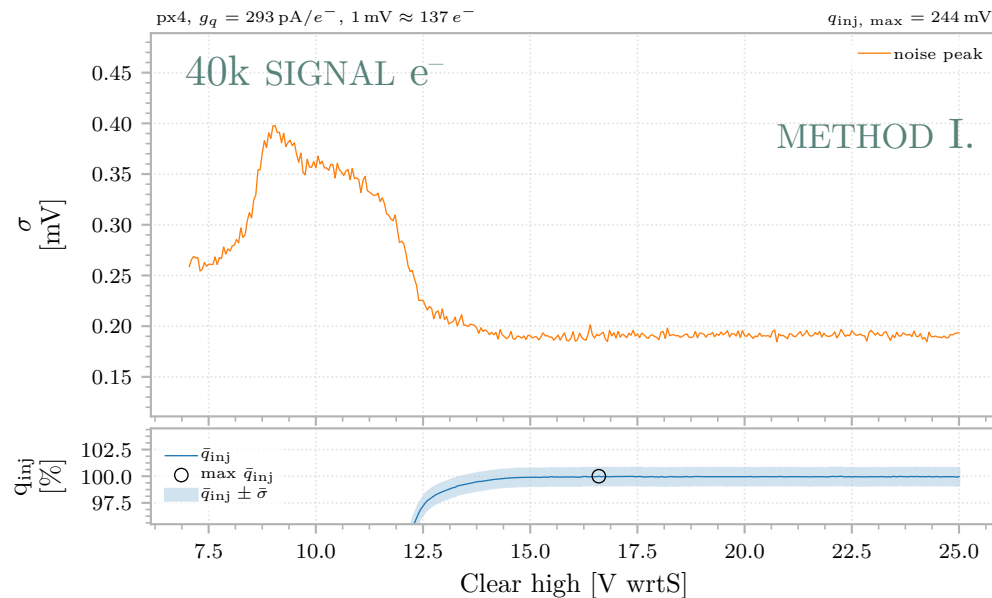
- efficiency of complete charge removal from internal gate and overflow regions.

Slow switching stage of SwitcherS ASIC limits  $t_c > 70$  ns. Final camera setup  $t_c \sim 20$  ns achieved with SwitcherB ASIC.

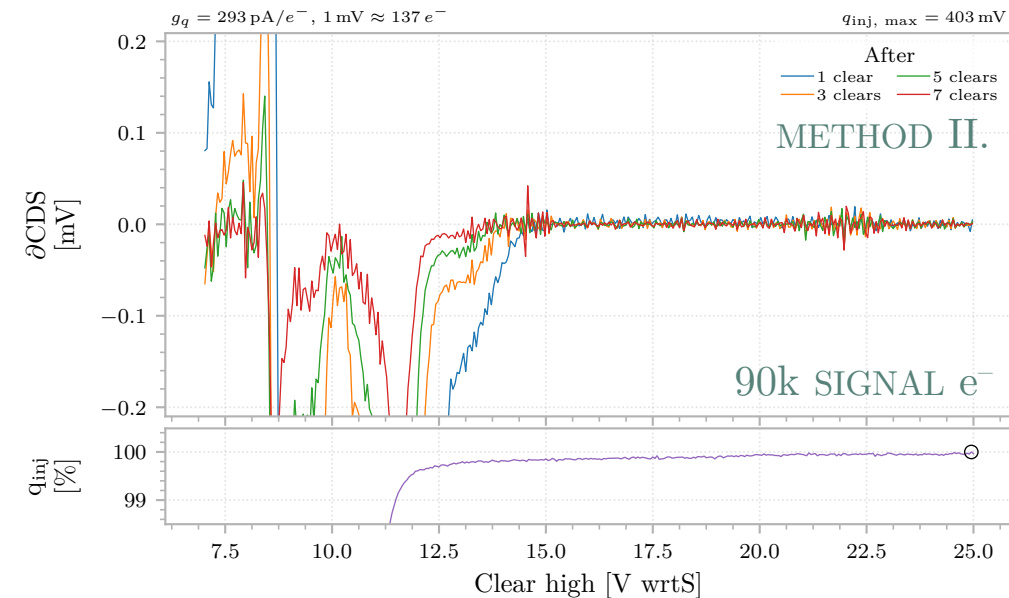
W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; ALMOST FULL INTERNAL GATE



FFIL; FILLING THE OVERFLOW REGIONS



# Measurements – incomplete clear

on depleted 50  $\mu\text{m}$  thick EDET structures



Clear high voltage and clear pulse length ( $t_c$ ) influence

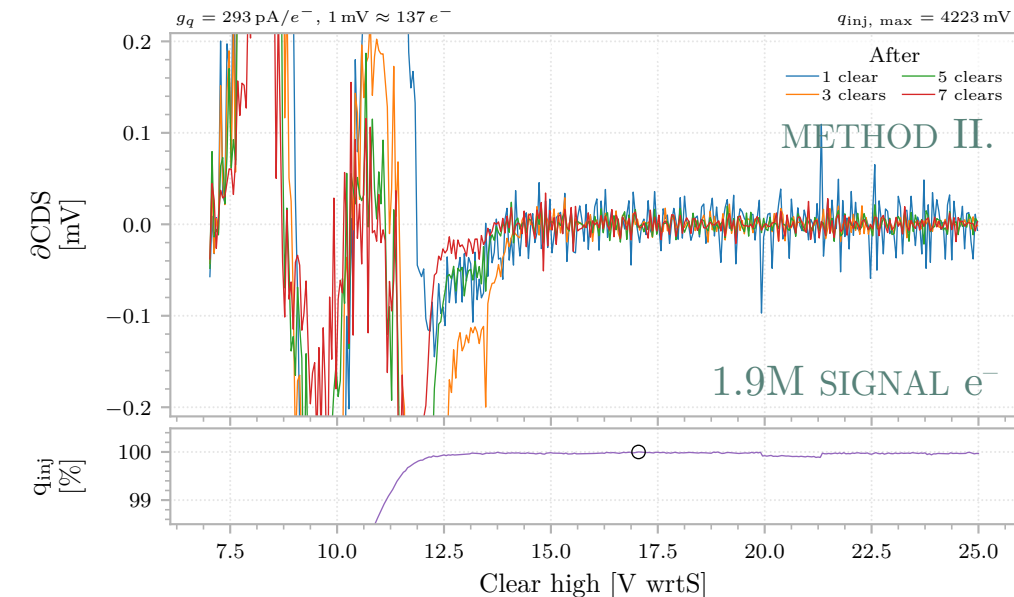
- efficiency of complete charge removal from internal gate and overflow regions.

Slow switching stage of SwitcherS ASIC limits  $t_c > 70$  ns. Final camera setup  $t_c \sim 20$  ns achieved with SwitcherB ASIC.

W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; COMPLETELY FILLED STATE



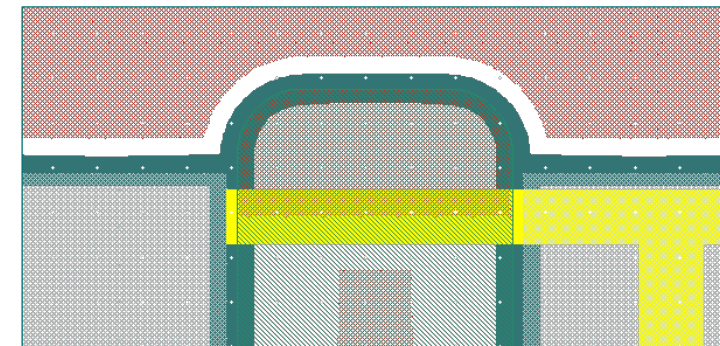
# Measurements – charge collection

on depleted 50  $\mu\text{m}$  thick EDET structures

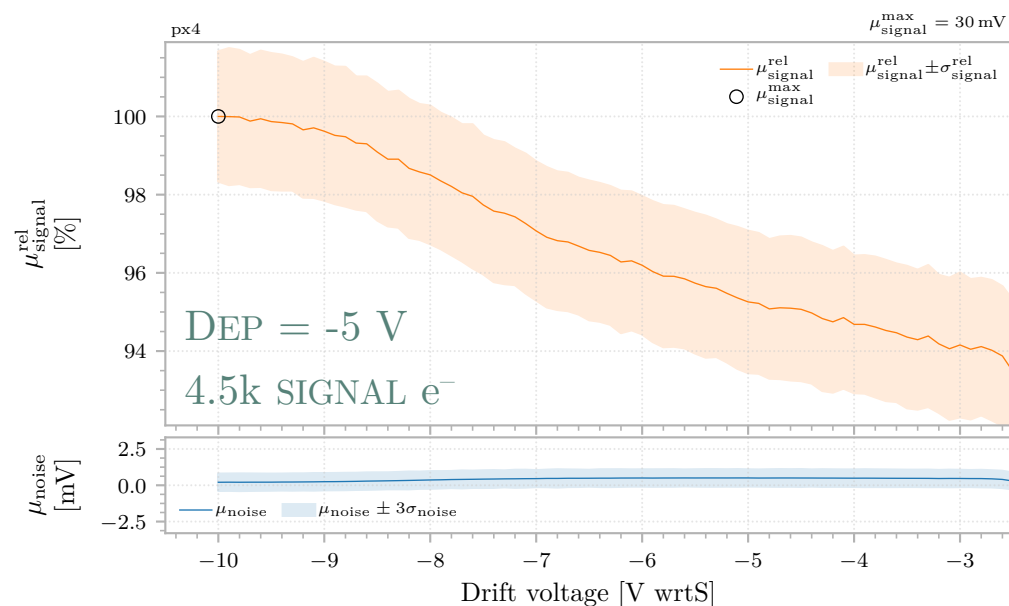
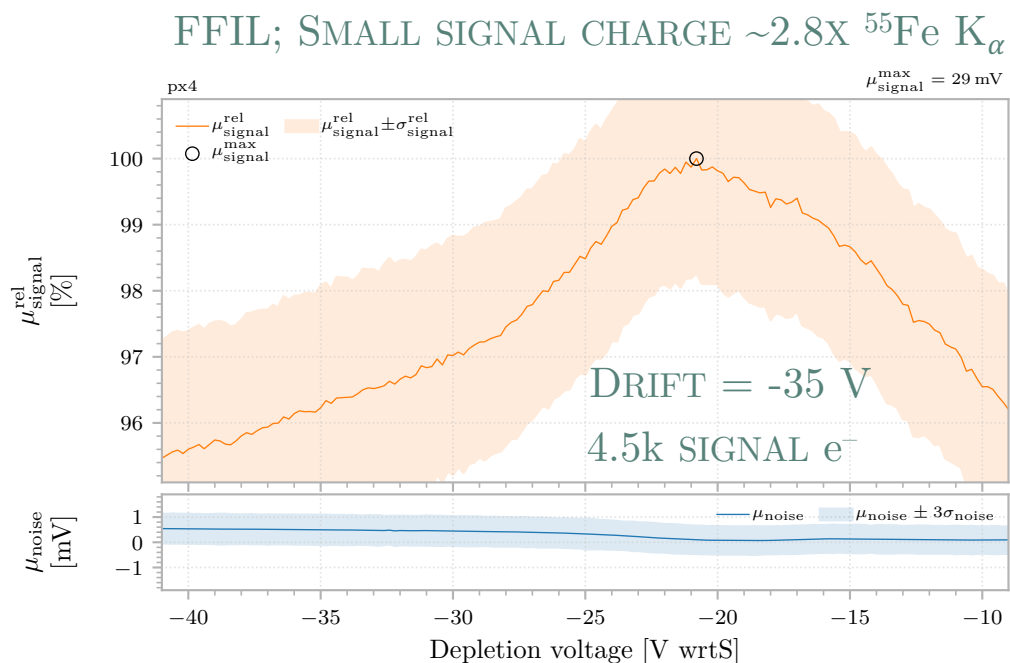


## Depletion and Drift voltage influence

- integrated 1<sup>st</sup> stage amplification ( $g_q$ ),
- charge loss to Clear, and
- charge loss to Drift region.



W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V



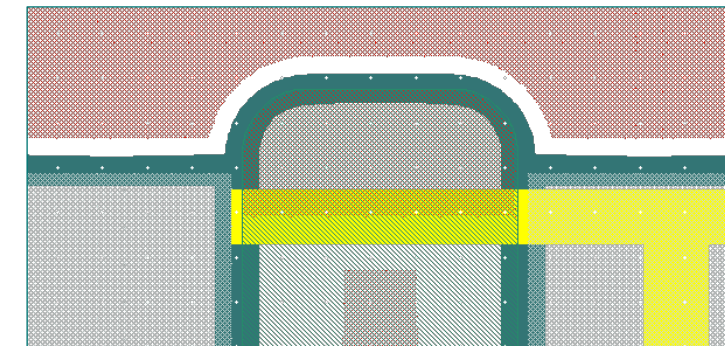
# Measurements – charge collection

on depleted 50  $\mu\text{m}$  thick EDET structures



## Depletion and Drift voltage influence

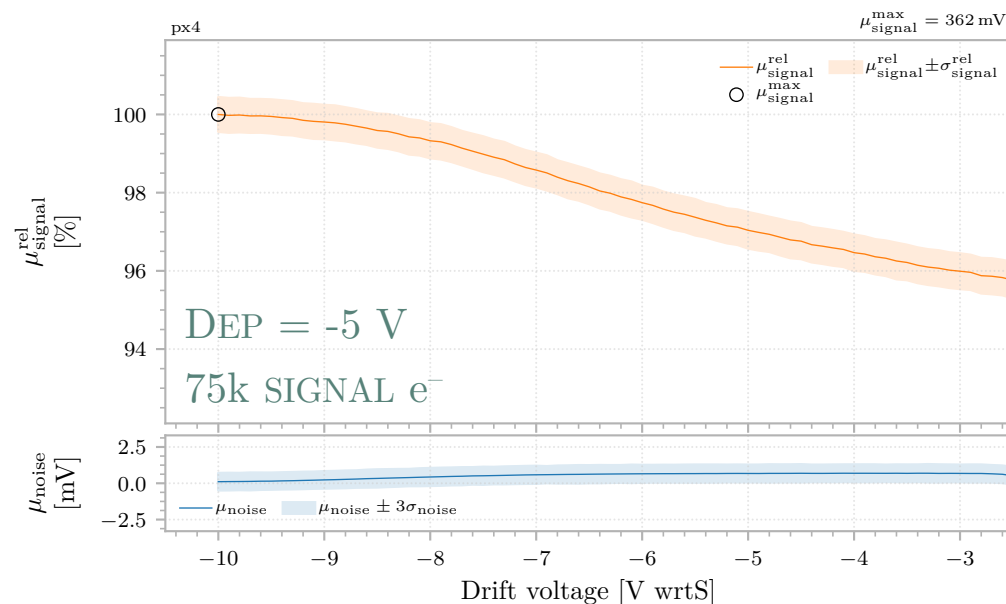
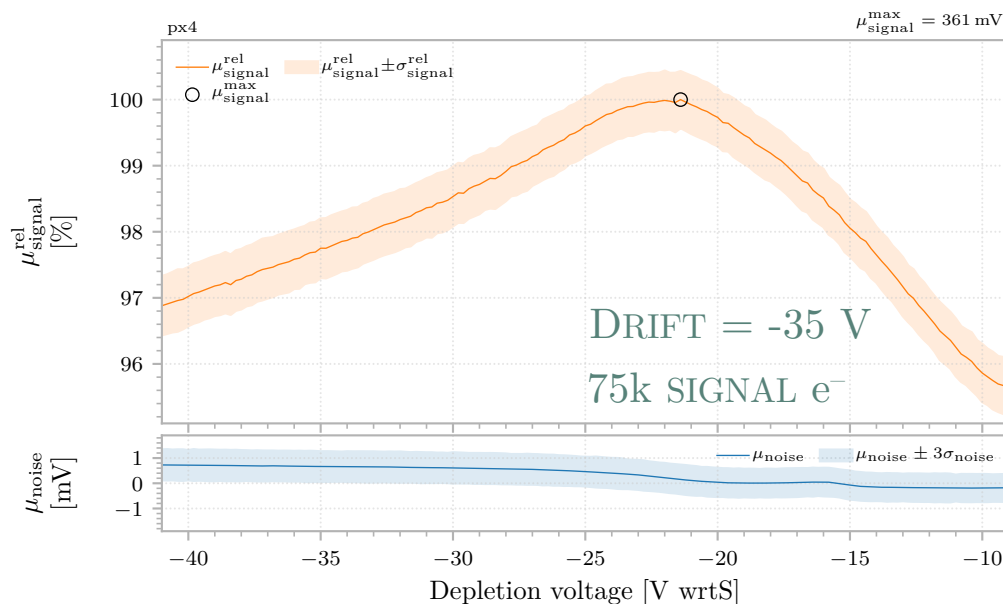
- integrated 1<sup>st</sup> stage amplification ( $g_q$ ),
- charge loss to Clear, and
- charge loss to Drift region.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

## FFIL; FILLING THE OVERFLOW REGIONS; LESS LOSSES – FILLED POTENTIAL POCKET UNDER DRIFT



# Measurements – charge collection

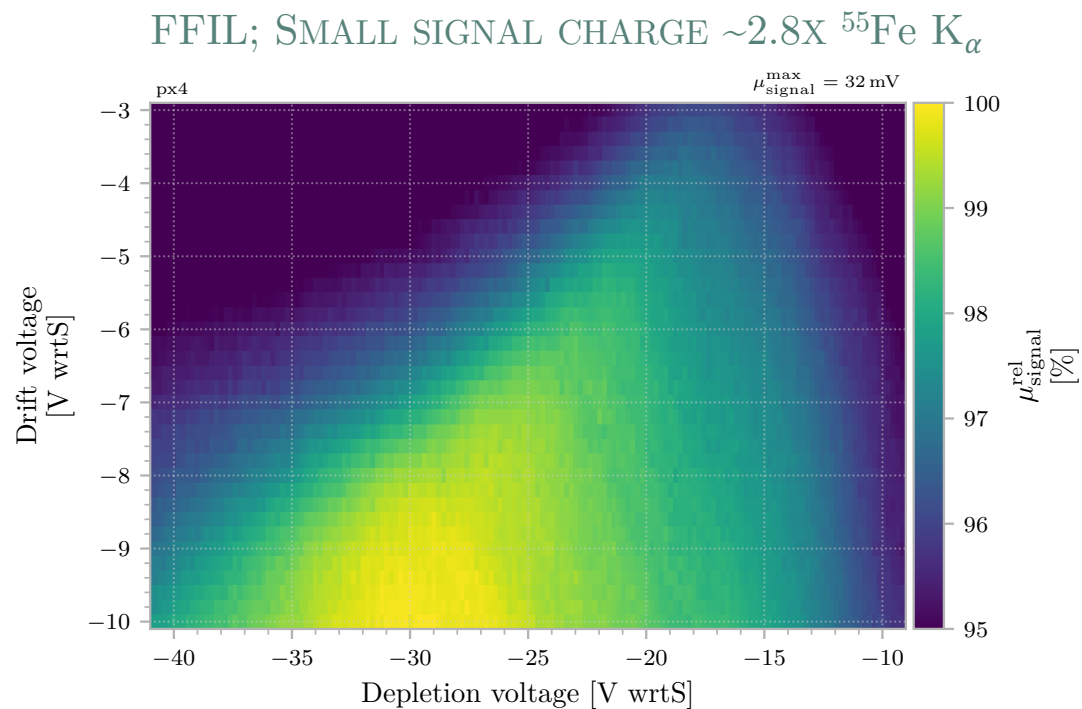
on depleted 50  $\mu\text{m}$  thick EDET structures



## Depletion and Drift voltage influence

- integrated 1<sup>st</sup> stage amplification ( $g_q$ ),
- charge loss to Clear, and
- charge loss to Drift region.

W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V



OPERATIONAL POINT ALSO DEPENDS ON THE DRIFT AND THE DEPLETION CURRENT DUE TO PROBLEMATIC HEAT DISSIPATION IN THIN DEVICES.

# Measurements – charge collection

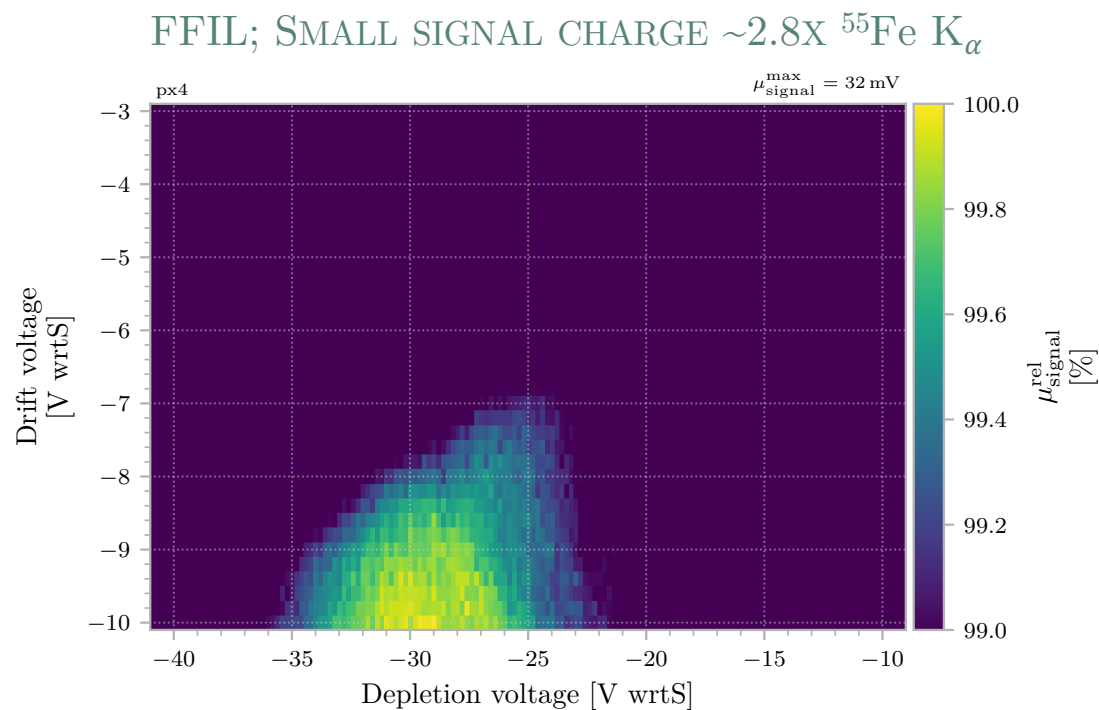
on depleted 50  $\mu\text{m}$  thick EDET structures



## Depletion and Drift voltage influence

- integrated 1<sup>st</sup> stage amplification ( $g_q$ ),
- charge loss to Clear, and
- charge loss to Drift region.

W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

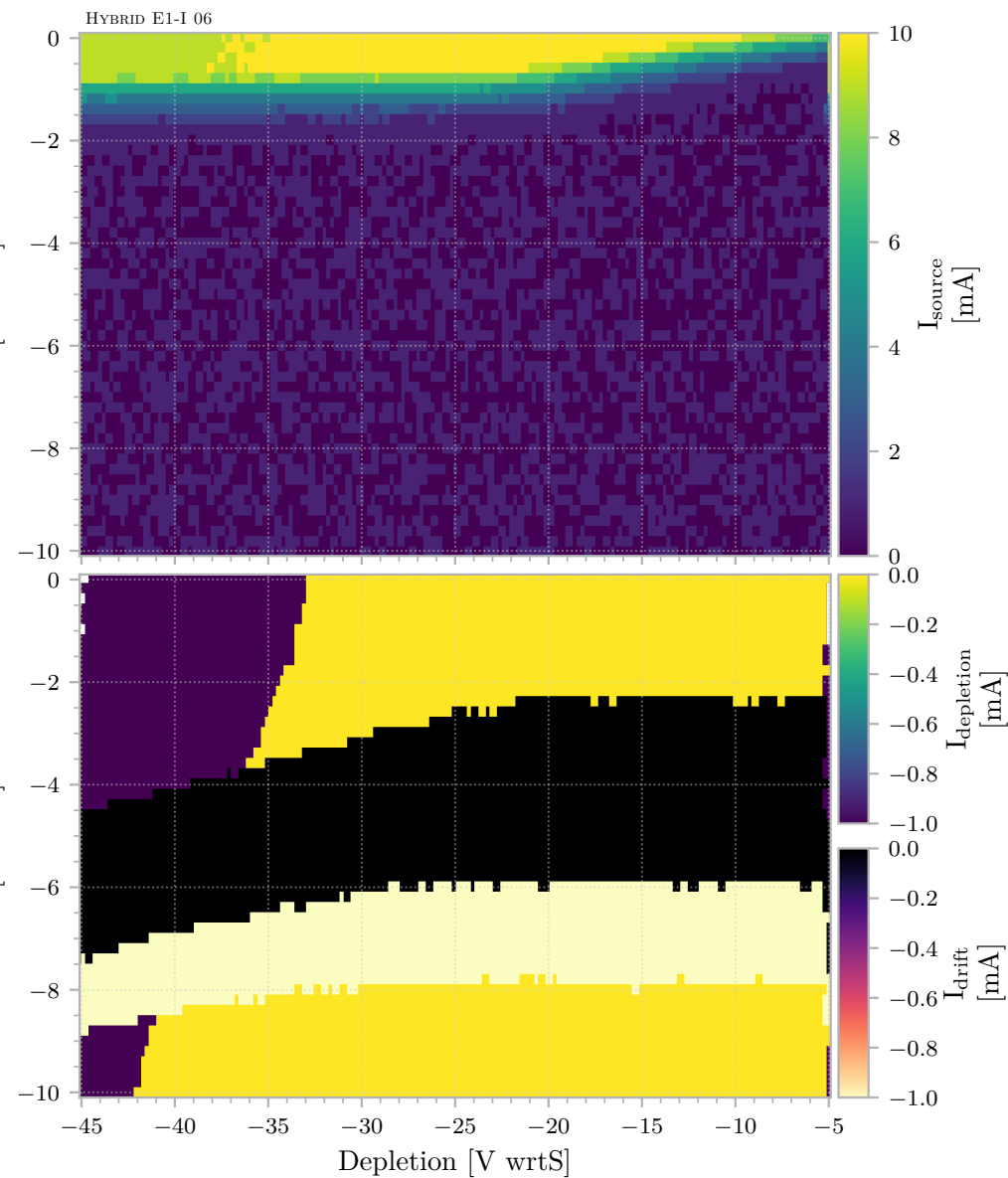
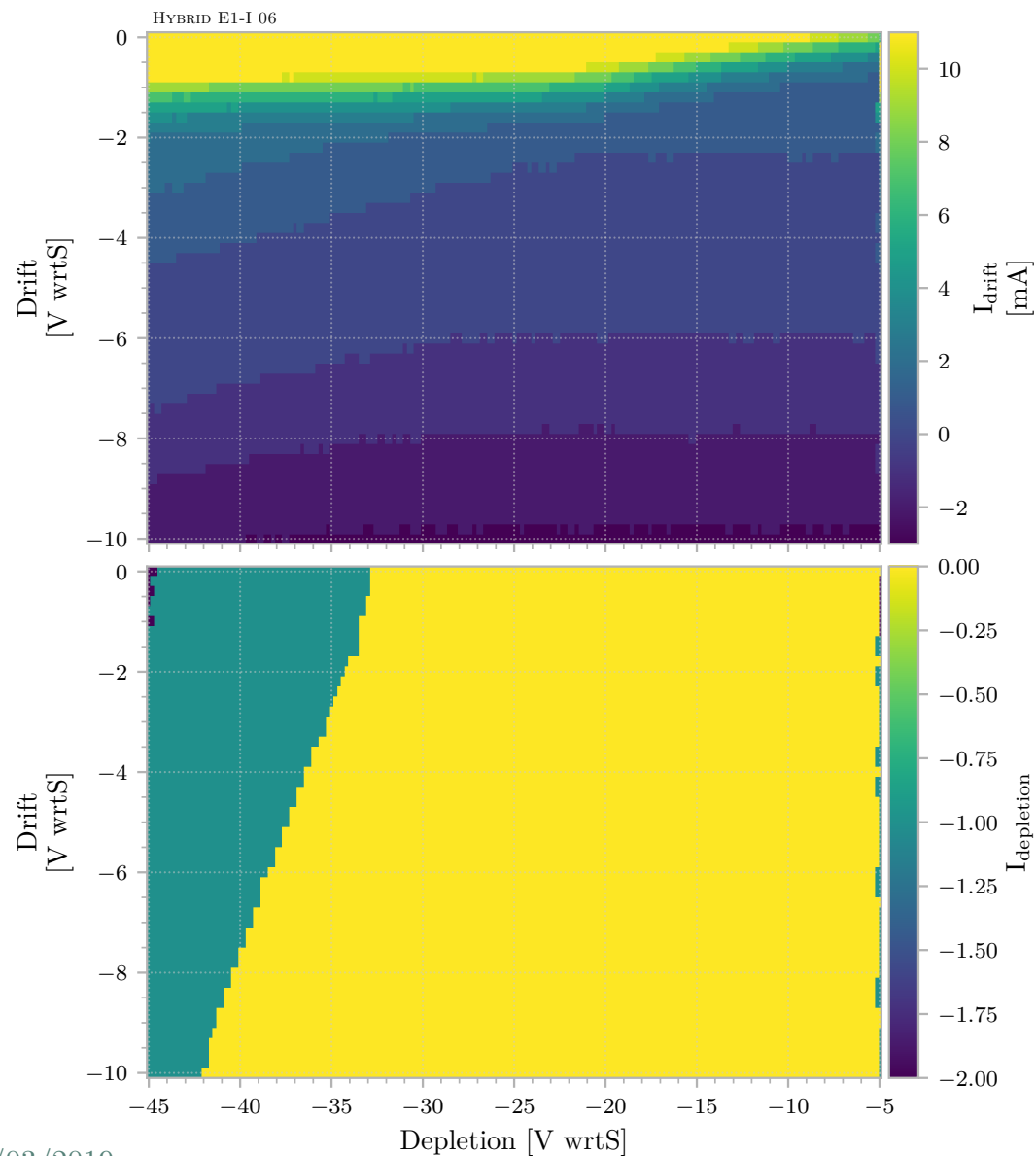


OPERATIONAL POINT ALSO DEPENDS ON THE DRIFT AND THE DEPLETION CURRENT DUE TO PROBLEMATIC HEAT DISSIPATION IN THIN DEVICES.



# Measurements – charge collection

on depleted 50  $\mu\text{m}$  thick EDET structures



# Measurements – charge collection

on depleted 50  $\mu\text{m}$  thick EDET structures

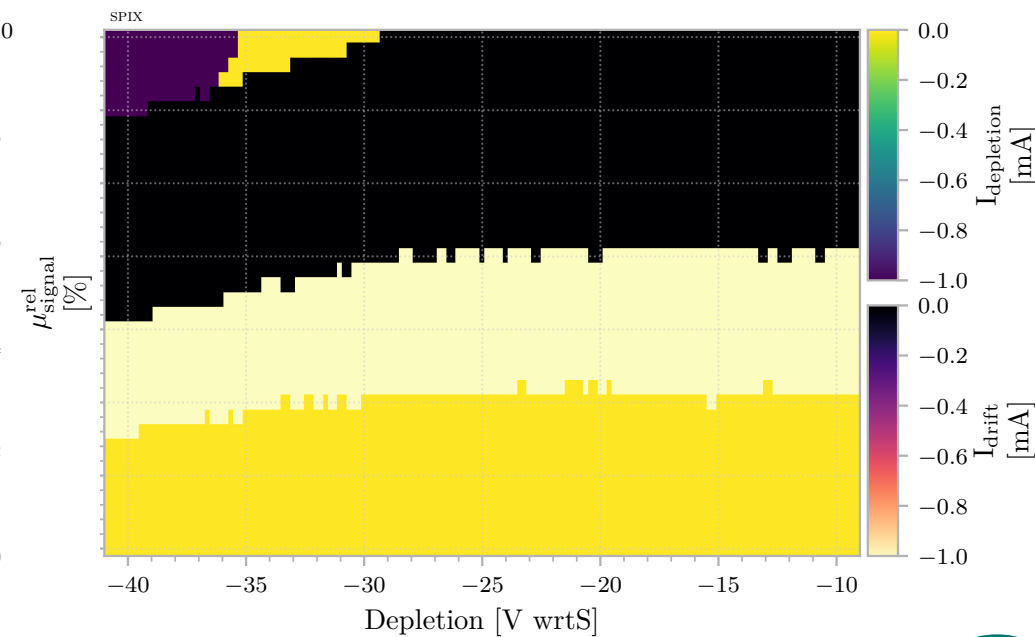
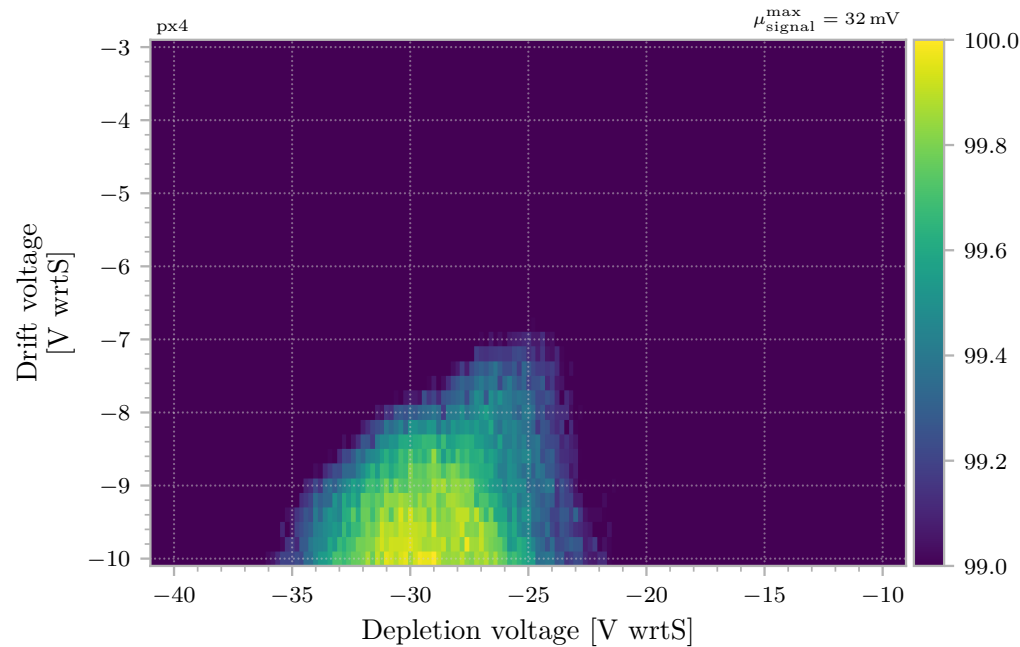


## Depletion and Drift voltage influence

- integrated 1<sup>st</sup> stage amplification ( $g_q$ ),
- charge loss to Clear, and
- charge loss to Drift region.

W09 F07	
Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

FFIL; SMALL SIGNAL CHARGE  $\sim 2.8 \times {}^{55}\text{Fe } K_{\alpha}$



# Measurements – noise v integration time

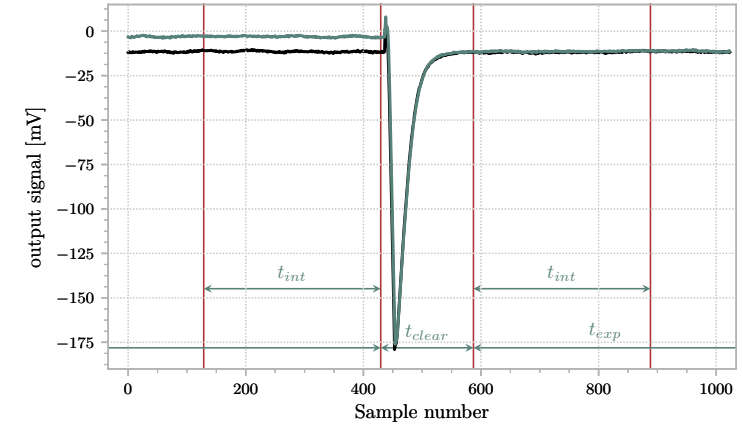
on depleted 50  $\mu\text{m}$  thick EDET structures



Integration time ( $t_{\text{int}}$ ) influences

- the overall noise performance of the system.

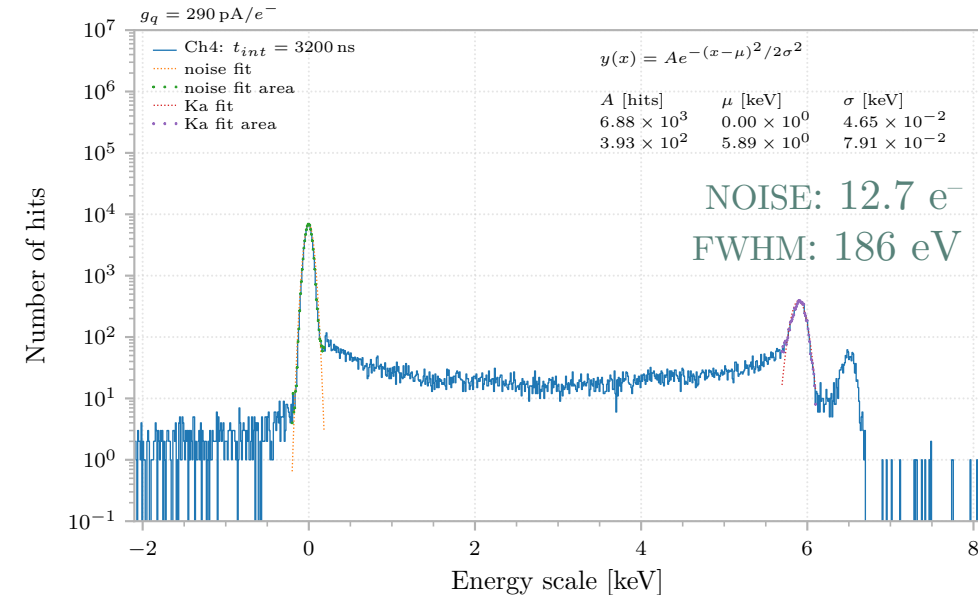
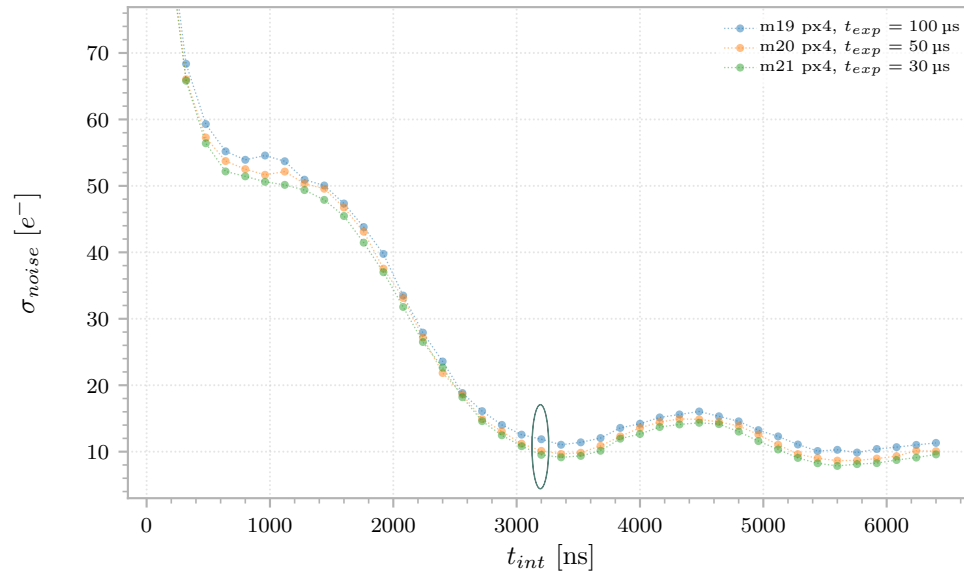
Noise dominated by Leakage Current and Common Mode Noise.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	-21.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

$^{55}\text{Fe}$  RADIOACTIVE SOURCE ILLUMINATION



# Measurements – noise v integration time

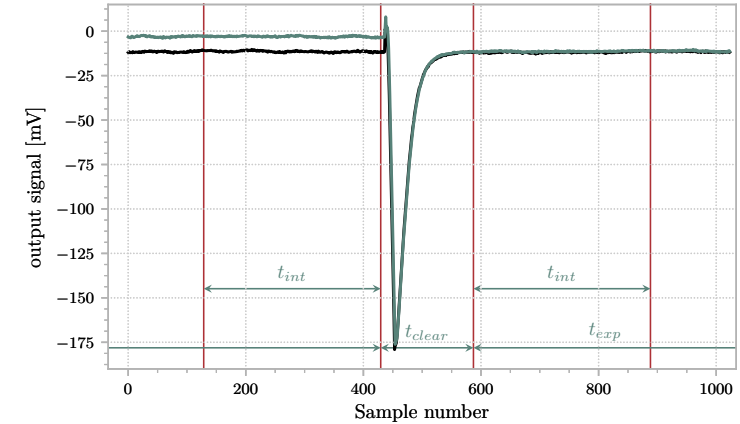
on depleted 50  $\mu\text{m}$  thick EDET structures



Integration time ( $t_{\text{int}}$ ) influences

- the overall noise performance of the system.

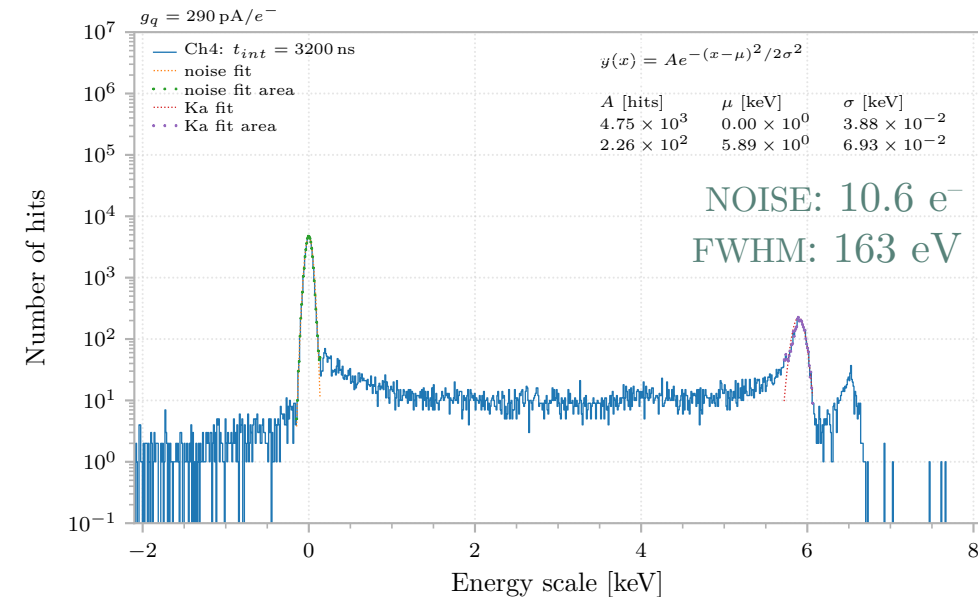
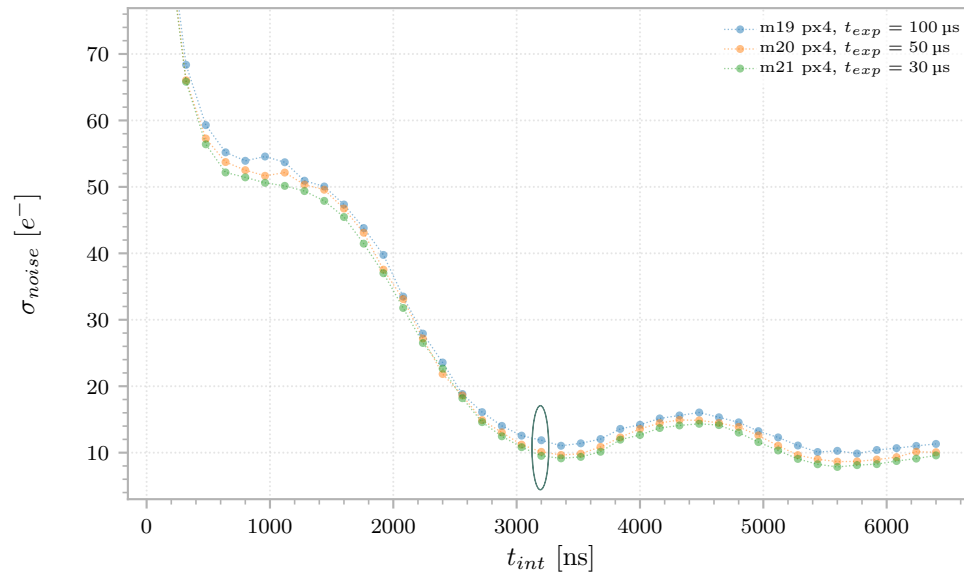
Noise dominated by Leakage Current and Common Mode Noise.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
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Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
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Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	-21.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

$^{55}\text{Fe}$  RADIOACTIVE SOURCE ILLUMINATION



# Measurements – noise v integration time

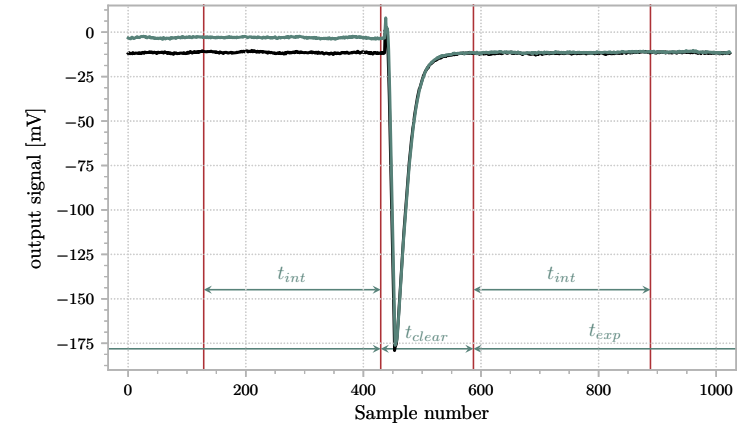
on depleted 50  $\mu\text{m}$  thick EDET structures



Integration time ( $t_{\text{int}}$ ) influences

- the overall noise performance of the system.

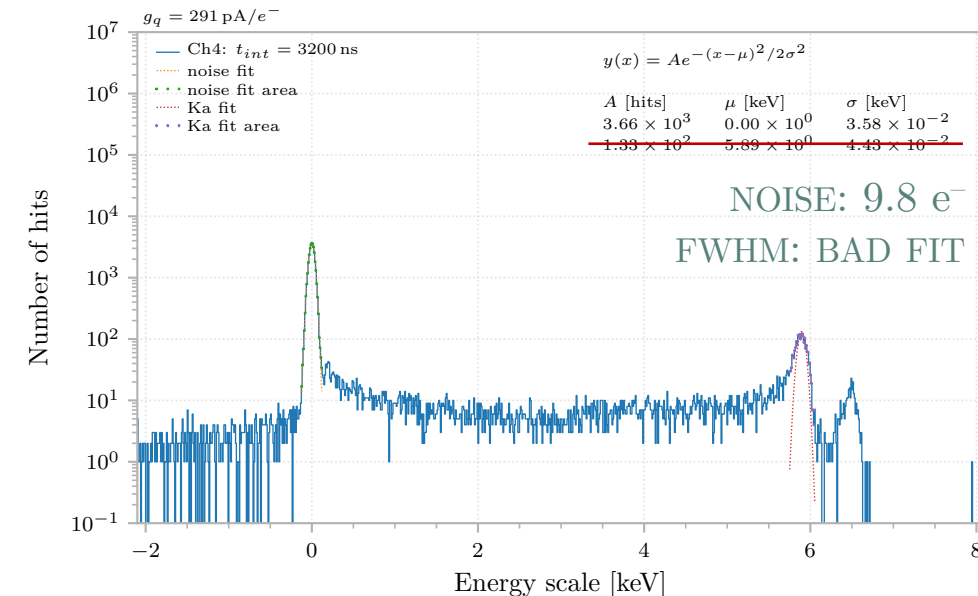
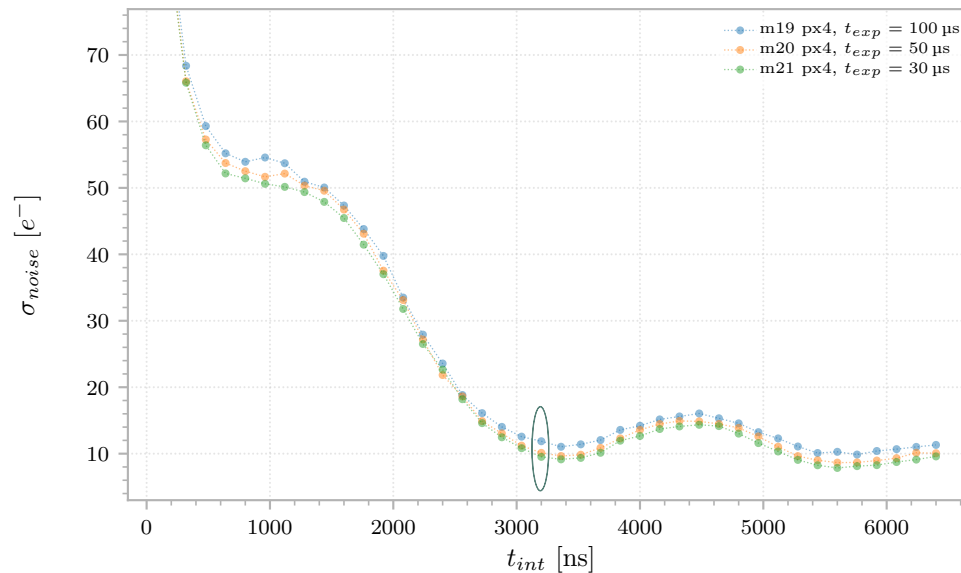
Noise dominated by Leakage Current and Common Mode Noise.



W09 F07

Thickness	50 $\mu\text{m}$
Gate L	5.0 $\mu\text{m}$
Gate W	27.2 $\mu\text{m}$
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	-21.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

$^{55}\text{Fe}$  RADIOACTIVE SOURCE ILLUMINATION



# Response function – Calibration

of depleted 50  $\mu\text{m}$  thick EDET structures



## Procedure:

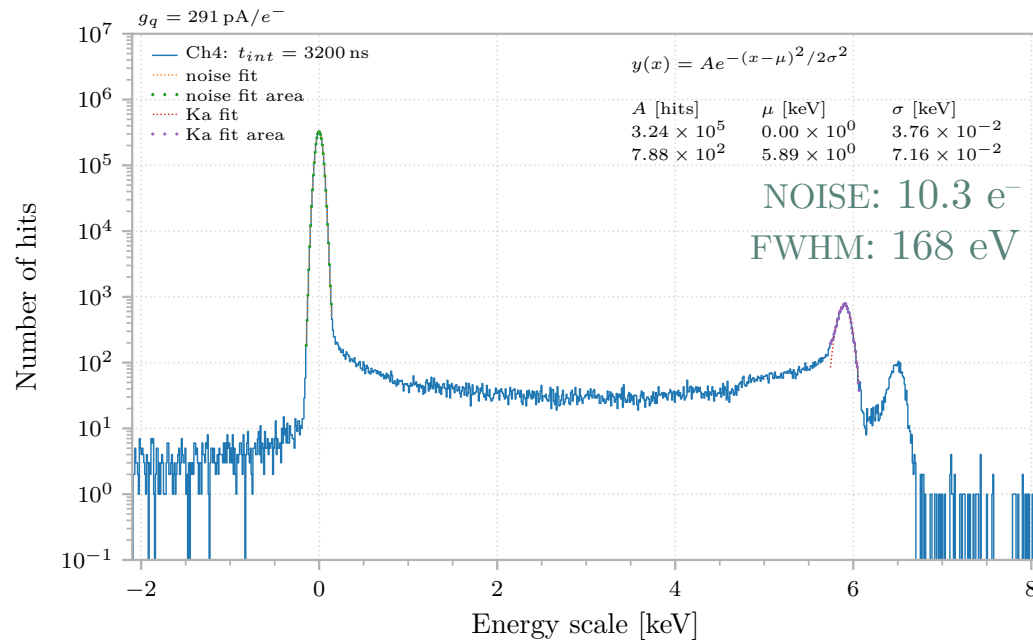
- insertion of fixed amount of charge by  $^{55}\text{Fe}$  radioactive source at optimized operation voltages
- extraction of the primary  $g_q$
- explore the full dynamic range with calibrated LED pulses and leakage current

PRIMARY  $g_q = 291 \text{ pA}/e^- (1 \pm 0.014)$

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## $^{55}\text{Fe}$ RADIOACTIVE SOURCE ILLUMINATION



# Response function – Dynamic range

of depleted 50  $\mu\text{m}$  thick EDET structures



## Procedure:

- insertion of fixed amount of charge by  $^{55}\text{Fe}$  radioactive source at optimized operation voltages
- extraction of the primary  $g_q$
- explore the full dynamic range with calibrated LED pulses and leakage current

PRIMARY  $g_q = 291 \text{ pA/e}^- (1 \pm 0.003)$

SECONDARY  $g_q = 70 \text{ pA/e}^- (1 \pm 0.10)$

LEAKAGE  $I_L = 0.57 \text{ e}^-/\mu\text{s} (1 \pm 0.05)$

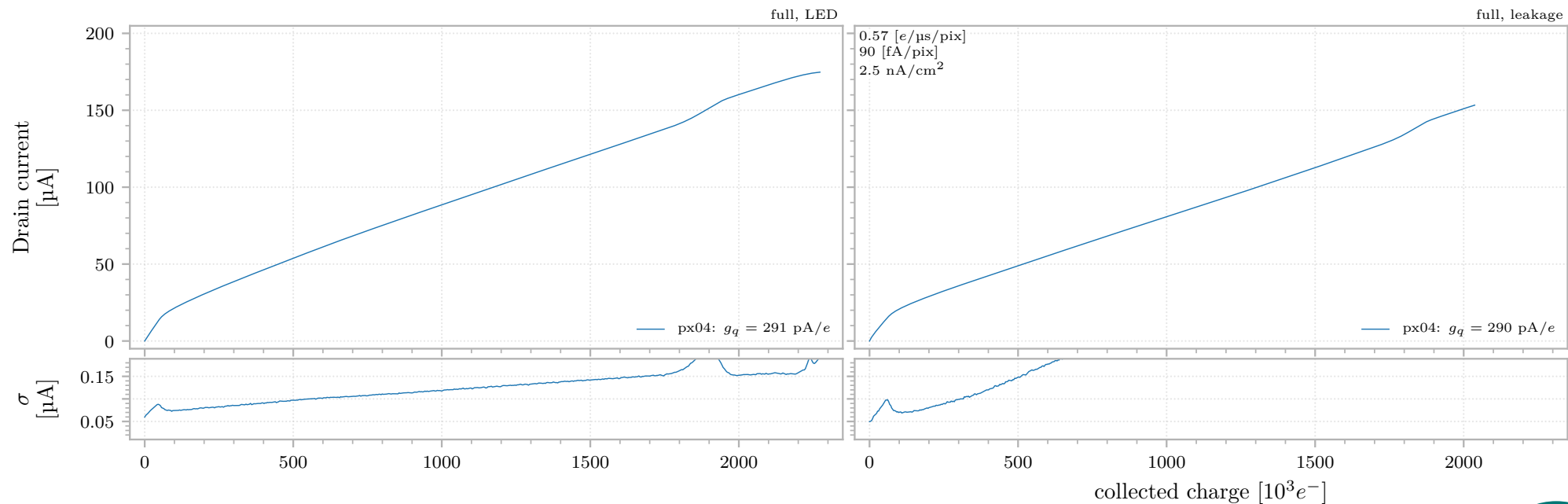
W09 F07

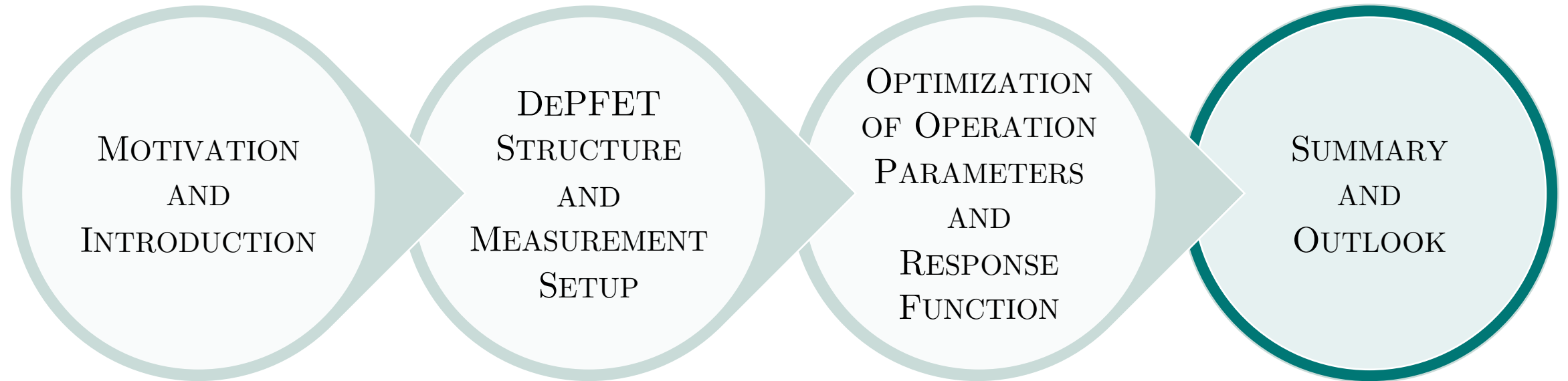
Thickness 50  $\mu\text{m}$   
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Drain -5.0 V  
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 Clear low 1.0 V  
 Clear high 18.0 V  
 Clear Gate -0.5 V  
 Depletion -21.0 V  
 Bulk 10.0 V  
 Drift -5.0 V  
 Guard -5.0 V

FFIL;  $t_{\text{exp}} = 3.1 \text{ ms}$ ; 601 PULSES

LEAKAGE CURRENT;  $t_{\text{exp}} = 3.6 \text{ s}$ ;







# Summary and outlook

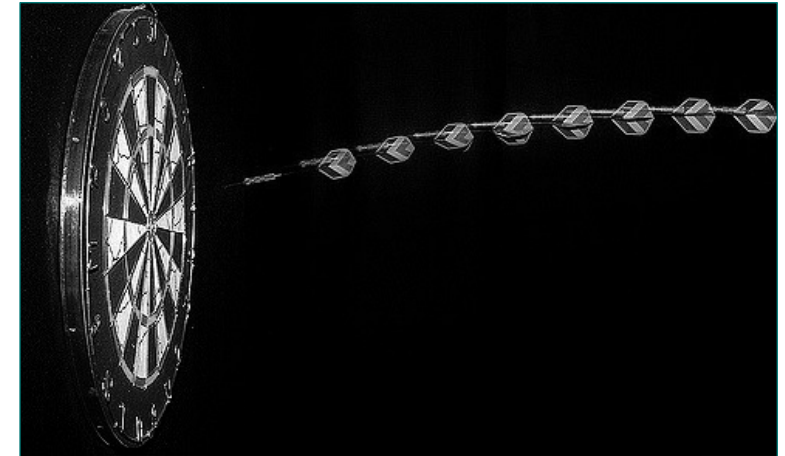
for the project

## EDET project

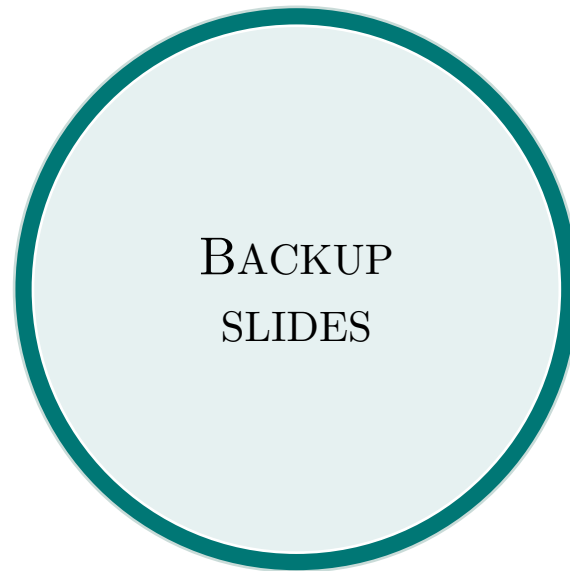
- pilot production successfully finished and characterized
- fabrication of the main batch has been resumed
- pilot devices showing expected results
  - signal compression
    - 290 pA/e<sup>-</sup> for the first ~50 k signal e<sup>-</sup>
    - ~70 pA/e<sup>-</sup> for the rest
  - dynamic range of >800k signal e<sup>-</sup>
  - operation window big enough to operate the large area devices

## FUTURE plans

- characterize 30 μm thin sensor and an additional “wild-card” design
- start the simulations of the design
  - possible optimizations
- radiation hardness studies



THANK YOU FOR YOUR ATTENTION!



BACKUP  
SLIDES

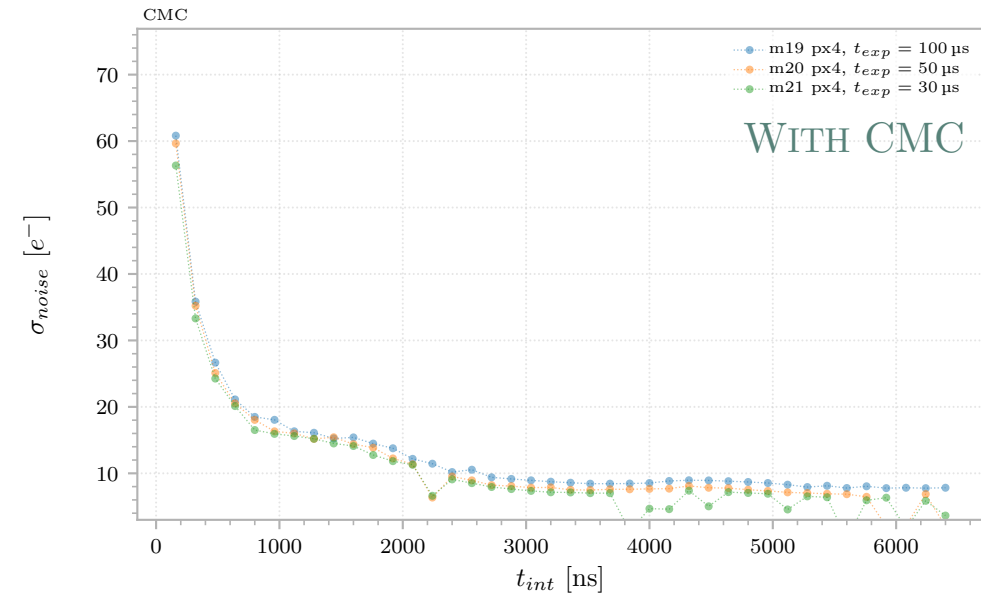
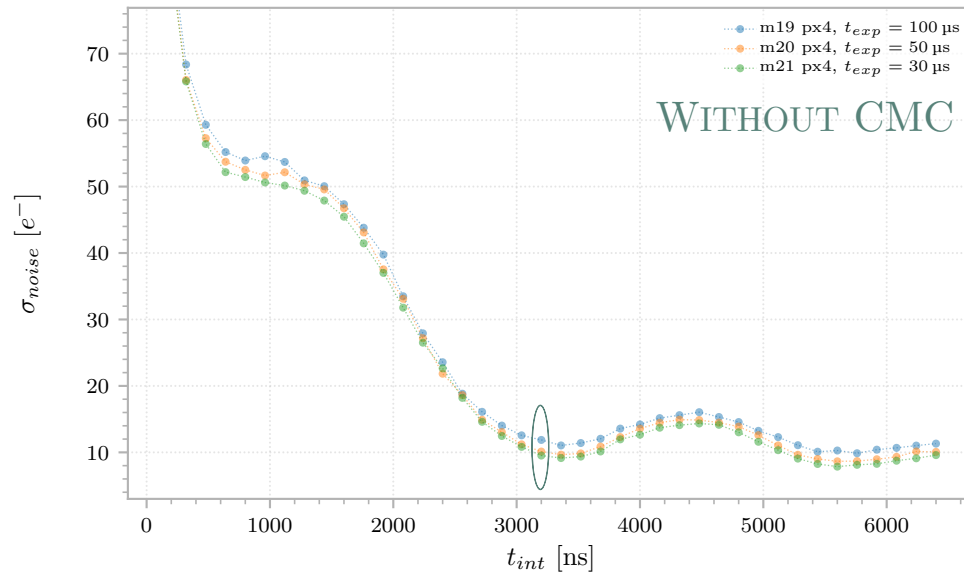
# Common mode noise



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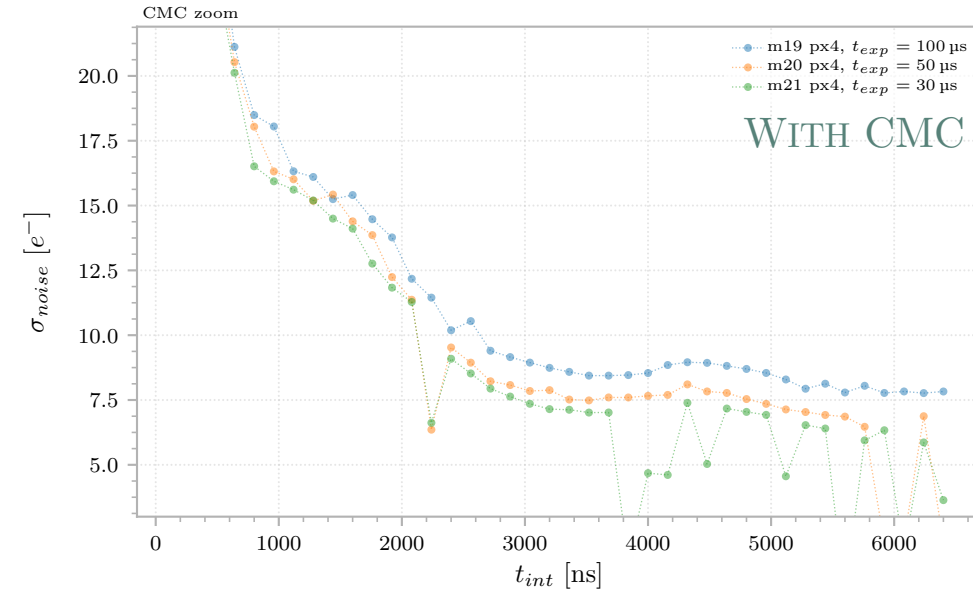
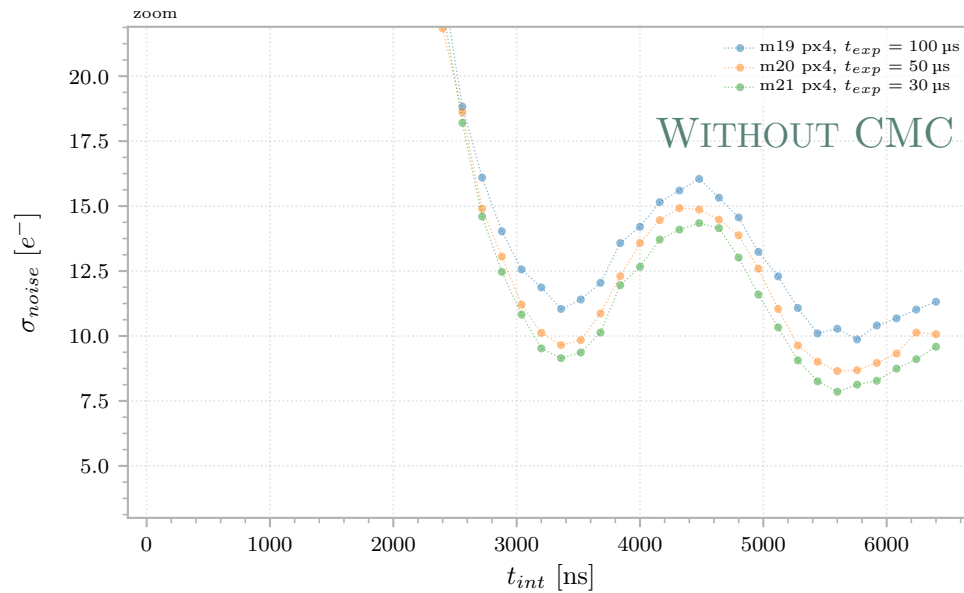
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20 % CHANGE IN  $\sigma_{noise}$



# Radiation hardness

Radiation causes positive charge buildup in Oxide:

- homogeneous radiation – compensated by gate voltage shifts
- inhomogeneous radiation – could cause problems

