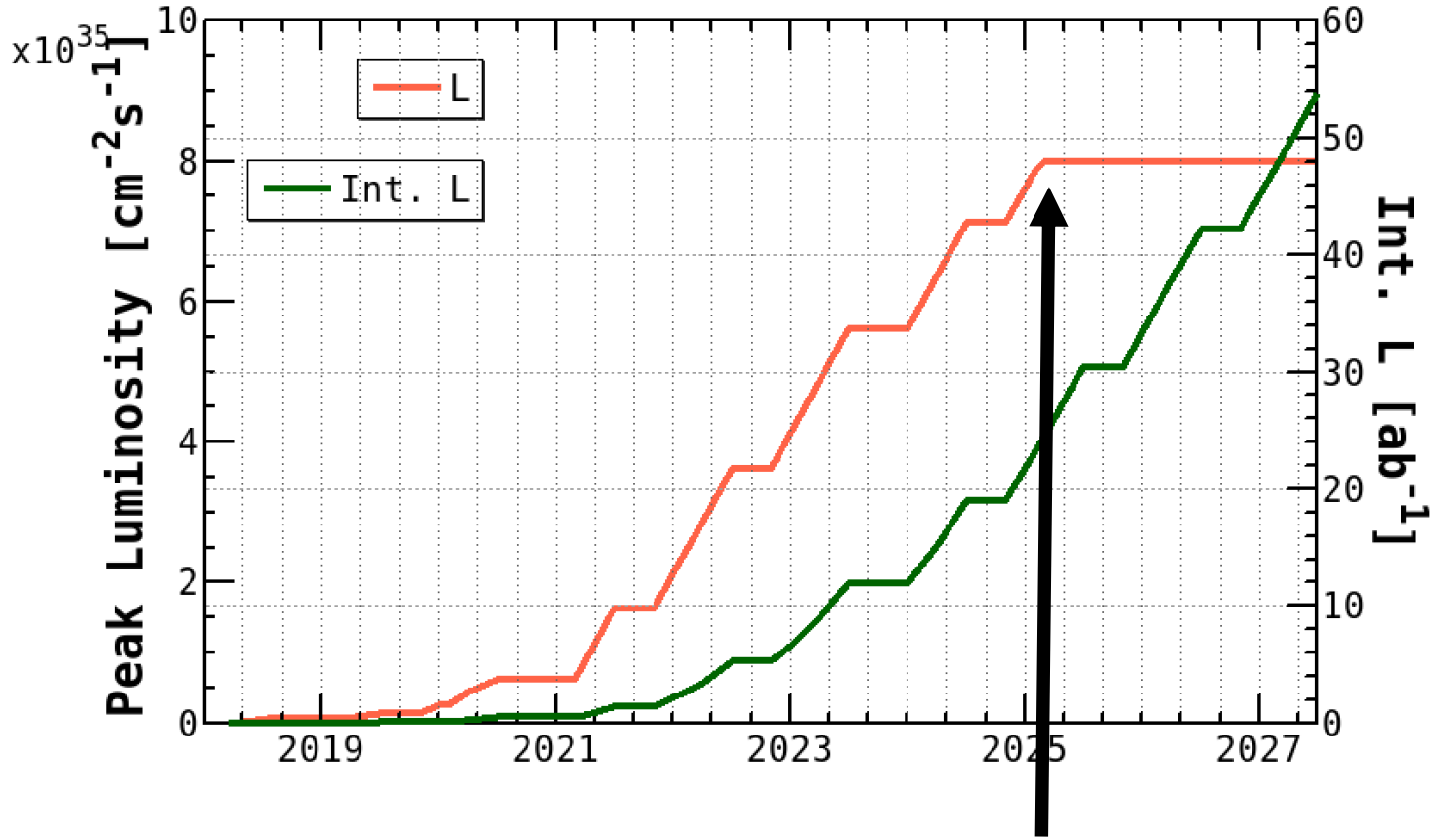
SuperKEKB upgrade (→ HyperKEKB ???)

or: is there a future for DEPFETs in HEP?

SuperKEKB schedule



2025: design peak lumi of 8e35 $cm^{-2}s^{-1}$ … then run to accumulate data …

Starting point: phase 3 BG predictions

	Phase2 findings	Dangerous at early phase3?	Dangerous at final phase3?
SR	See ~10keV peaks in PXD/FANGS	+X side: OK(PXD) -X: side: FANGS analysis ongoing	Same as left
Integrated Dose	PXD, films see more than diamonds (as expected)	Rescaled MC: marginal (no injection BG included)	Rescaled MC: marginal for SVD, critical for PXD (7x reduction needed for HER BG)
PXD occupancy	See SR-like peak, but not dominant	Rescaled MC: marginal	Rescaled MC*: critical (2x more than DHP limit)
SVD occupancy	noise (or SR-like) peak at ~10keV, not dominant	Rescaled MC: marginal	Rescaled MC*: critical (10x more than limit)
CDC rates	"persistent current" is critical.	Pure MC: marginal Rescaled MC: not prepared yet	Pure MC: critical (5x than limit) Rescaled MC: not prepared yet
TOP rates	(clean) continuous injections are not a big problem for TOP	Rescaled MC: critical** (5x than limit) for short-life PMTs, which need to survive till 2020 summer	Rescaled MC: critical (2x more than limit) for ALD-type PMTs
ECL dose on crystals	-	Pure MC: OK Rescaled MC: not prepared yet	Pure MC: critical (2x than limit) Rescaled MC: not prepared yet
KLM	?	?	?
ARICH	?	?	?

*Rescaled MC for final phase3 = (final phase3 MC) * (phase2 data/MC).
Rescaled MC for early phase3 = (final phase3 MC) * (phase2 data/MC) * ¼, or (phase2 data)* (scaling with I^2) using phase2 collimators
**At early Phase 3, background improvement will be further pursued by tuning SuperKEKB parameters and the new collimators installed

Many critical items. Expected mitigations with collimator optimization.
We will need to see how phase 3 goes

Still some unknowns

Better understanding after early phase3?

Upgrade plans

- Flavor physics has the potential of exploring new physics territory provided large enough samples are available
- Machine upgrade is not impossible
  - No concrete plan yet, just initial discussions
  - Consider a factor 5 increase in luminosity (peak and integrated)
  - Also under consideration the possibility to introduce polarization
- Initial study to understand detector limits and mitigation measures
- Explore upgrade possibilities considering evolution of technology
- Small effort that should not affect Belle II operation and physics. Useful to:
  - keep hardware-oriented expertise on the collaboration
  - imagine a longer term future for the experiment
  - understand current detector and help making it more robust

Feb 13, 2019 F.Forti - Future Upgrades

Summary

Akio Morita
March 7, 2019

- Polarization
  - Construct-able hardware design WOULD be required.
  - Lattice design and beam dynamics study WOULD be required.
- Luminosity improvement
  - No free lunch in SuperKEKB design parameter
  - Factor 5 scaling looks like difficult by using current available technology without new tunnel.
    - New (or SF) technology MIGHT be required.
    - One of technical feasible option is to make many copy of SuperKEKB system if SuperKEKB design luminosity is achievable.
- Remarks
  - Feasibility of SuperKEKB design parameter is not confirmed by real machine!
    - Beam dynamics issue (lifetime with beam-beam effect) was found after hardware fabrication start.
    - QCS measured multipole distribution predicts shorter beam lifetime than design model. (preliminary)

Detector activities currently lead by Francesco Forti (SVD)

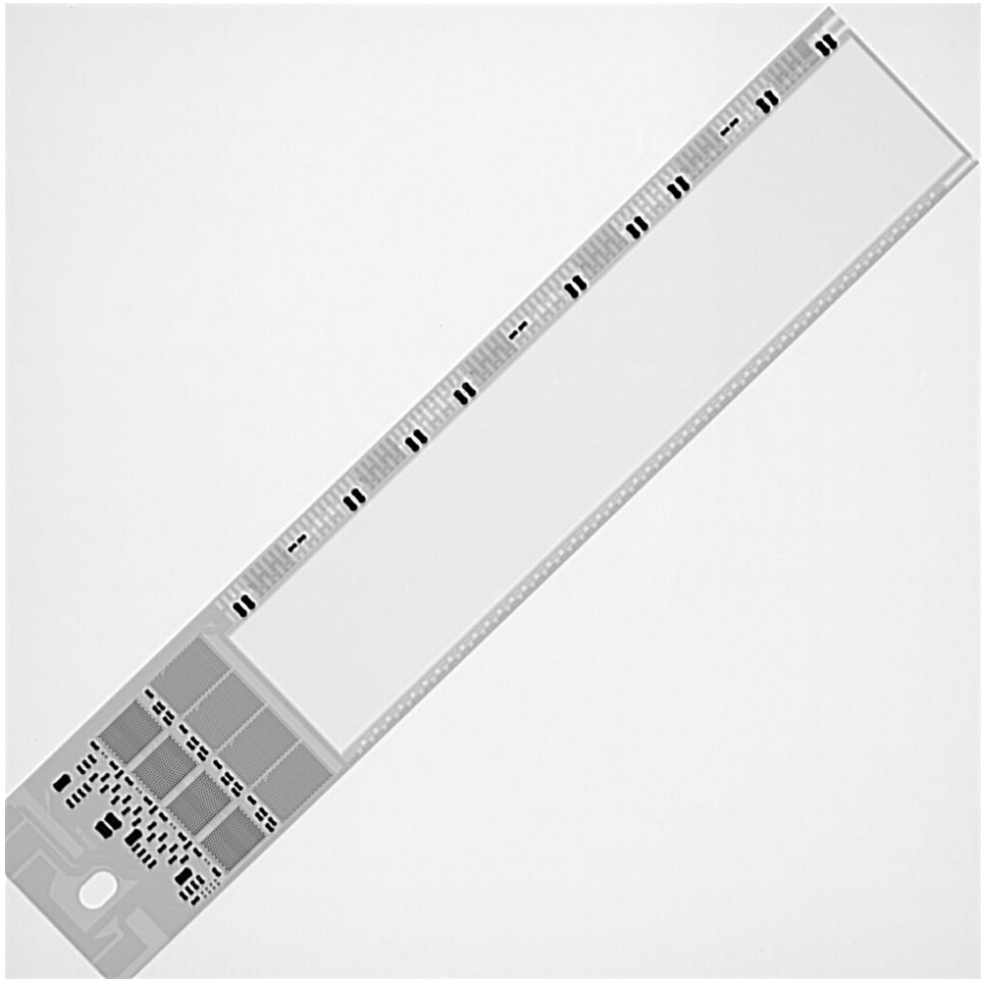
- Regular monthly meetings of UWG (upgrade working group)
  - PXD representative Carlos Marinas
- upgrade for all sub-detectors will be discussed
- VXD upgrade workshop early July at CERN (?)
  - Organized by VXD group (PXD and SVD)
  - Open for all technologies and groups, also outside from Belle II
  - Guess: in general moving towards "all-pixel vertex" detector to cope with increased occupancy (increase granularity)
    - Different flavors of CMOS pixel
    - SOIPIX/SOFIST
    - other…
- What could we, the "DEPFET Collaboration", do?

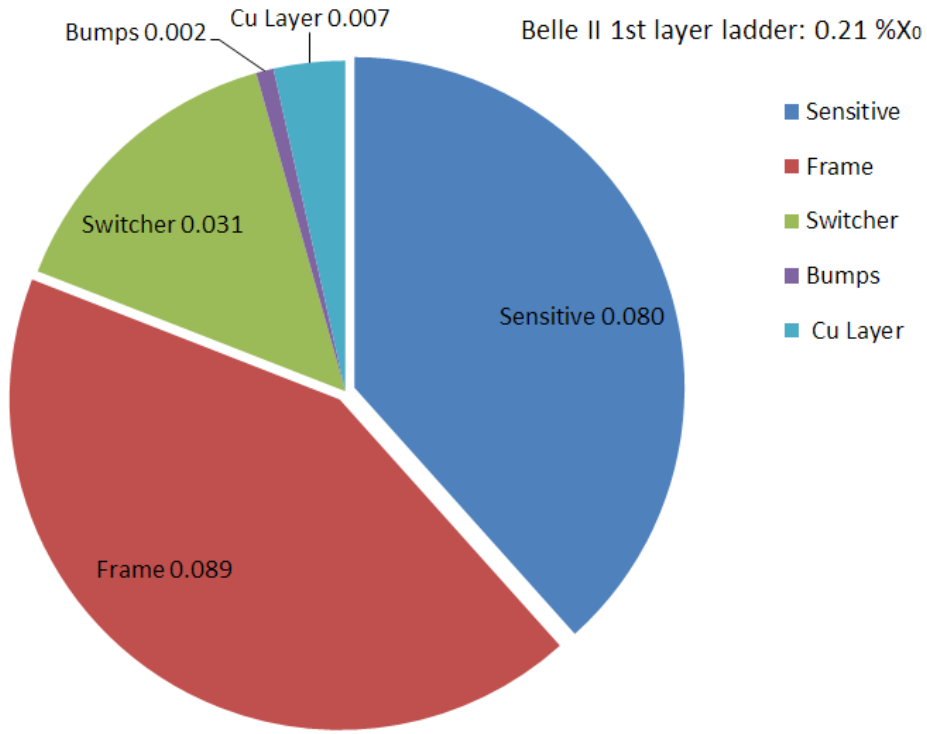
For each system

- Identify possible upgrade paths that would allow increasing luminosity by a factor >5
  - Initially just a brainstorming of possibilities to explore the entire phase space
  - Briefly examine merits/difficulties to identify the most interesting options
    - performance, robustness, technology readiness, cost, complexity, required time, etc…
- Start a deeper evaluation of most promising solutions
  - Give a ballpark estimate of cost, time, and effort required
  - If positive feedback, start a conceptual design
- Most likely will need open workshops to involve a broader community
  - Details will need to be defined

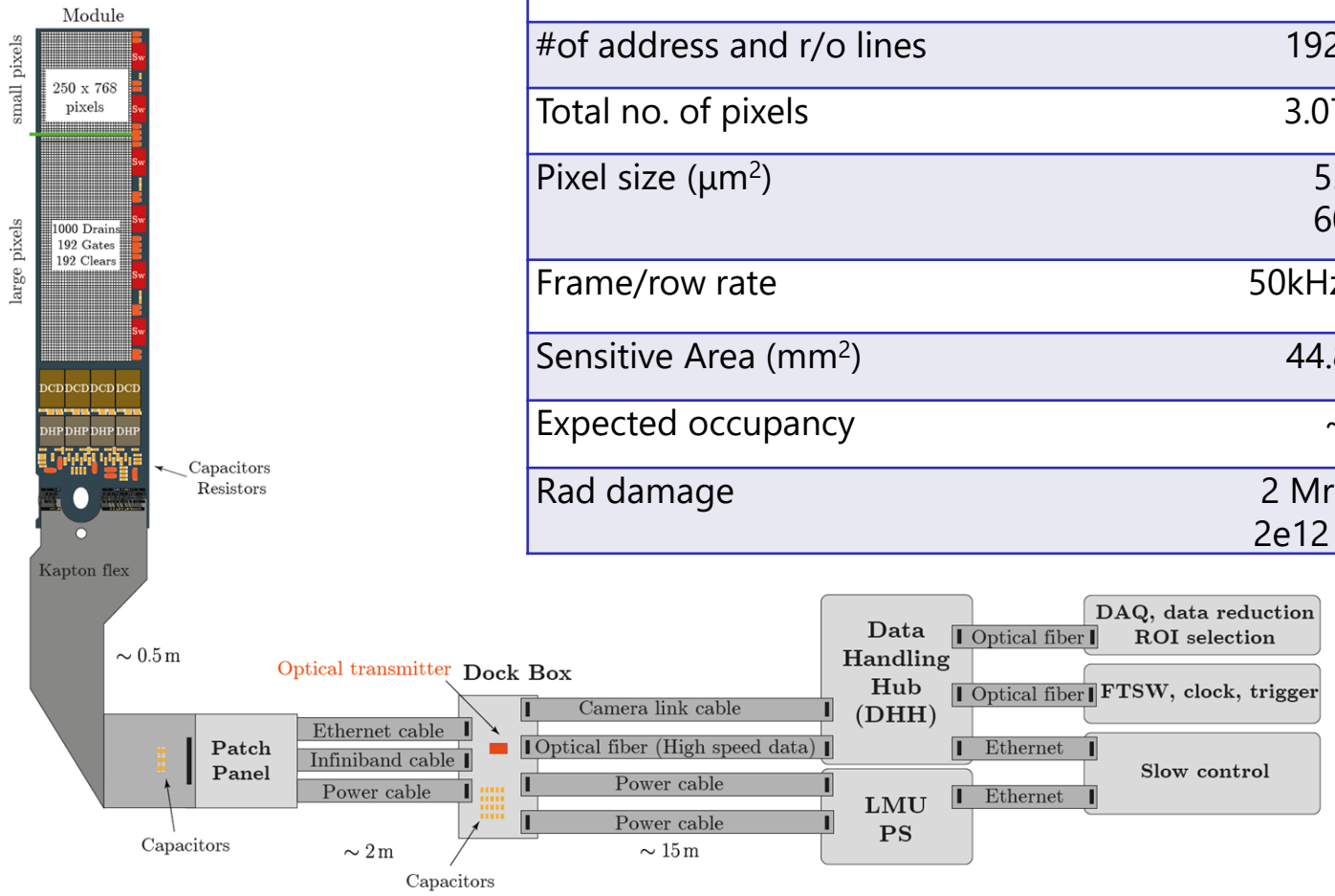
Starting point

- Assumptions
  - 5x lumi increase → 5x occupancy → need higher frame rate and/or higher granularity to keep it around 1%
  - Physics stays basically the same: low energy particles → IP resolution limited by MS, need low-mass sensors





The PXD system



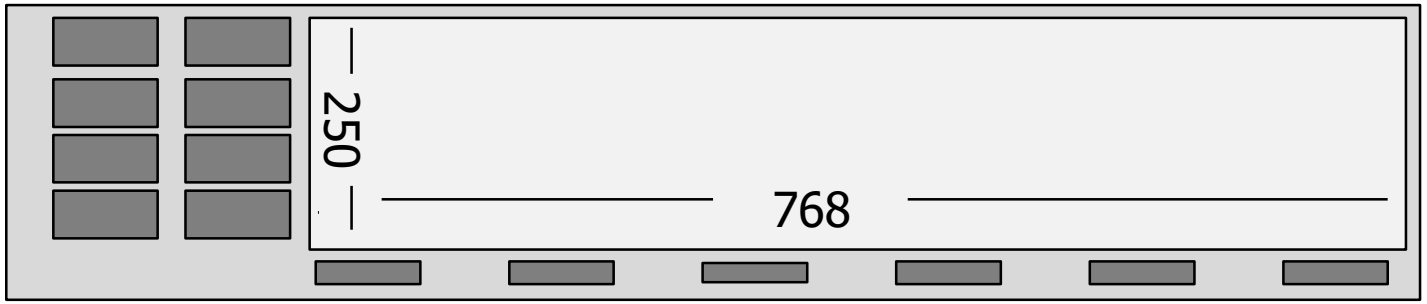
	L1	L2
# ladders (modules)	8 (16)	12 (24)
#pixels/module	768x250	768x250
#of address and r/o lines	192x1000	192x1000
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (μm^2)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Sensitive Area (mm^2)	44.8x12.5	61.44x12.5
Expected occupancy	~1%	
Rad damage	2 Mrad/year, 2e12 n_{eq}/year	

The basic idea – evolution rather than revolution

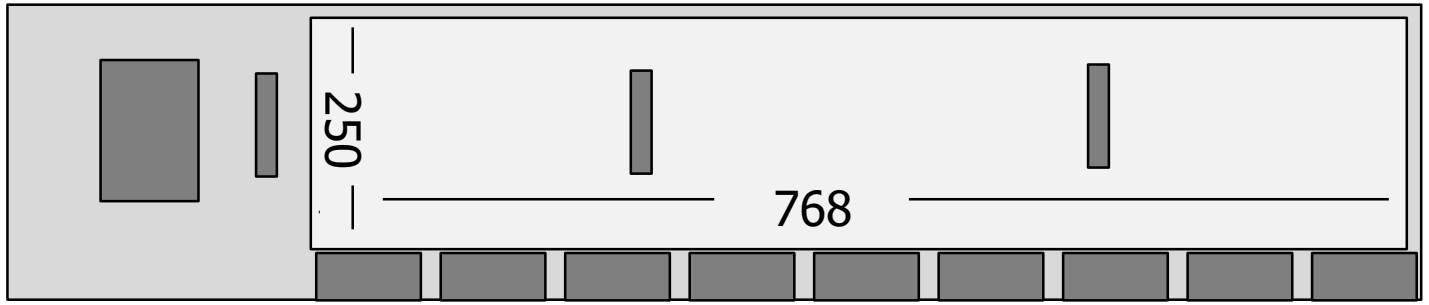
- Keep system/backend as much as possible as it is
- Main emphasis is low material, in particular for the inner layers (“PXD”)
- Goal: gain 5x (at least!) in occupancy to compensate for higher luminosity
  - Higher frame rate
  - Smaller pixels

- Possible improvements on pixel and module level
  - DEPFET pixel cell → better gq → thinner sensitive area
  - Periphery and interconnect on the module → higher frame rate
  - Module topology → speed
  - ASICs → speed, S/N, gated mode
  - Cooling system

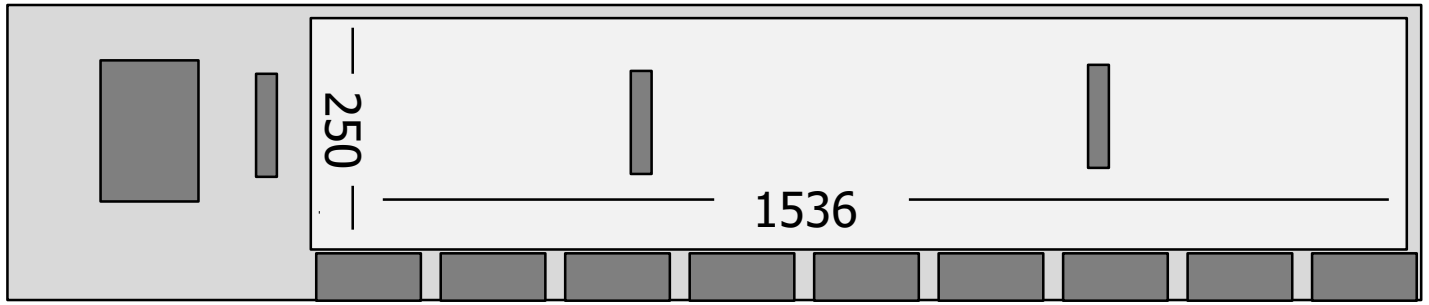
The basic idea – evolution rather than revolution



PXD2019
-: 1000 DCD channels
-: 192 SWB channels



3x speed
-: 3072 DCD channels
-: 62 SWB channels

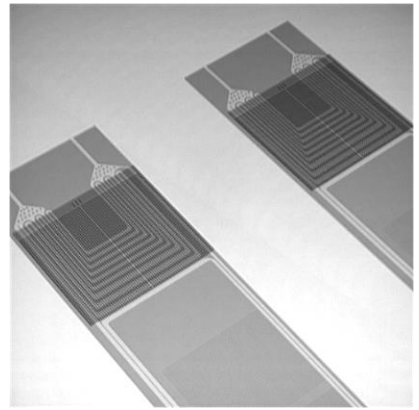


3x speed and 2x occupancy
-: 6144 DCD channels
-: 62 SWB channels

Another 2x possible with faster DCD! → 12x improvement occupancy, ~3µs per frame not science fiction

What do we need for this?

- Improvement of the metal system on the module → technology development planarization (started)
  - 3rd Alu layer
  - Possibly 2nd Cu layer



- Micro-channel cooling along the long balcony → see previous talks
  - Wafer bond technology to be installed at HLL

- New ASICs
  - DCD: smaller, more channels, less ADC bits, faster, driving capability …. → has to be slim, thin, small bump pitch …
  - SWB: improved driving capabilities, more channels .. → has to be thin, small bumps (material)
  - Do we need a module controller chip (off-module driver, sequencer ..)

- Assembly
  - Basically business as usual, bit of R&D for flip chipping of thin ASICs to balcony and thin sensitive region
  - Technology is under control

- Need to refine the concept, discuss, define R&D steps … we are not starting from scratch!