Ringberg DEPFET workshop 2019

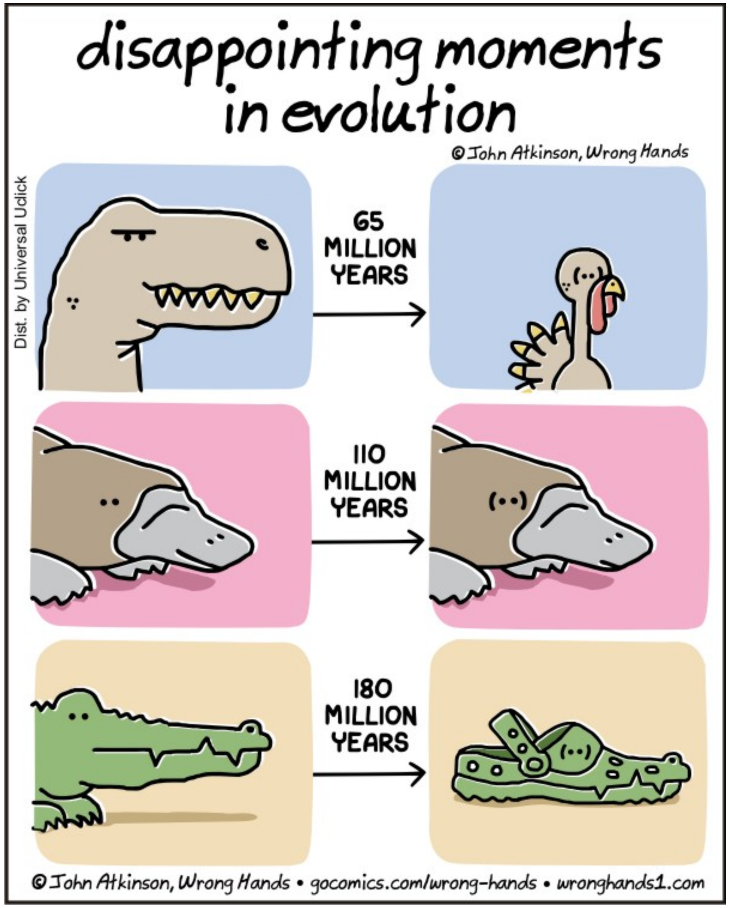
DEPFET devices - Conceptual evolution & the DEPFET device family tree

Ringberg, 11.3.2019

J. Treis on behalf of the MPG Semiconductor Lab

Contents:

- Outline of DEPFET evolution
- DEPFET family portrait

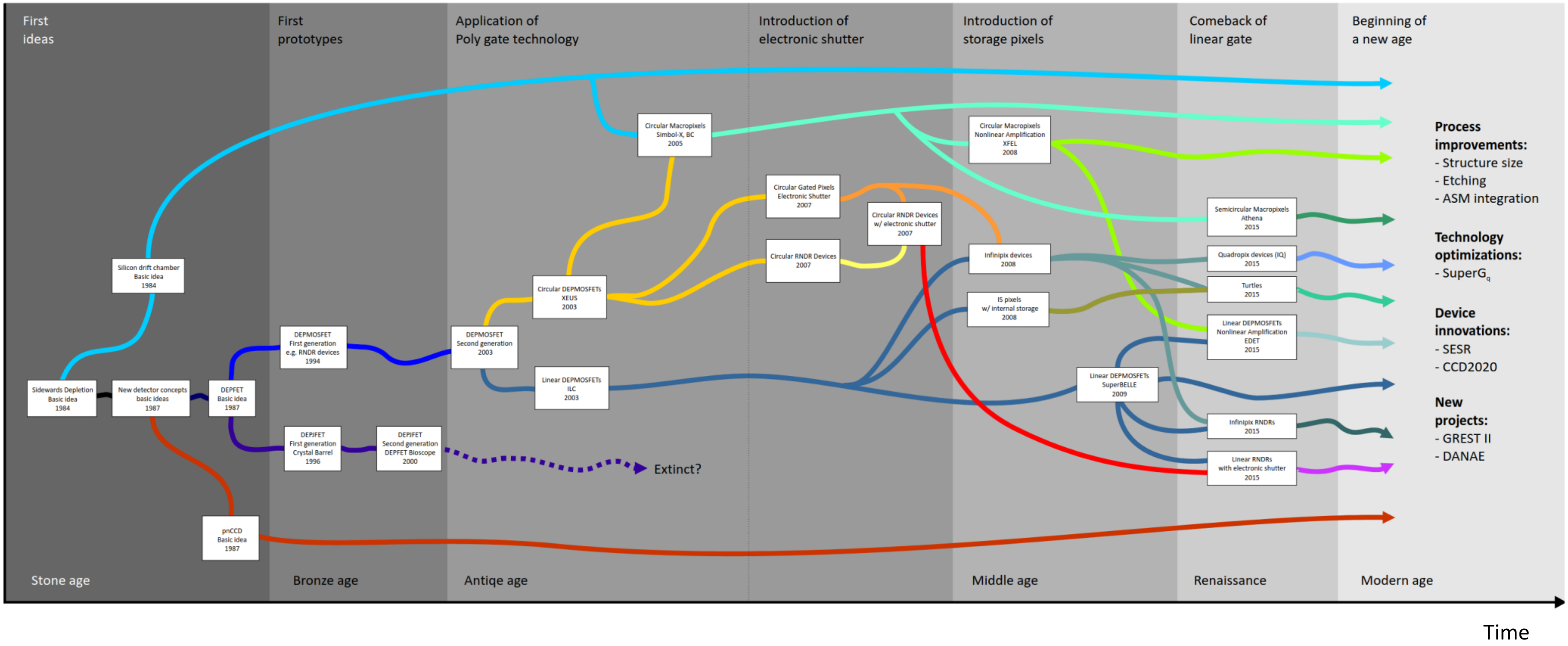


Part I

DEPFET evolutionary timeline

Dirk brings his family tree to class

Overview



Process improvements:
- Structure size
- Etching
- ASM integration

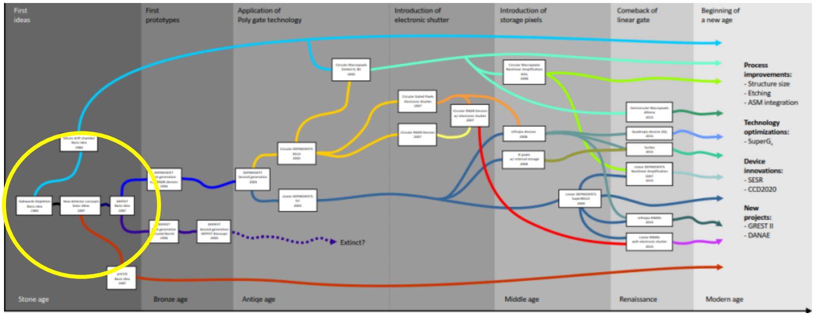
Technology optimizations:
- SuperG$_q$

Device innovations:
- SESR
- CCD2020

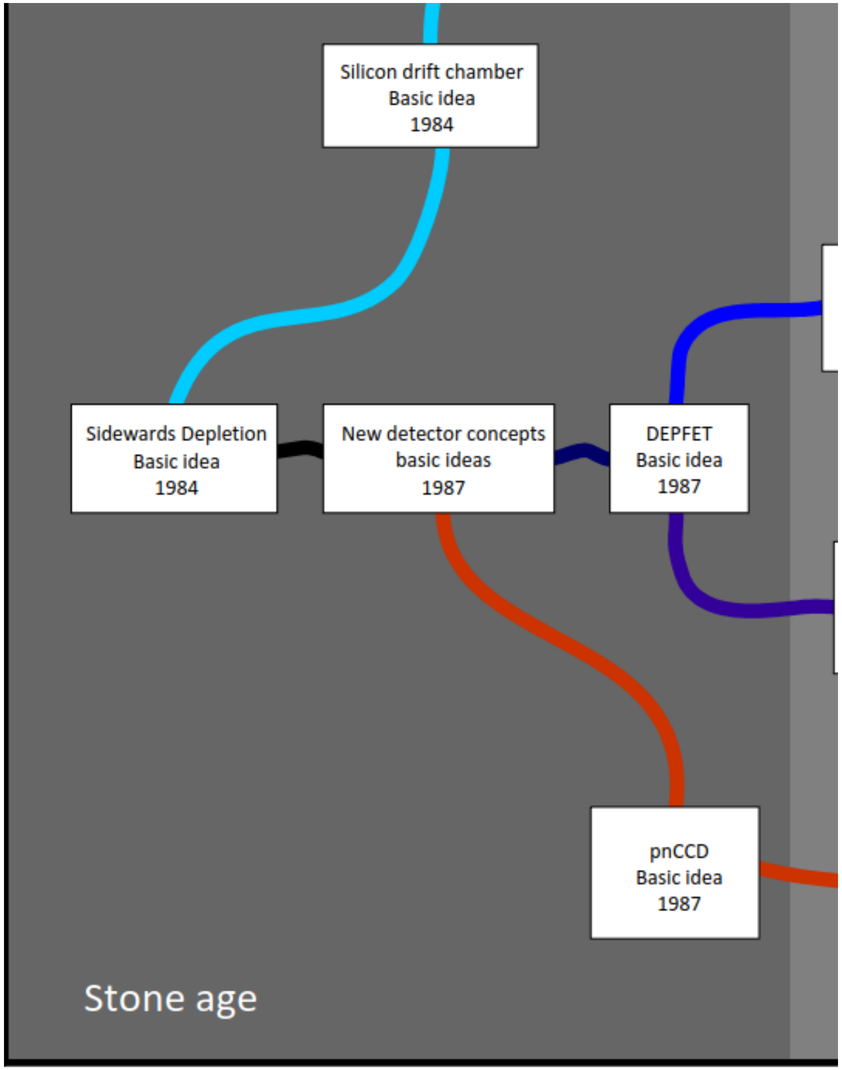
New projects:
- GREST II
- DANAE

The DEPFET evolutionary timeline
(as of 2019)

The beginnings



- DEPFET development based on two innovative papers
- Breakthrough in planar detector development



Silicon drift chamber
Basic idea
1984

Sidewards Depletion
Basic idea
1984

New detector concepts
basic ideas
1987

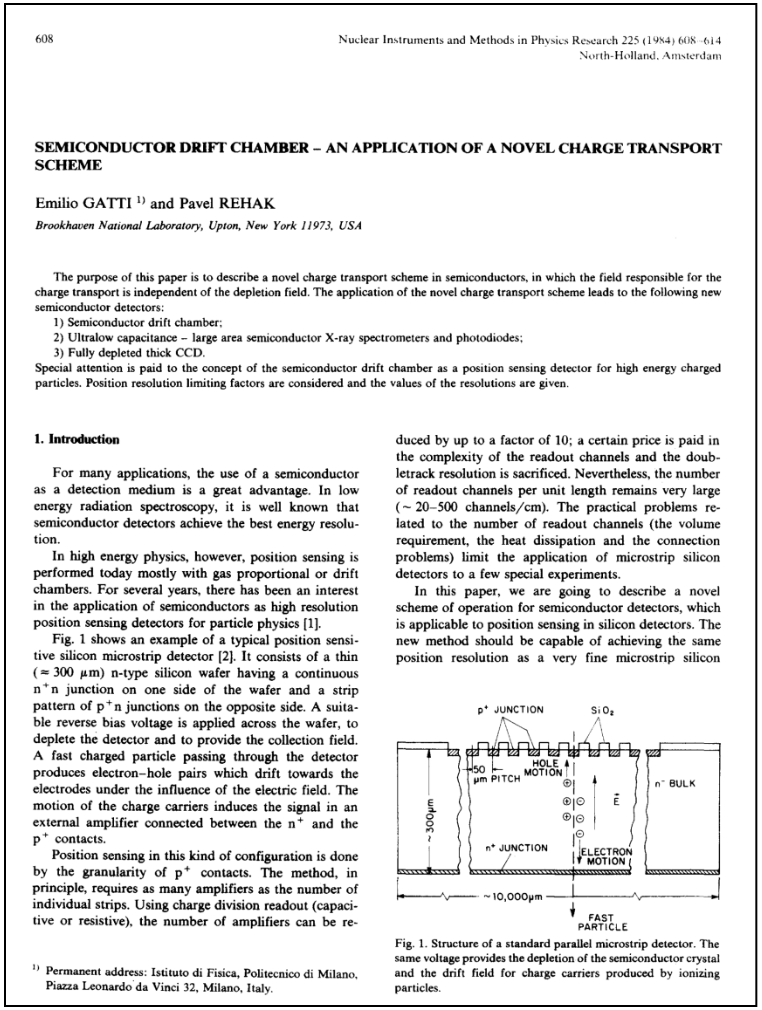
DEPFET
Basic idea
1987

pnCCD
Basic idea
1987

Stone age

The beginnings

Sidewards depletion
(1984)



608

Nuclear Instruments and Methods in Physics Research 225 (1984) 608–614
North-Holland, Amsterdam

SEMICONDUCTOR DRIFT CHAMBER – AN APPLICATION OF A NOVEL CHARGE TRANSPORT SCHEME

Emilio GATTI [1] and Pavel REHAK

Brookhaven National Laboratory, Upton, New York 11973, USA

The purpose of this paper is to describe a novel charge transport scheme in semiconductors, in which the field responsible for the charge transport is independent of the depletion field. The application of the novel charge transport scheme leads to the following new semiconductor detectors:

1) Semiconductor drift chamber;
2) Ultralow capacitance – large area semiconductor X-ray spectrometers and photodiodes;
3) Fully depleted thick CCD.

Special attention is paid to the concept of the semiconductor drift chamber as a position sensing detector for high energy charged particles. Position resolution limiting factors are considered and the values of the resolutions are given.

1. Introduction

For many applications, the use of a semiconductor as a detection medium is a great advantage. In low energy radiation spectroscopy, it is well known that semiconductor detectors achieve the best energy resolution.

In high energy physics, however, position sensing is performed today mostly with gas proportional or drift chambers. For several years, there has been an interest in the application of semiconductors as high resolution position sensing detectors for particle physics [1].

Fig. 1 shows an example of a typical position sensitive silicon microstrip detector [2]. It consists of a thin ($\approx 300\ \mu m$) n-type silicon wafer having a continuous n^+n junction on one side of the wafer and a strip pattern of p^+n junctions on the opposite side. A suitable reverse bias voltage is applied across the wafer, to deplete the detector and to provide the collection field. A fast charged particle passing through the detector produces electron–hole pairs which drift towards the electrodes under the influence of the electric field. The motion of the charge carriers induces the signal in an external amplifier connected between the n^+ and the p^+ contacts.

Position sensing in this kind of configuration is done by the granularity of p^+ contacts. The method, in principle, requires as many amplifiers as the number of individual strips. Using charge division readout (capacitive or resistive), the number of amplifiers can be reduced by up to a factor of 10; a certain price is paid in the complexity of the readout channels and the doubletrack resolution is sacrificed. Nevertheless, the number of readout channels per unit length remains very large (~ 20–500 channels/cm). The practical problems related to the number of readout channels (the volume requirement, the heat dissipation and the connection problems) limit the application of microstrip silicon detectors to a few special experiments.

In this paper, we are going to describe a novel scheme of operation for semiconductor detectors, which is applicable to position sensing in silicon detectors. The new method should be capable of achieving the same position resolution as a very fine microstrip silicon

Fig. 1. Structure of a standard parallel microstrip detector. The same voltage provides the depletion of the semiconductor crystal and the drift field for charge carriers produced by ionizing particles.

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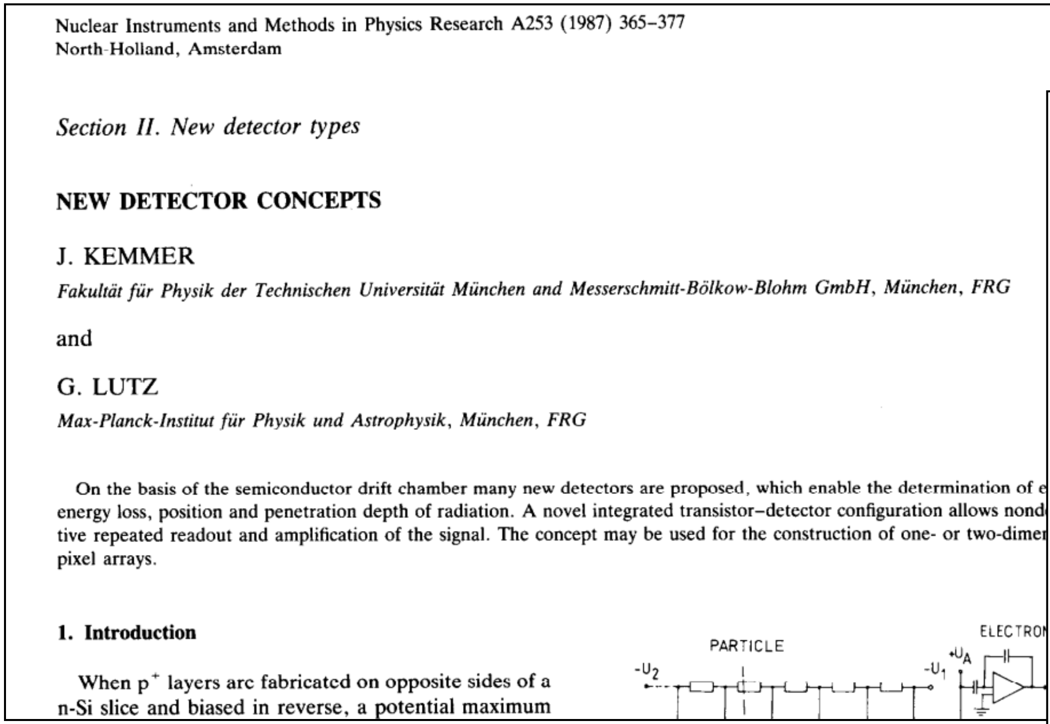
[1] Permanent address: Istituto di Fisica, Politecnico di Milano, Piazza Leonardo da Vinci 32, Milano, Italy.

The beginnings



Nuclear Instruments and Methods in Physics Research A253 (1987) 365–377
North-Holland, Amsterdam

365

Section II. New detector types

NEW DETECTOR CONCEPTS

J. KEMMER

Fakultät für Physik der Technischen Universität München and Messerschmitt-Bölkow-Blohm GmbH, München, FRG

and

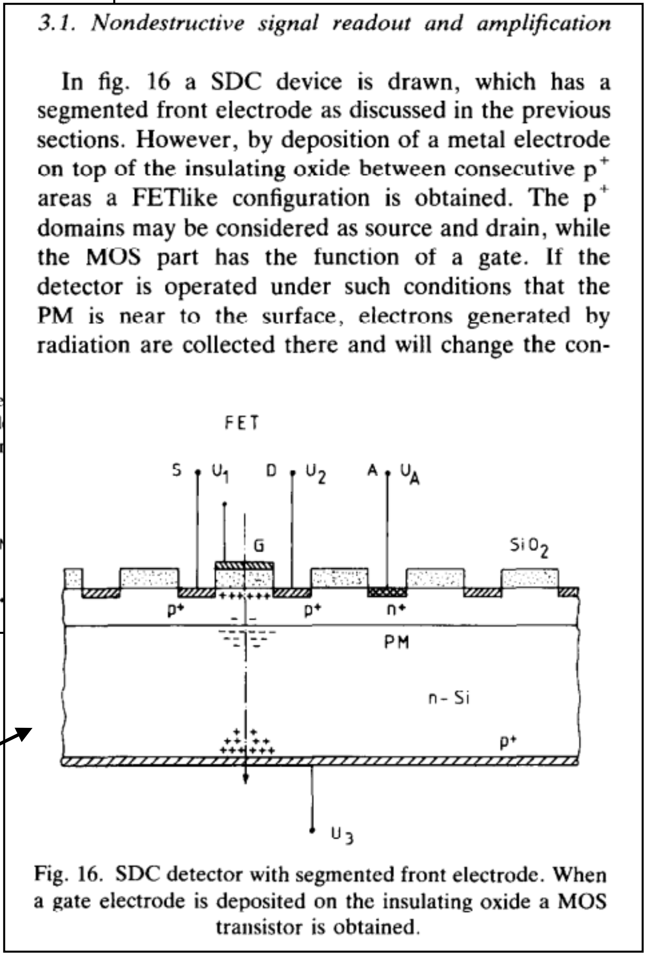
G. LUTZ

Max-Planck-Institut für Physik und Astrophysik, München, FRG

On the basis of the semiconductor drift chamber many new detectors are proposed, which enable the determination of e
energy loss, position and penetration depth of radiation. A novel integrated transistor–detector configuration allows nond
tive repeated readout and amplification of the signal. The concept may be used for the construction of one- or two-dimer
pixel arrays.

1. Introduction

When p^+ layers are fabricated on opposite sides of a n-Si slice and biased in reverse, a potential maximum



3.1. Nondestructive signal readout and amplification

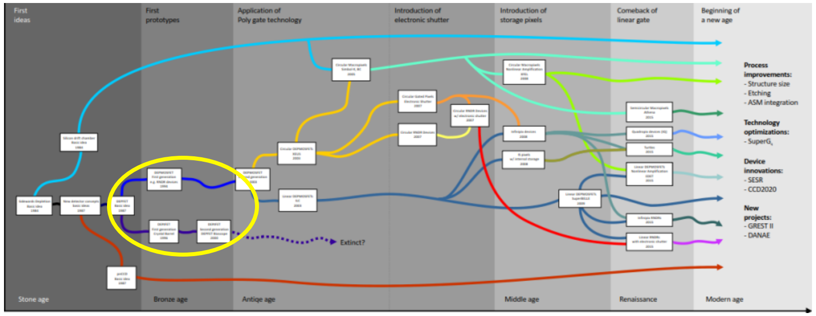
In fig. 16 a SDC device is drawn, which has a segmented front electrode as discussed in the previous sections. However, by deposition of a metal electrode on top of the insulating oxide between consecutive p^+ areas a FETlike configuration is obtained. The p^+ domains may be considered as source and drain, while the MOS part has the function of a gate. If the detector is operated under such conditions that the PM is near to the surface, electrons generated by radiation are collected there and will change the con-

Fig. 16. SDC detector with segmented front electrode. When a gate electrode is deposited on the insulating oxide a MOS transistor is obtained.

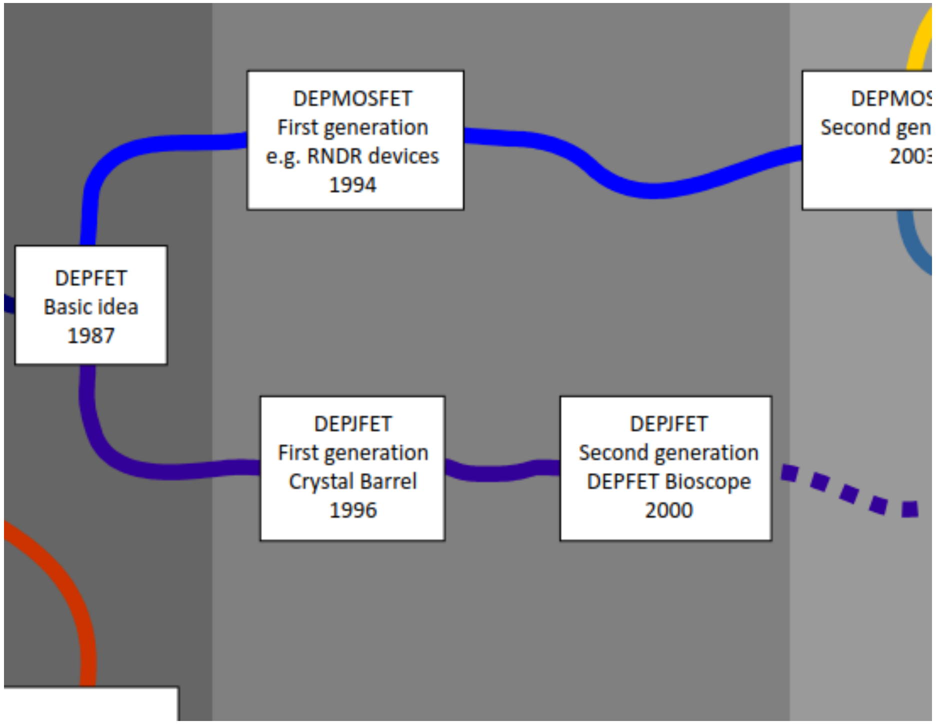
P. 370:
First published drawing of a
DEP(MOS)FET

New detector concepts
(1987)

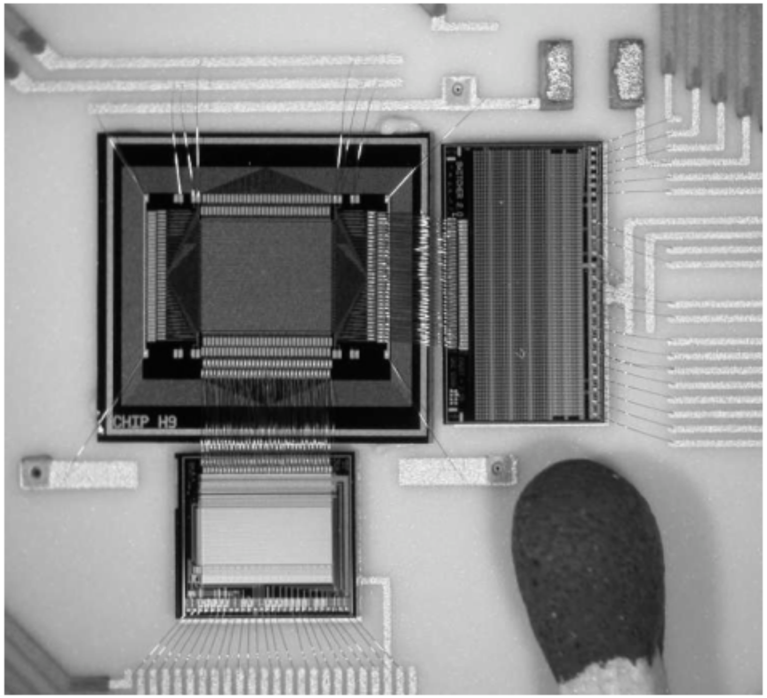
Early pioneers

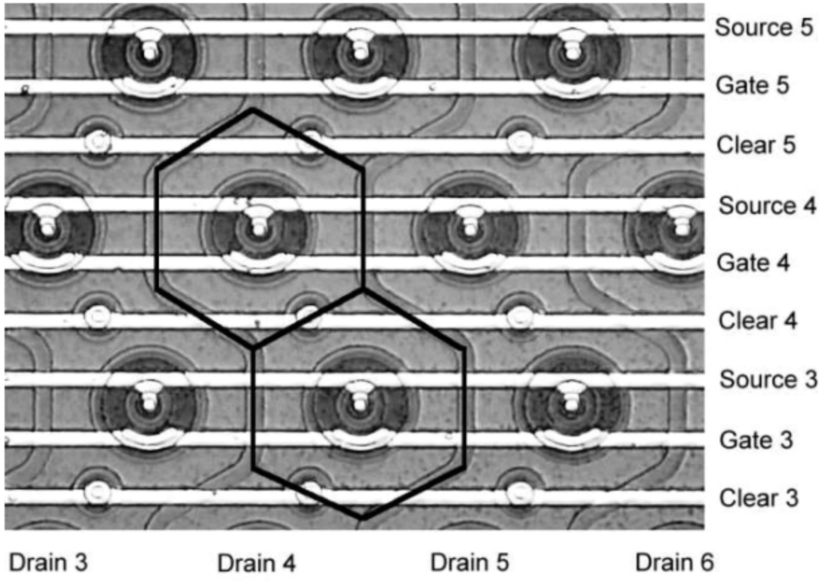


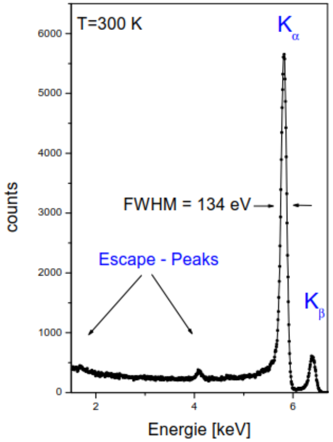
- First DEPMOSFETs in Metal-gate technology
- JFETs for HEP use
- JFETS for autoradiography
- JFET development discontinued until today (extinct?)

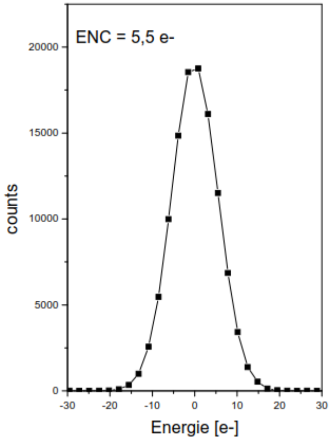


Early pioneers

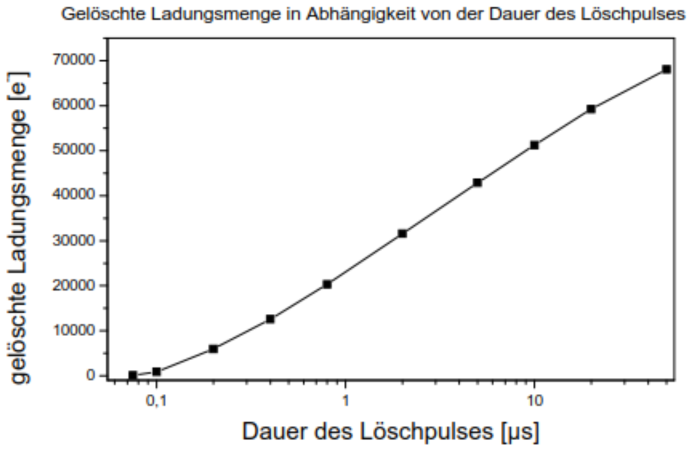


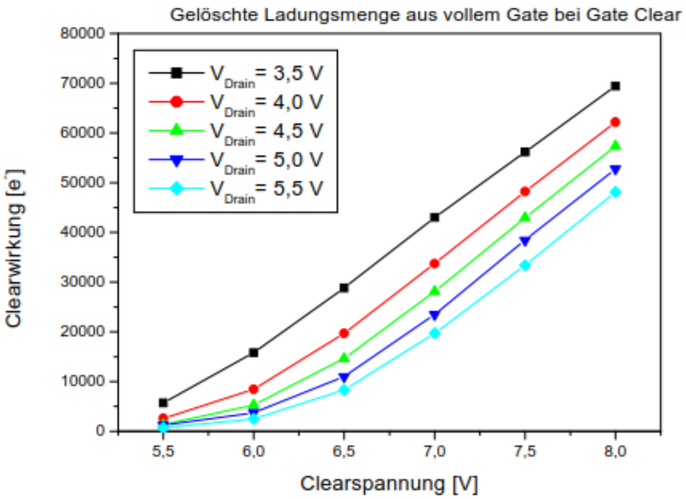


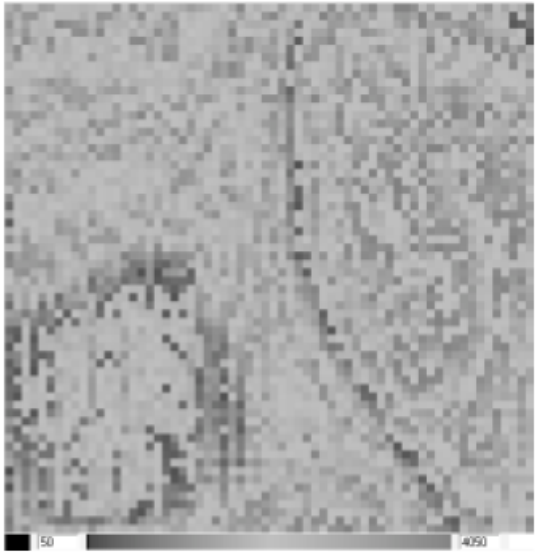




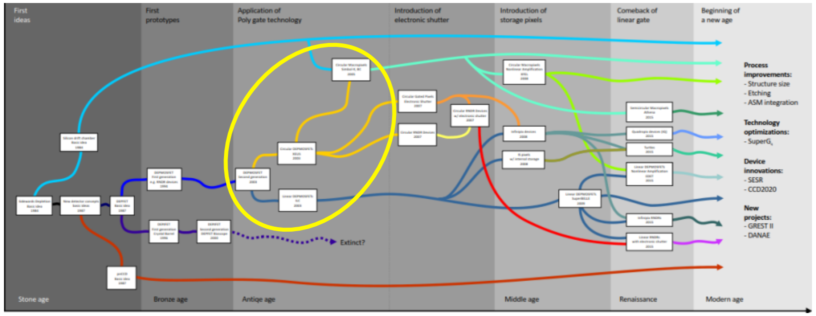
Early pioneers



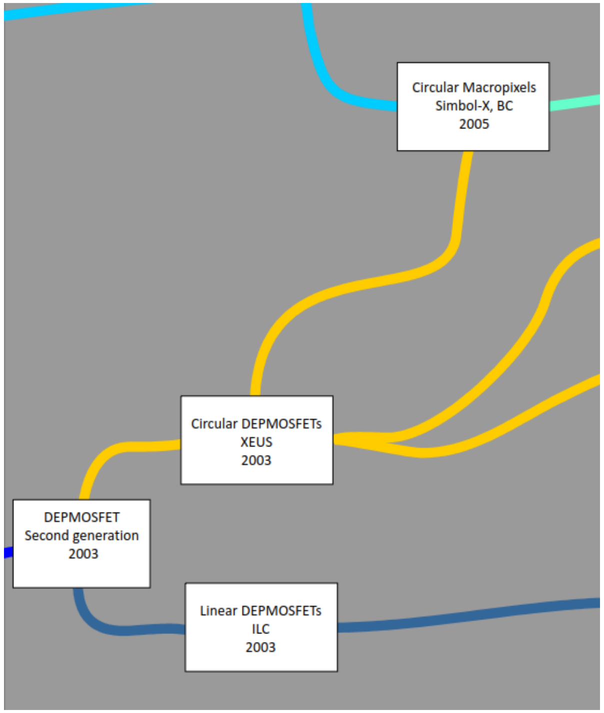




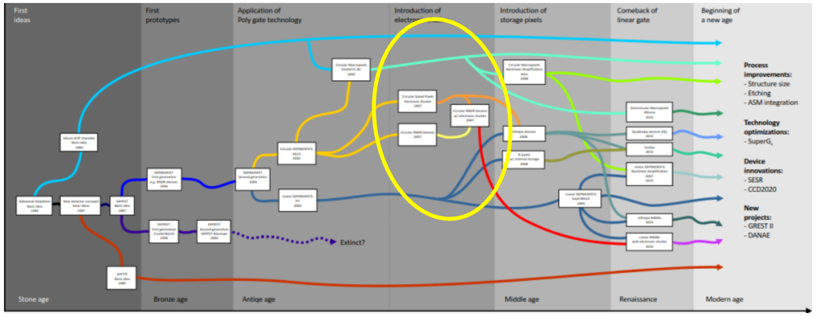
The classical era



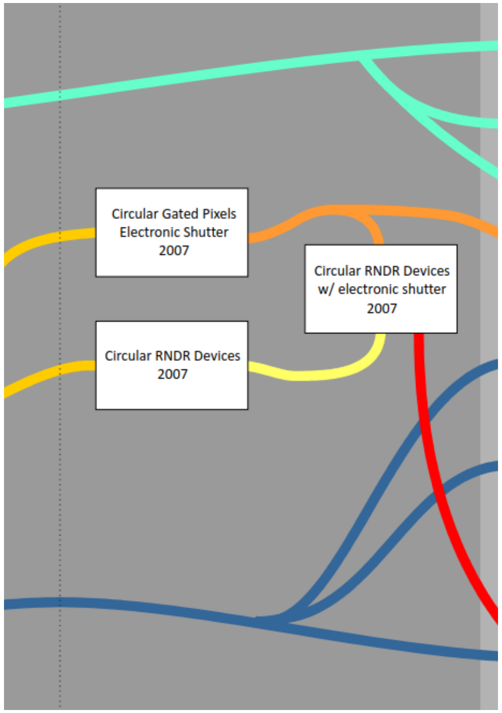
- Invention of double-poly technology
- DEPMOSFET devices
- Linear topology for
  - Small pixels
  - tracking applications (ILC)
- Circular topology for
  - X-ray imaging spectroscopy
- Macropixels



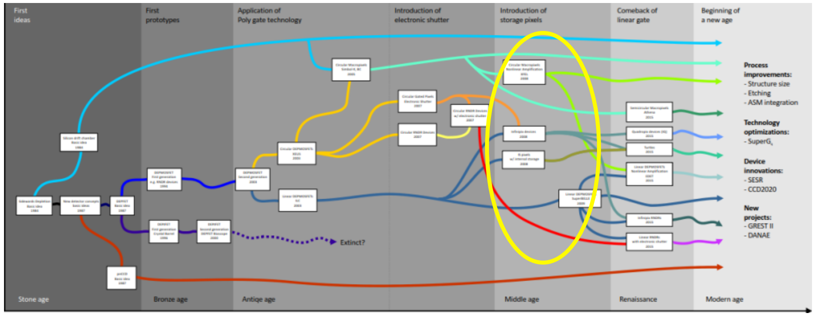
The neo-classical era



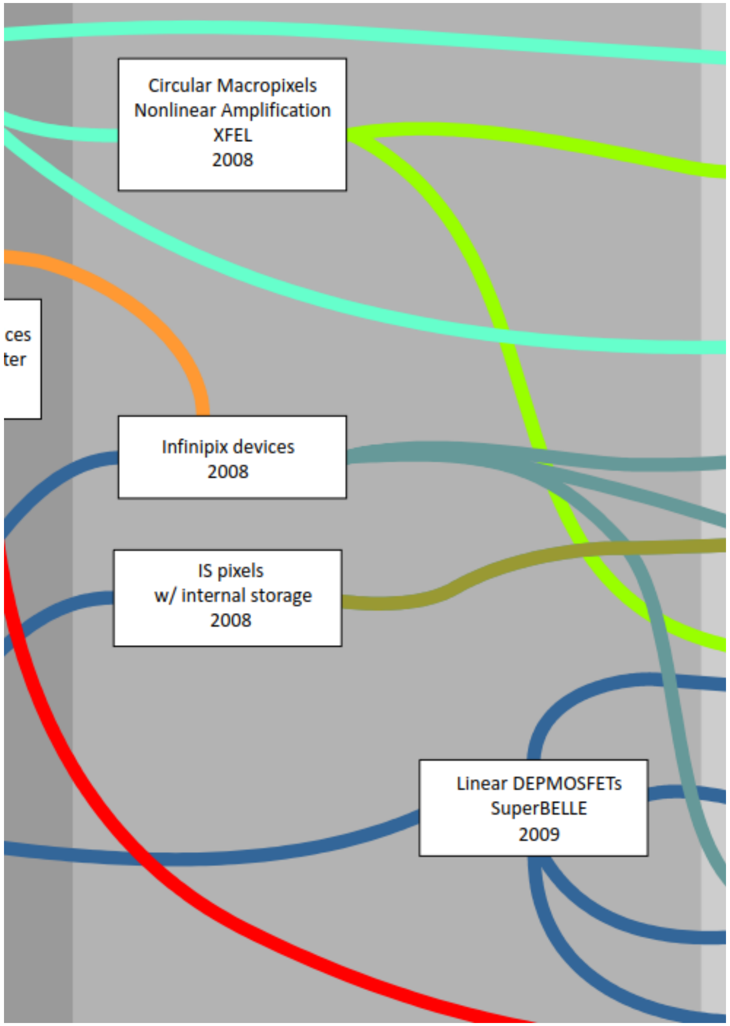
- Advent of electronic shutter
- Revival of RNDR structures
- Combination of concepts



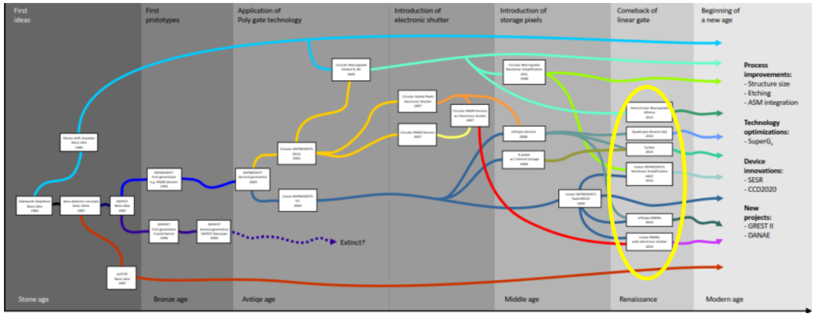
New solutions



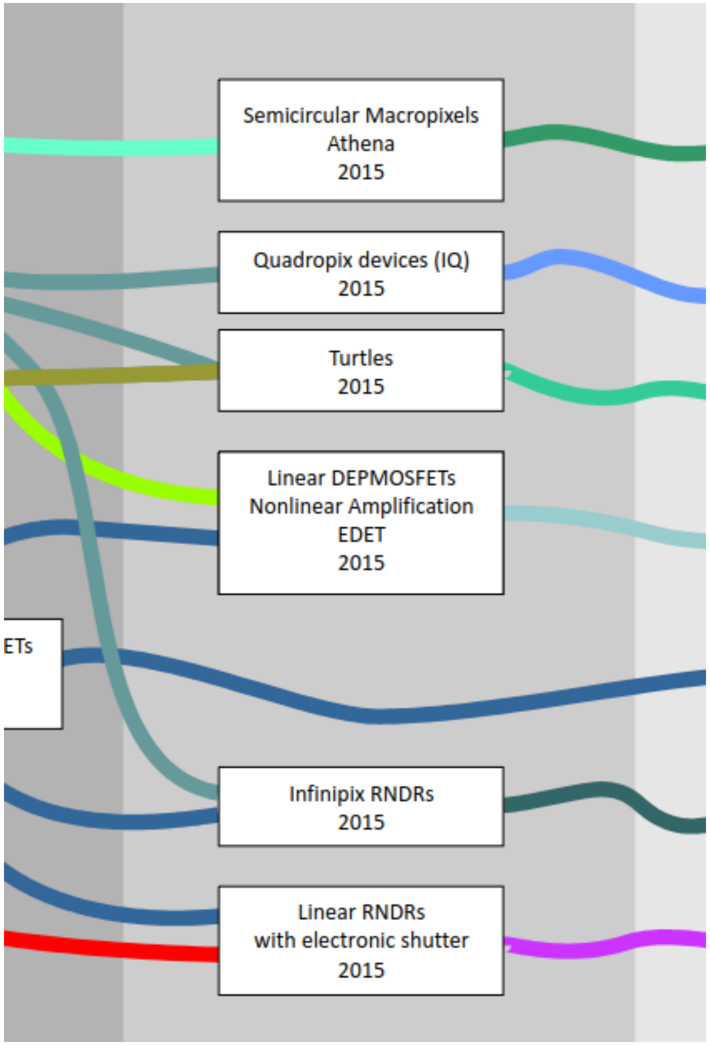
- Introduction of nonlinear amplification / in-sensor compression
- First multigate and internal storage pixels
- New energy for linear DEPFET development



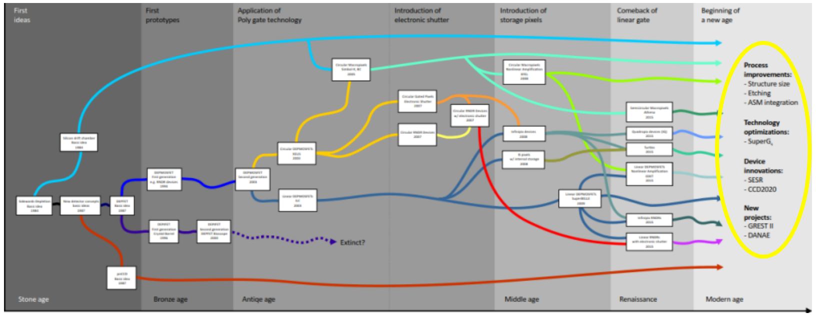
Today



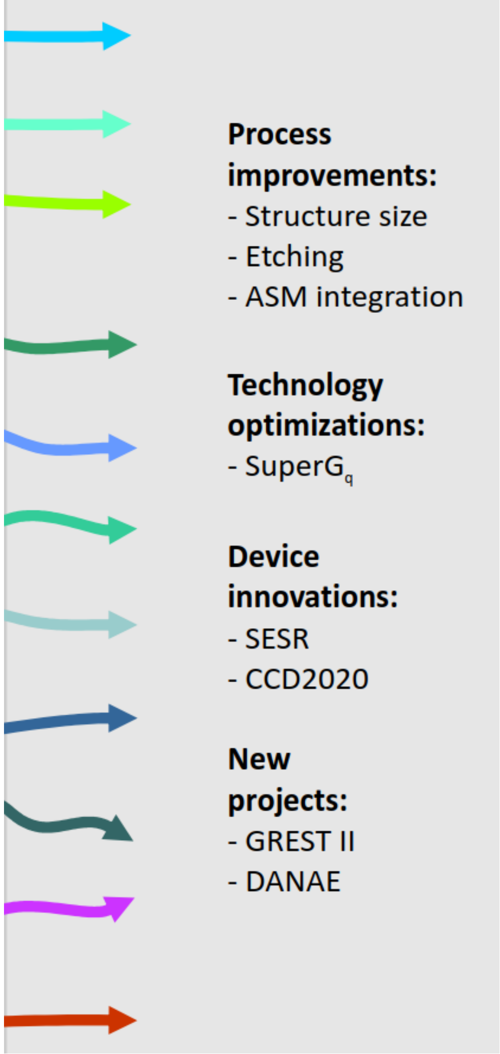
- Renaissance of the linear gates for spectroscopy
- Higher-order multigate structures
- Linear DEPFETs with nonlinear amplification
- Combinatorial devices



The future



- Variety of new technology & device ideas
- DEPFET based devices with unprecedented performance and capabilities
- Competition from
  - CMOS
  - SOI
  - DEPFET Competitors
- Exciting times ahead



Process improvements:
- Structure size
- Etching
- ASM integration

Technology optimizations:
- SuperG$_q$

Device innovations:
- SESR
- CCD2020

New projects:
- GREST II
- DANAE

Part II

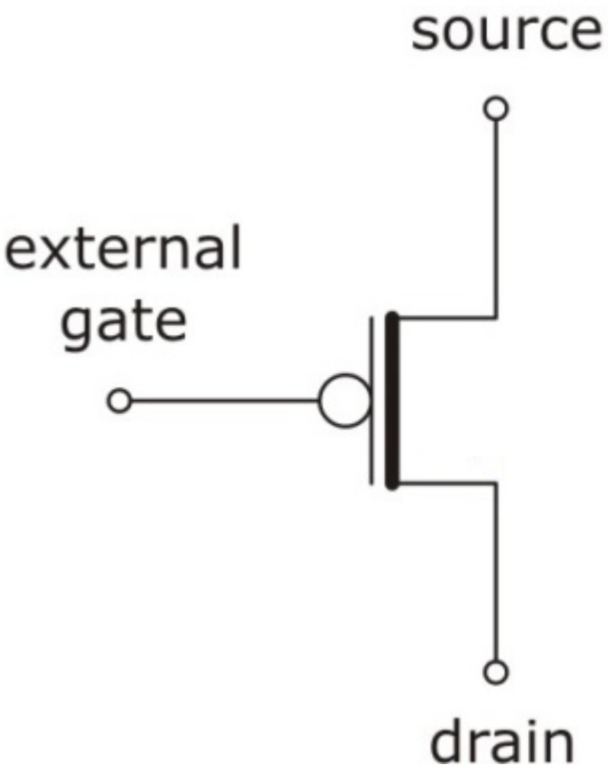
DEPFET family portait

Optimizations

All modifications made for the purpose of

- **Improving DEPFET performance**
- **Adding additional capabilities**
- **Making DEPFET a more versatile tool for experiments**

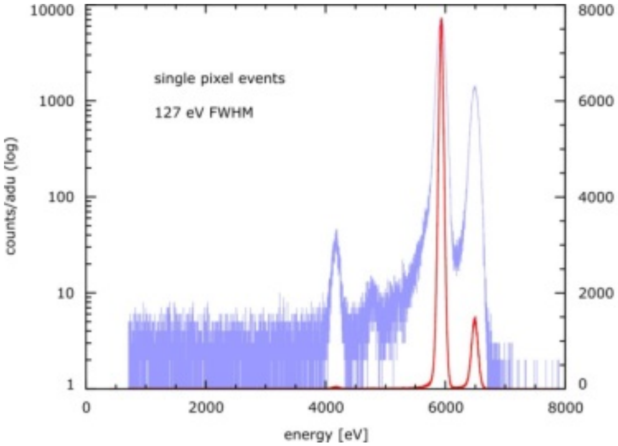
The "classical" DEPFETs

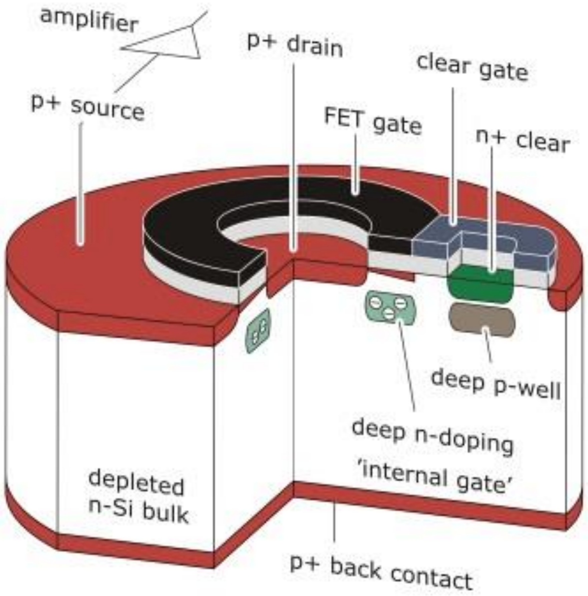


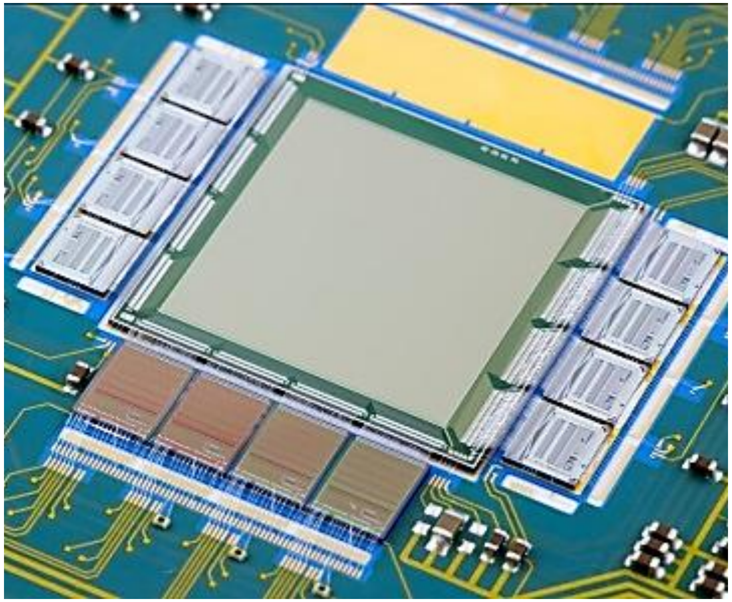
The "classical" DEPFETs

Circular topology:

- Large pixels > 75 µm^2
- Noise ~ 4 e- ENC
- Efficient filling of area
- W/L fixed
- X-ray imaging spectroscopy
- XEUS, IXO



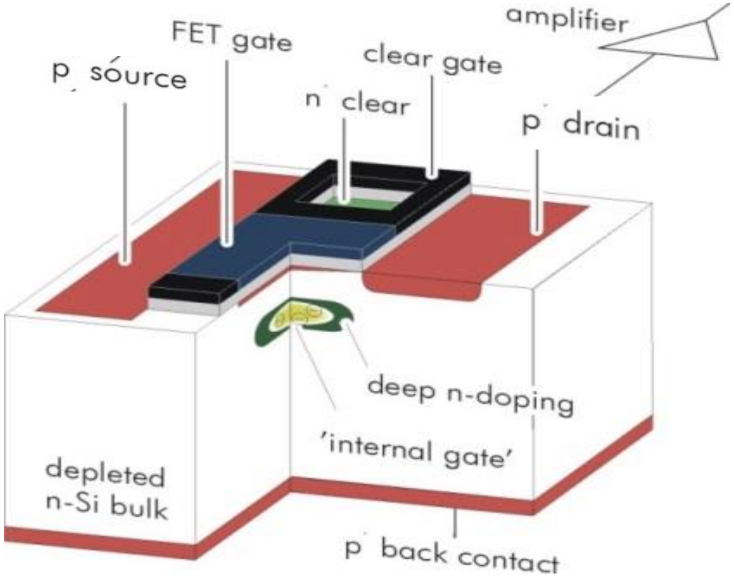


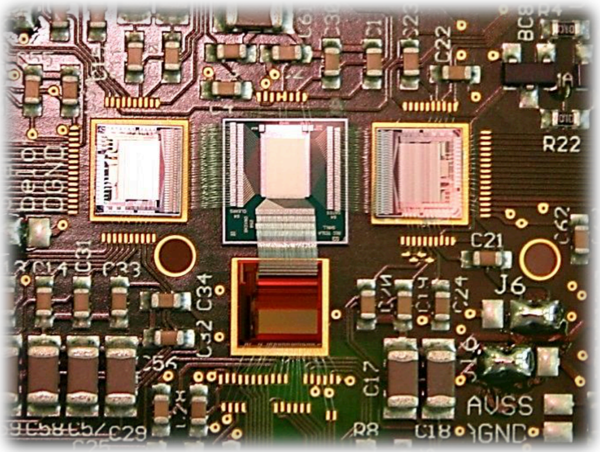


The "classical" DEPFETs

Linear topology:

- Small pixels > 25 µm^2
- Scalable W/L
- High packing density
- Highly array compatible
- Many shared contacts
- "Pixel couple" structure
- Optimized for fast readout due to
    - Drain current readout
    - Multiparallel readout

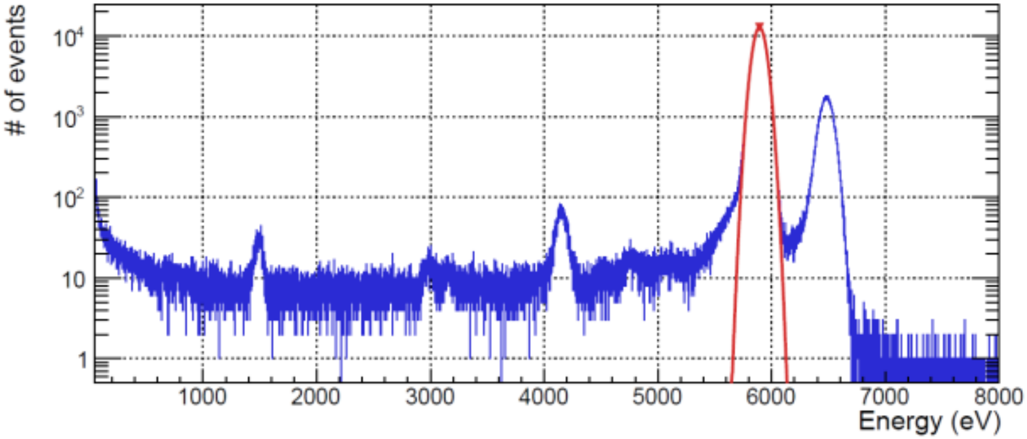


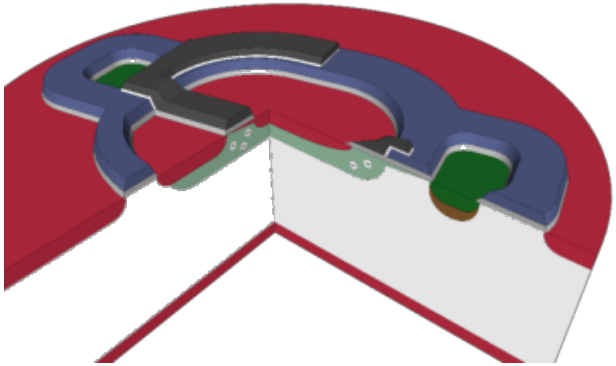


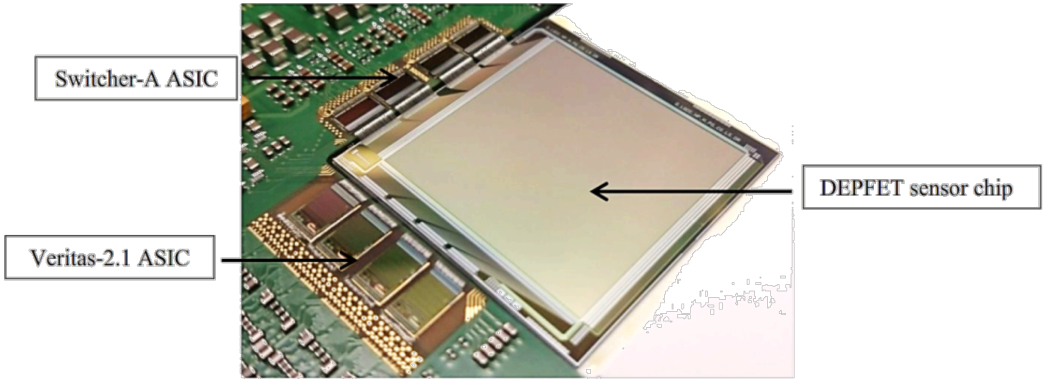
Semicircular DEPFET

Semicircular DEPFET

- Combine advantage from linear and circu device
- Scalable gate length
- Large pixels > 150 µm²
- Noise ~ 1.5 e- ENC
- Great spectroscopic performance
- Macropixel compatible

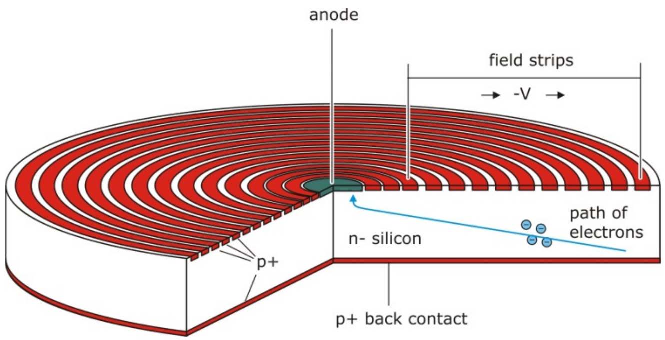






Measurement: W. Trebersburg, MPE

Some Arithmetics



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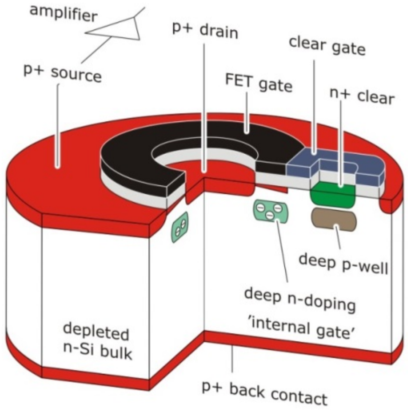

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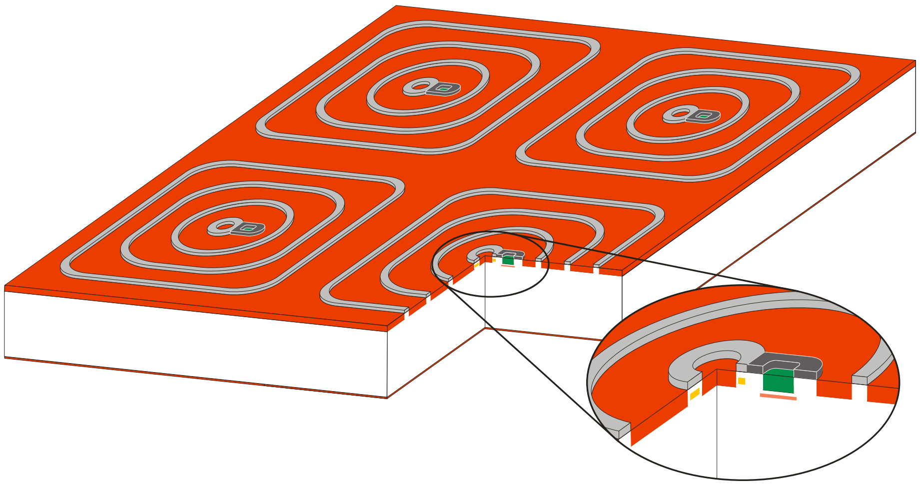
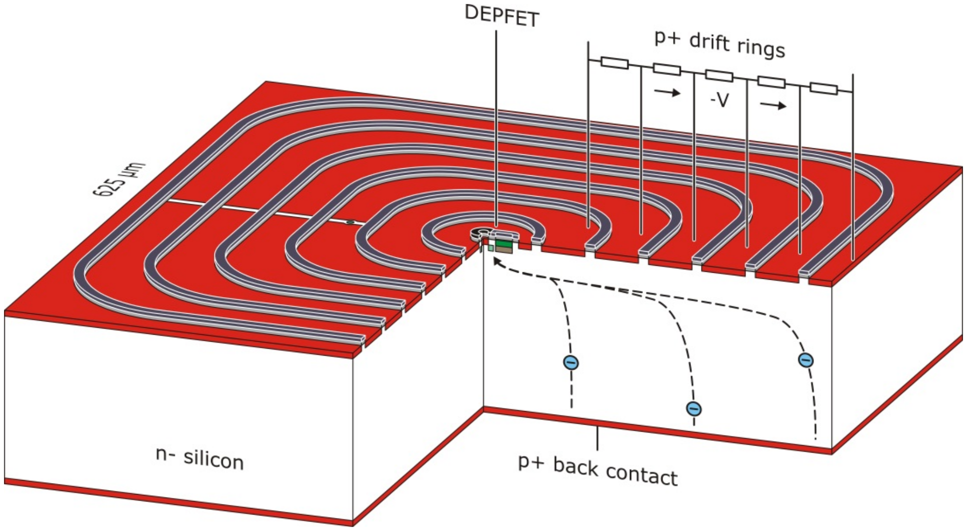
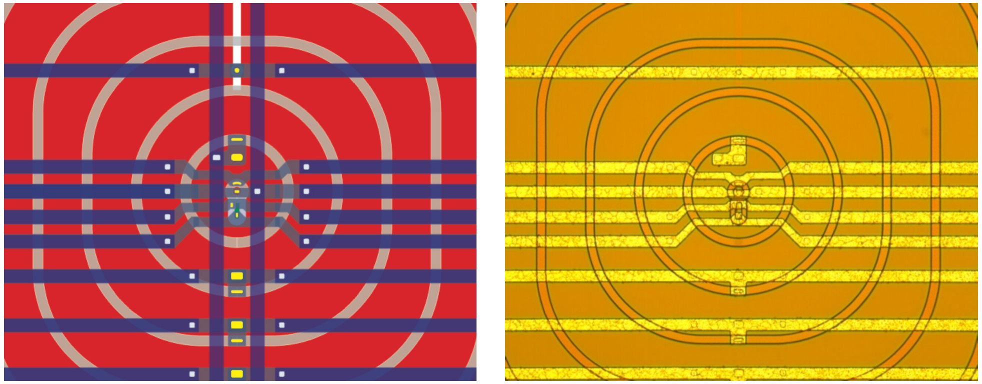


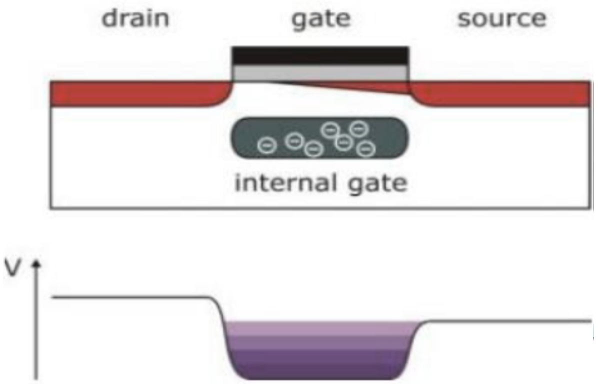
DEPFET Macropixel devices

- *Macro Pixel Detector (MPD)*
  - SDD & DePFET
    - ↳ **large area & low noise**
  - common backside diode & bulk
    - ↳ **thin entrance window**
    - ↳ **fill factor 1**
  - individually addressable pixels
    - ↳ **flexible readout**
    - ↳ **windowing**
  - Array readout scheme
    - ↳ **same as for “normal” pixels**
  - 1 active row, other pixels off
    - ↳ **low power consumption**
  - column parallel operation
    - ↳ **fast processing**





New requirement: High dynamic range!



Internal amplification

gq = dI/dQsig

for a given transistor :

gq ~ channel carrier velocity

gq ~ fraction of mirror charge

influenced in the channel by Qsig < 1

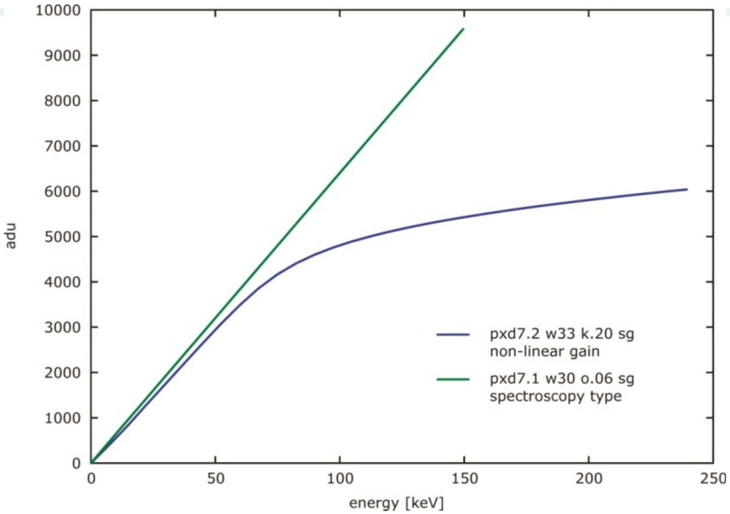
Multiple n-implants to create

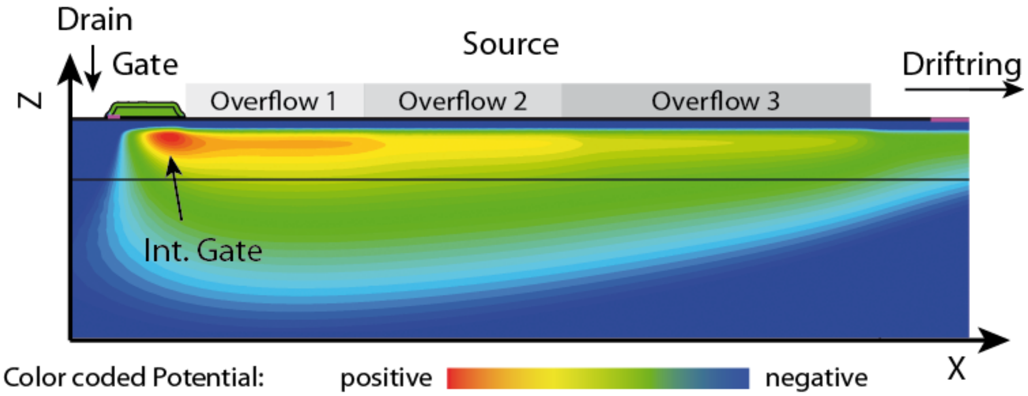
an electric field towards the Internal Gate

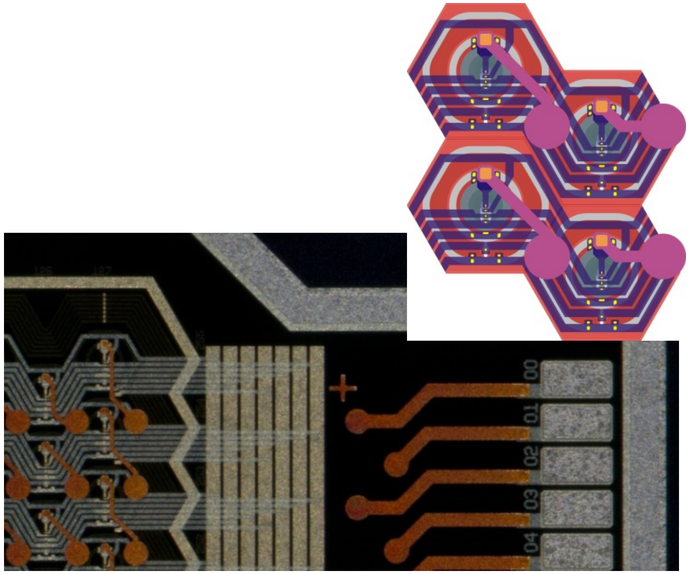
and to tailor the response

DEPFETs with signal compression

- The internal gate extends into the region below the source
- Small signals collected directly below the channel
  - ↳ Most effective, large signal
- Large signals spill over into the region below the source
  - ↳ Less effective, smaller signal
- staggered potential inside internal gate by varying impl. doses



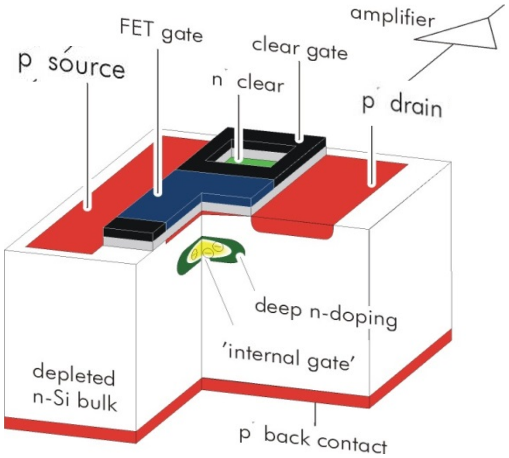




Linear nonlinear DEPFET Pixel

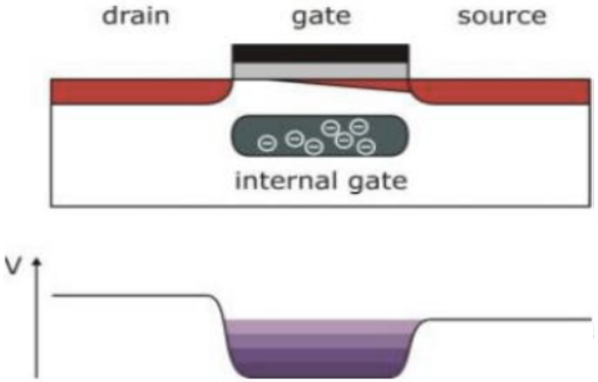
DEPFET integrated amplifier

- p-channel FET on depleted n-bulk
- Signal charge collected in potential minimum below FET channel
- **"Internal gate"**
- FET current modulation ≥ 300 pA/el.
- Reset via clearFET
- Low capacitance & noise
- Charge storage, readout on demand
- Rolling shutter mode



EDET pixels:

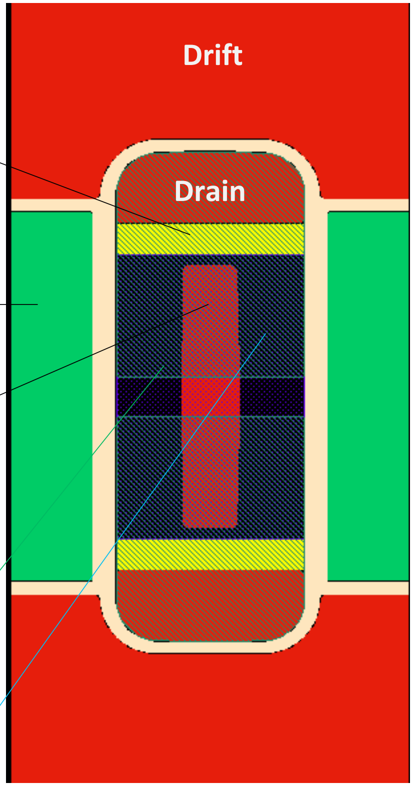
- Dynamic range problem
- Implement signal compression in pixel
- Overflow to source to tailor dynamic range



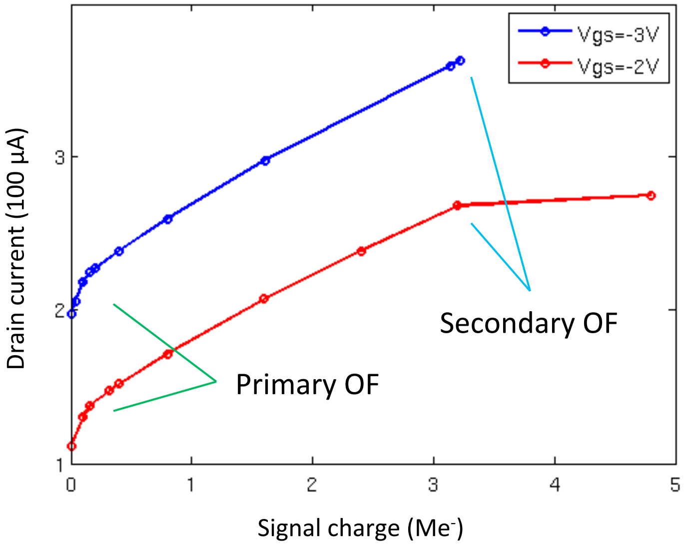
Linear nonlinear DEPFET Pixel

EDET pixels:

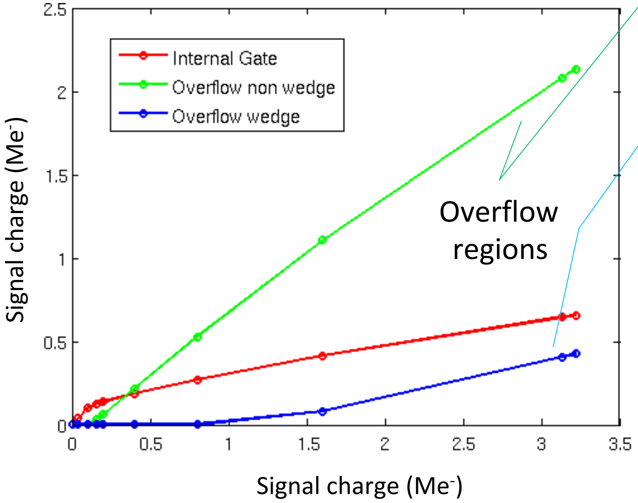
- Shape of source implant creates 2 overflow regions
- Different onset points of overflow
- Large dynamic range
- Sensor w/ integrated signal compression



No additional deep-n drift field by wedge shape

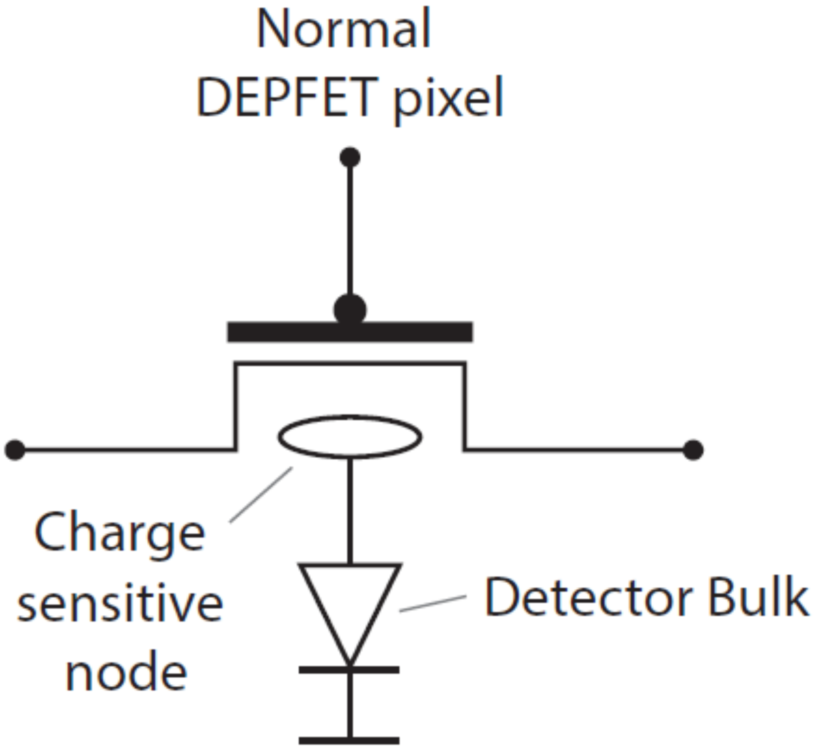


Response curve (V_{DS} = -5 V)

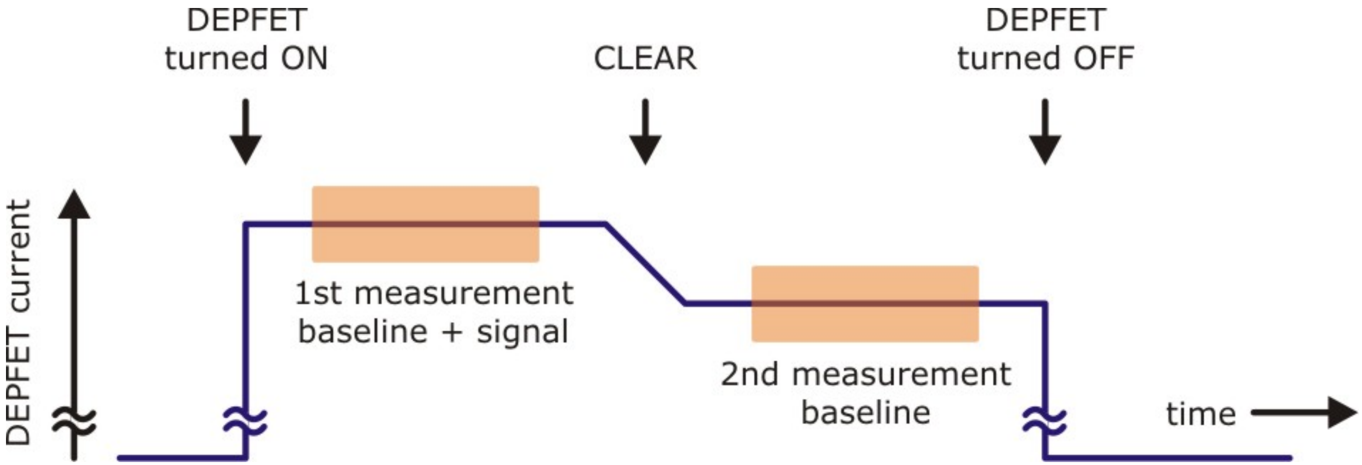


Charge distribution (VGS = -3 V, VDS = -5 V)

Limitations of the "classical" DEPFET

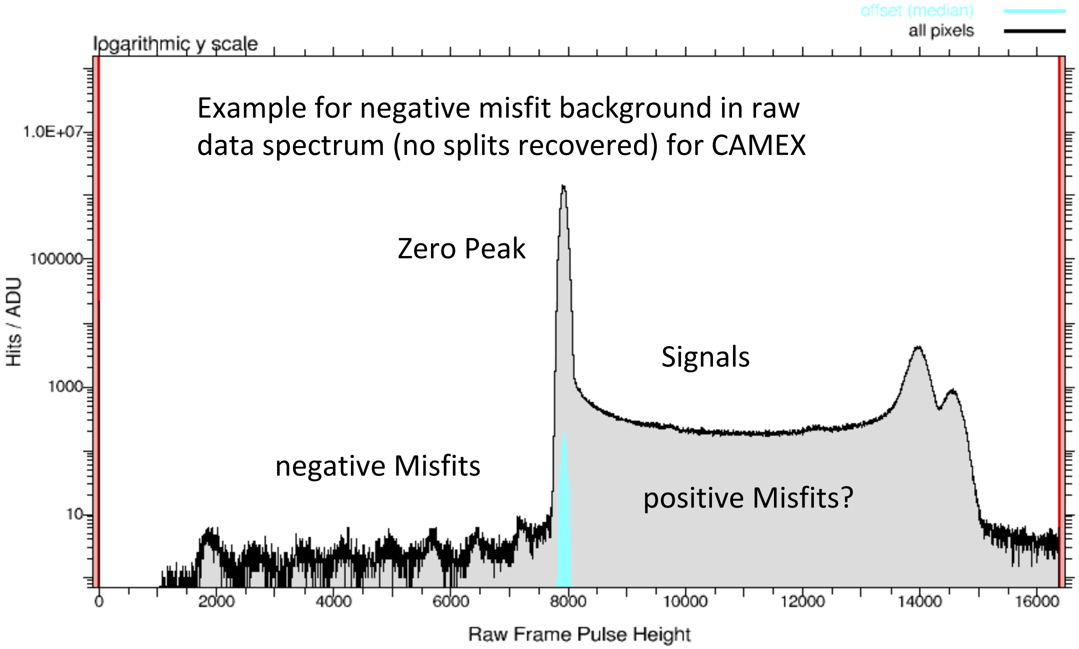


Problem I: Misfits

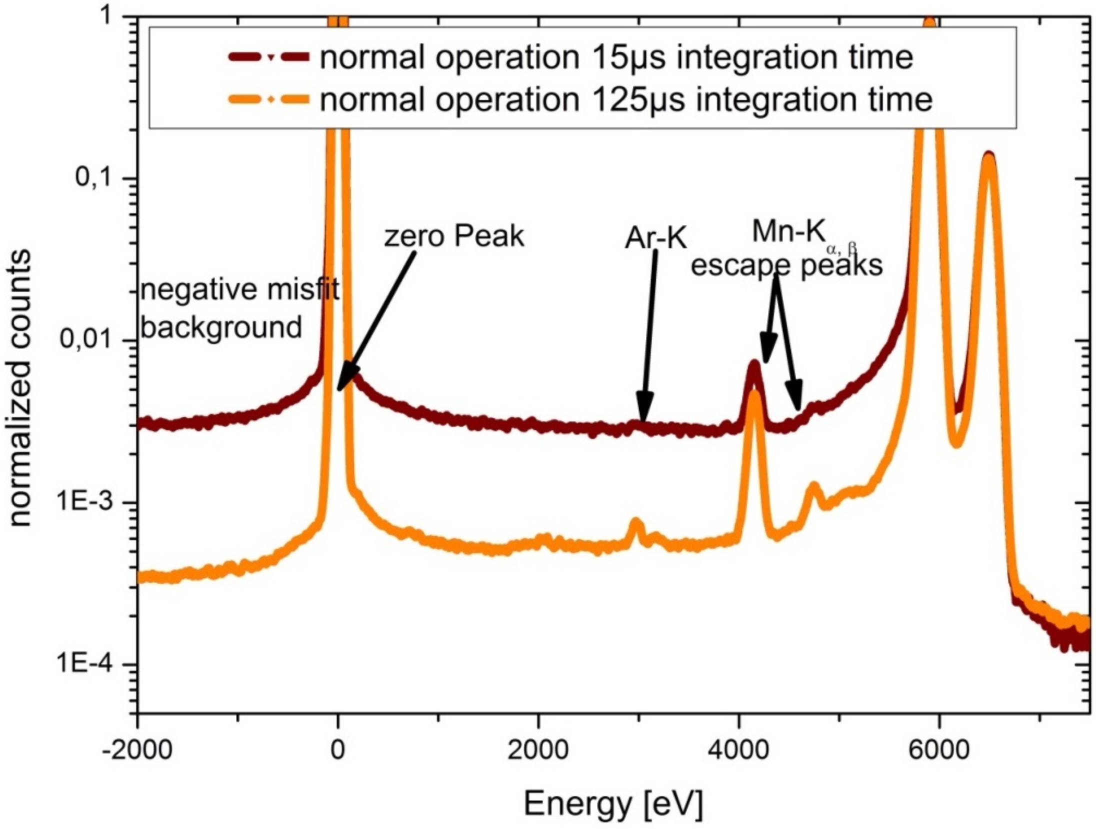


Measurement of signal:

- Measure signal levels
- Measure „mean values“ both before and after clear
- Calculate the difference of mean values = „charge Signal“
- DEPFET is permanently sensitive
- Hit during evaluation phase distorts signal



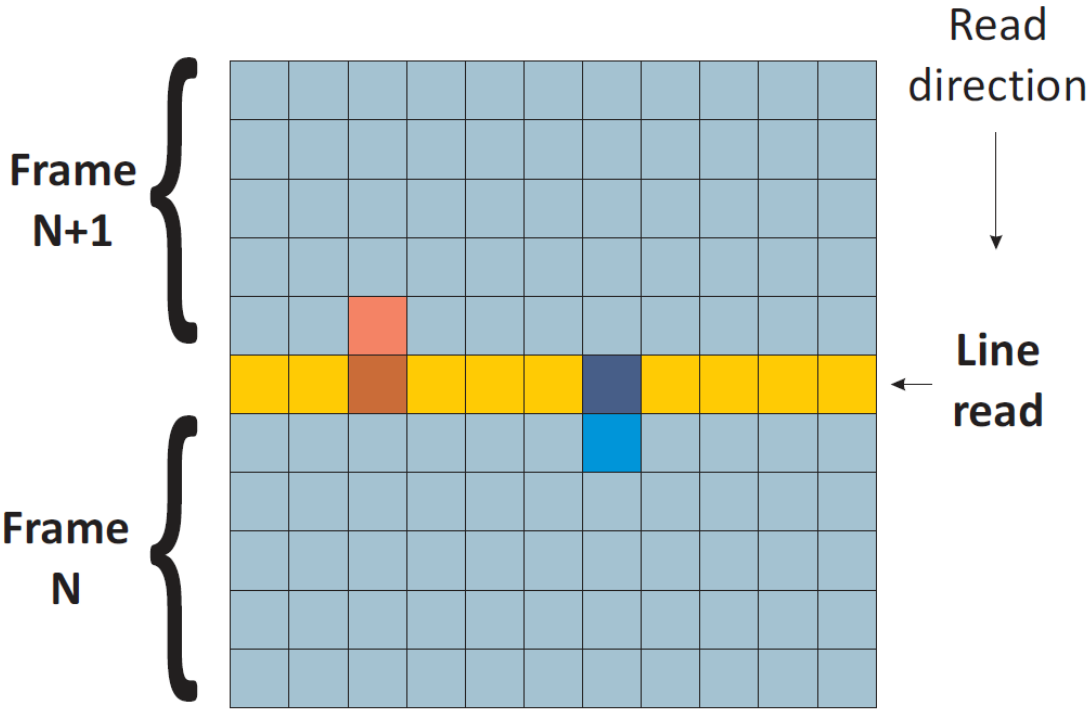
Problem I: Misfits



Signal processing of 4.2µs:

- P/B = 280, FWHM = 129 eV @ 15 µs signal integration
- P/B = 1600, FWHM = 133 eV @ 125 µs signal integration

Problem II: Broken patterns



- **Broken patterns** due to rolling shutter effect
- "Lost" split partners / allocated to different frames
- Pattern split "in time" instead of space
- **Red case:** Positive misfit causes broken pattern
- **Blue case:** Negative misfit causes broken pattern

Solution: Electronic shutter

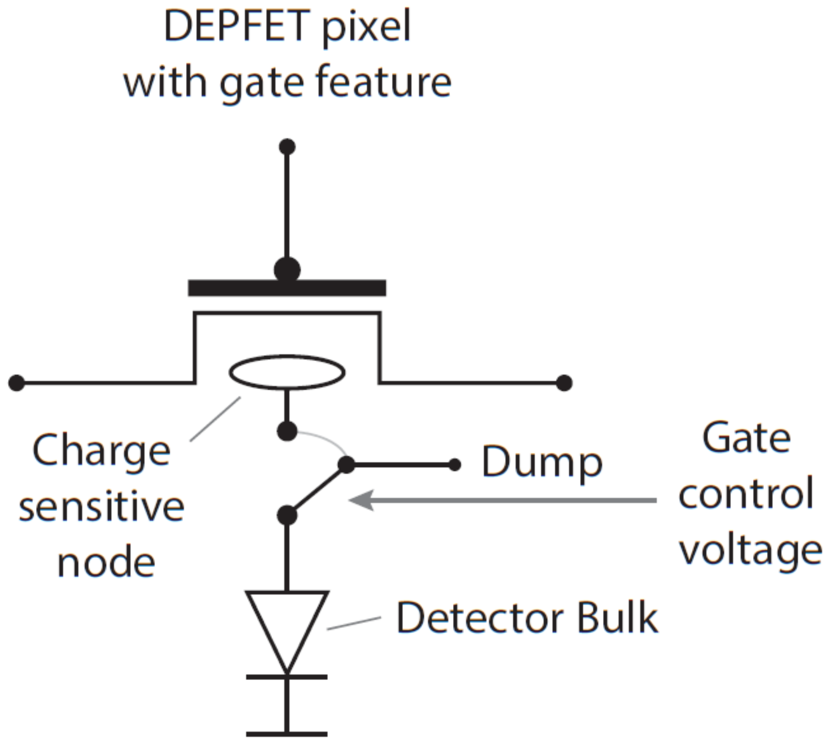
Turn off sensitivity of DEPFET during readout

Dump unwanted bulk generated charge to dedicated electrode

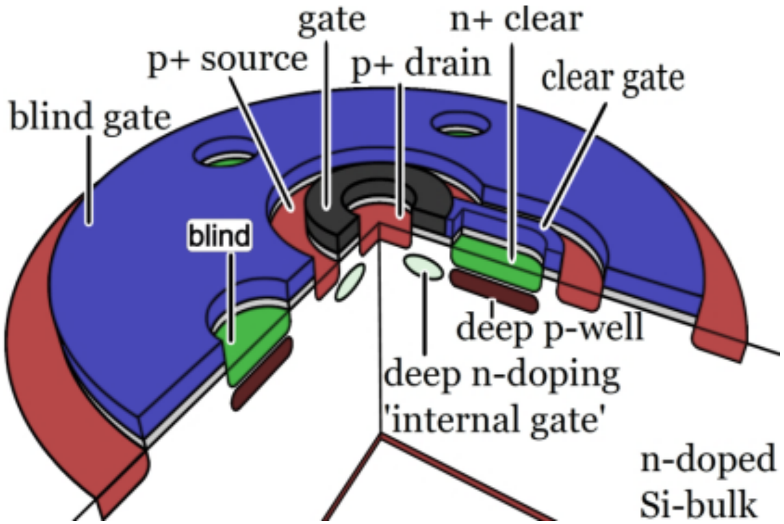
Global "electronic shutter" with precise (≤ 100ns) timing

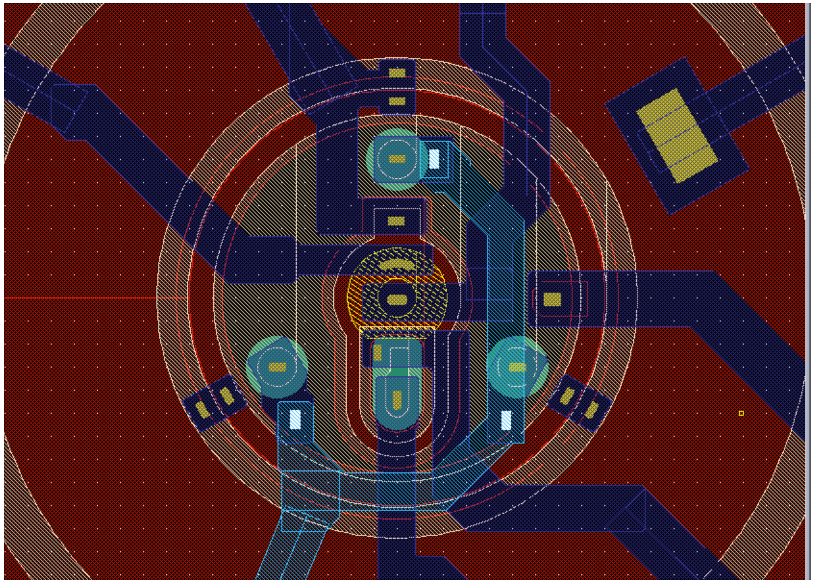
"GPIX" device

GPIX device


DEPFET pixel
with gate feature
Charge
sensitive
node
Dump
Gate
control
voltage
Detector Bulk

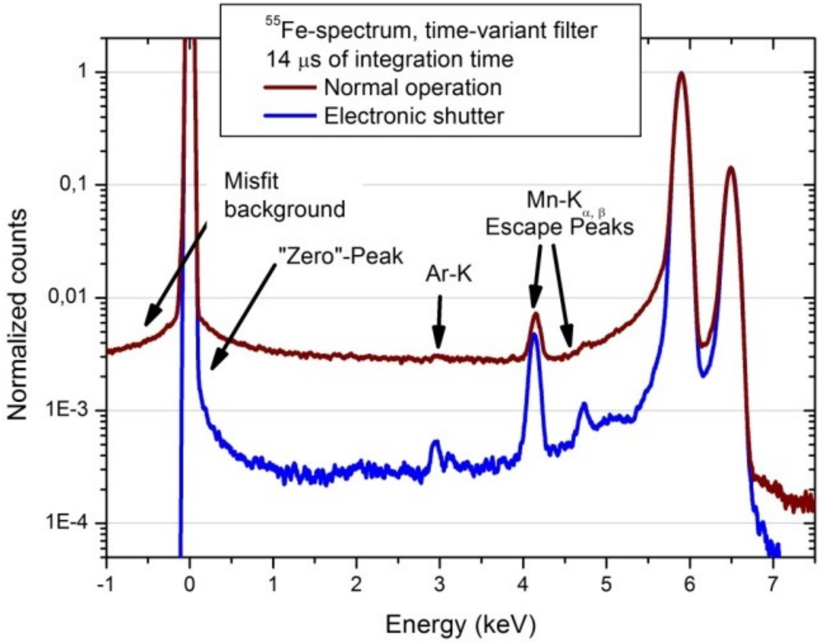
GPIX device

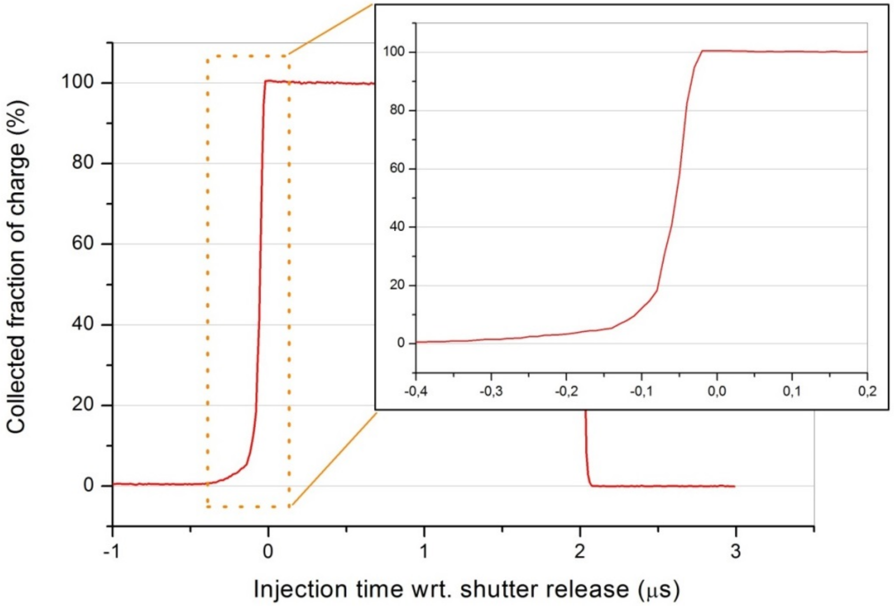




- **Critical parameters:**
  - Charge retention (similar to CHC)
  - Charge suppression > 5 x10^{-4}
  - Shutter speed < 100 ns

Results





Spectroscopic performance:

- P/B =   280, FWHM = 129 eV
- P/B = 3100, FWHM = 129 eV

Timing:

- Rise time 10% - 90 % < 100 ns

Measurements: A. Bähr

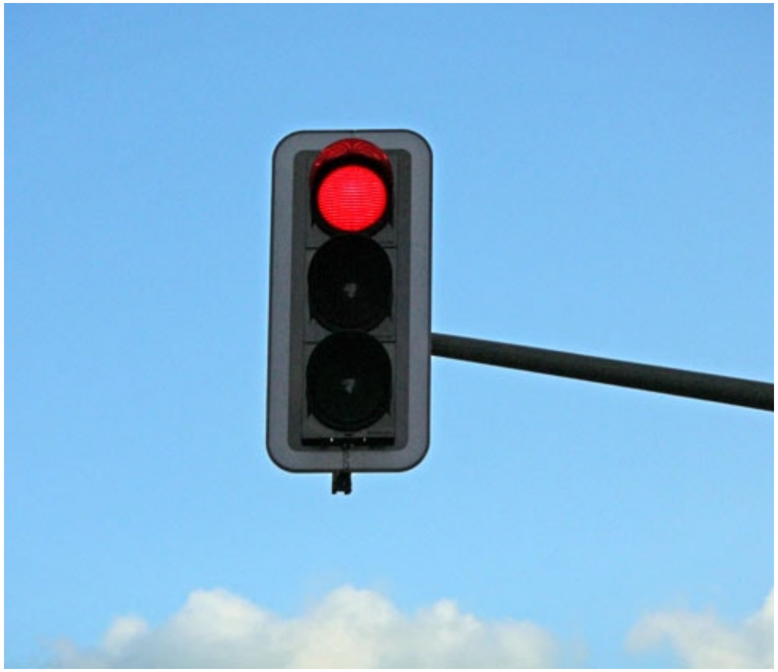
New problem: Dead time

Solution I: IS pixels

Collect charge in dedicated collection region (internal storage)

Transfer of charge to internal gate is regulated by transfer contact

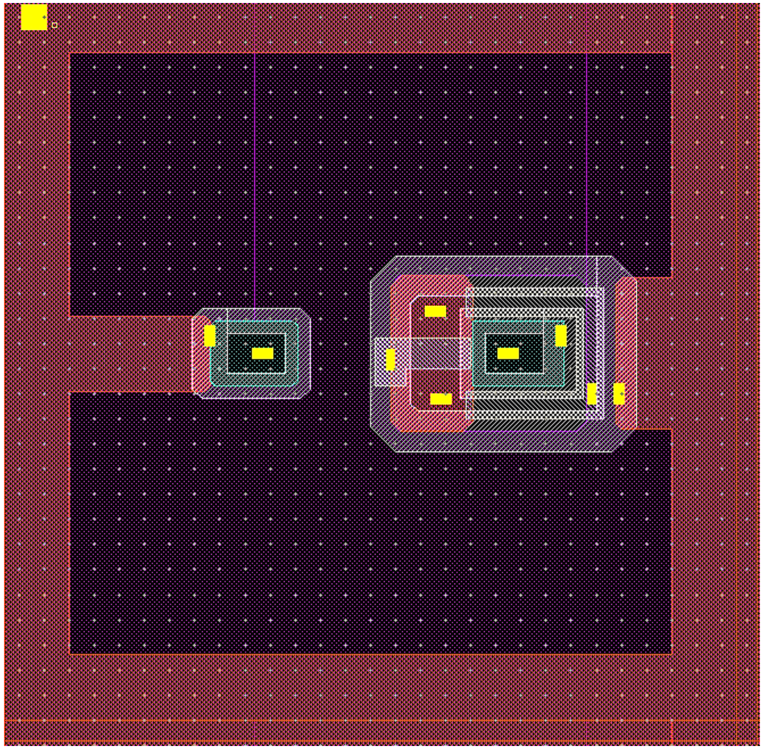
Transfer is done right before readout

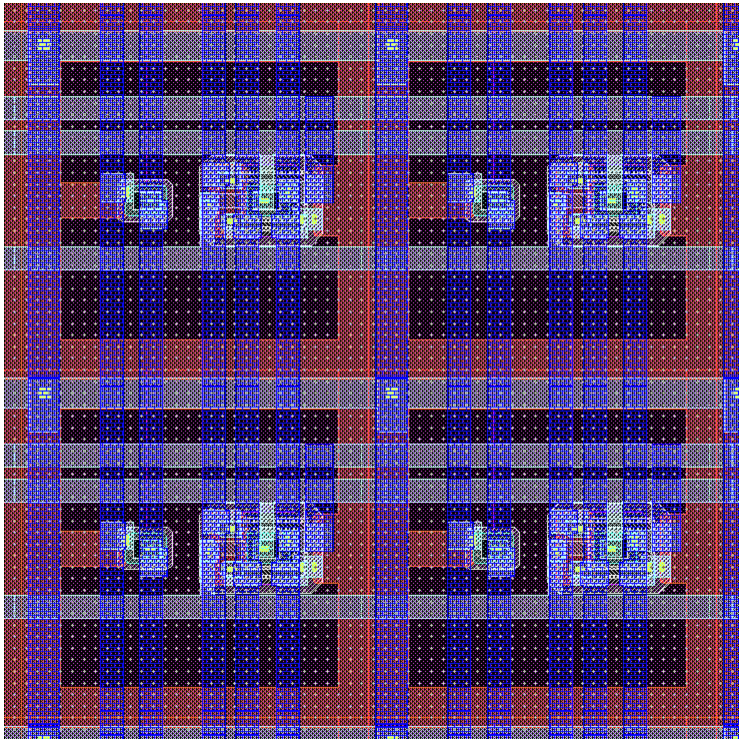


IS pixels

- **Principle:**
    - Store charge in complete pixel region EXCEPT internal gate
    - Transfer charge on-demand to internal gate for readout

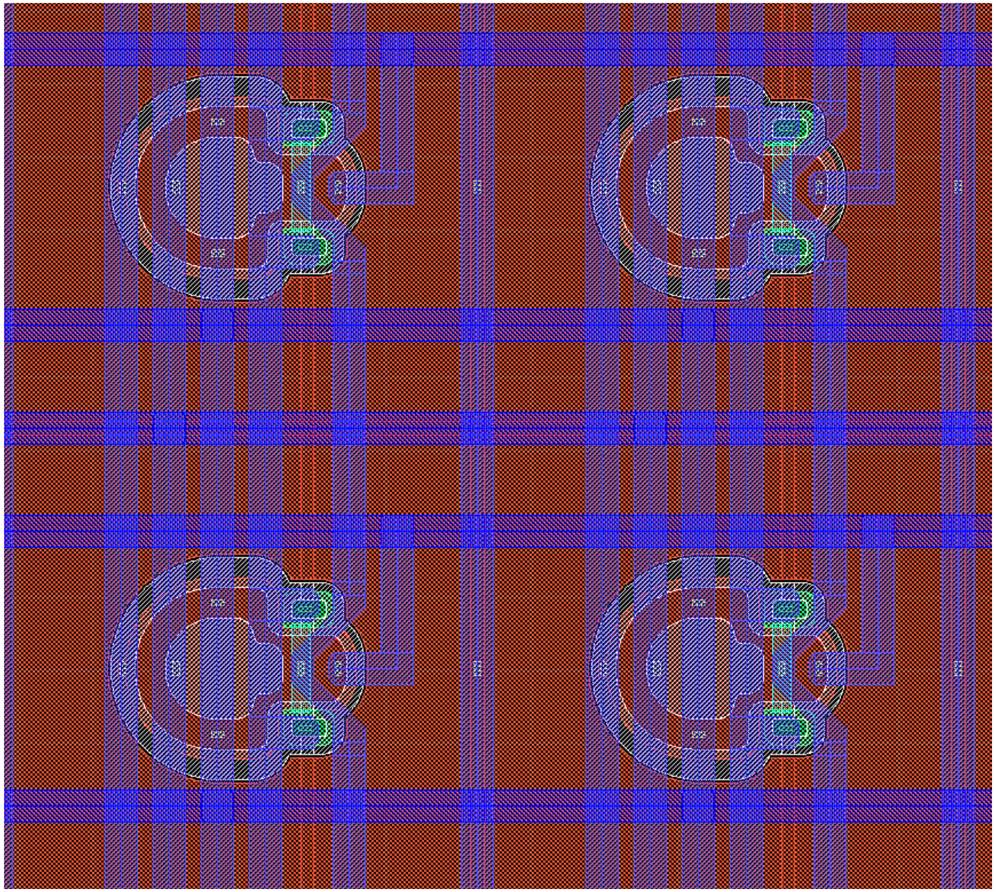
- **Principle:**
    - Charge transfer problematic
    - Charge losses





Turtles

- **Principle:**
    - Charge storage in limited area under dedicated poly-patch
    - Better charge transfer to internal gate
    - No charge losses
    - Easier pixel scalability
    - Works in simulation, not yet tested
    - Prototypes are in production



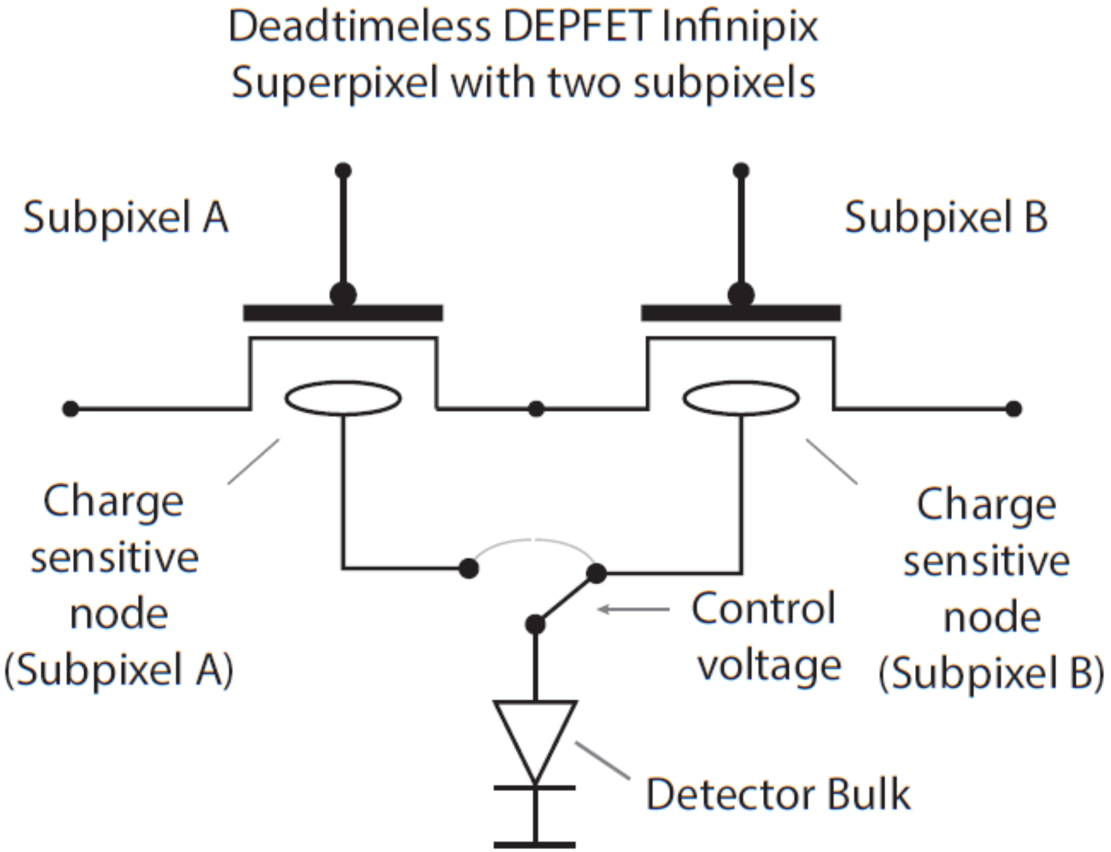
Solution II: Infinipix

Preserve sensitivity of DEPFET during readout

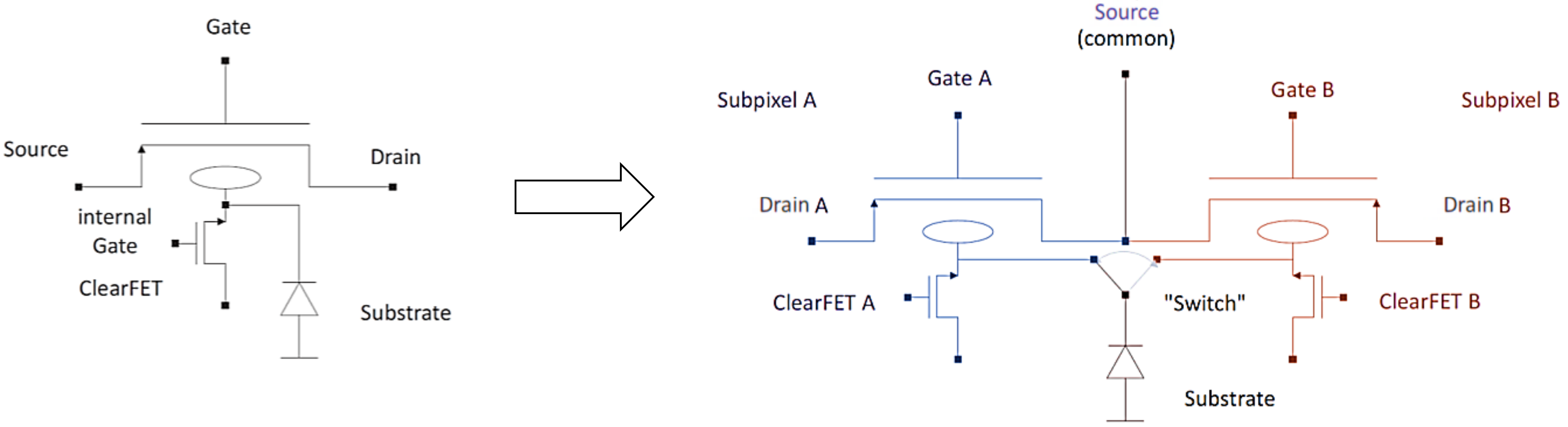
Do not dump charge, but deviate charge to neigboring collection node

Read out later

Infinipix

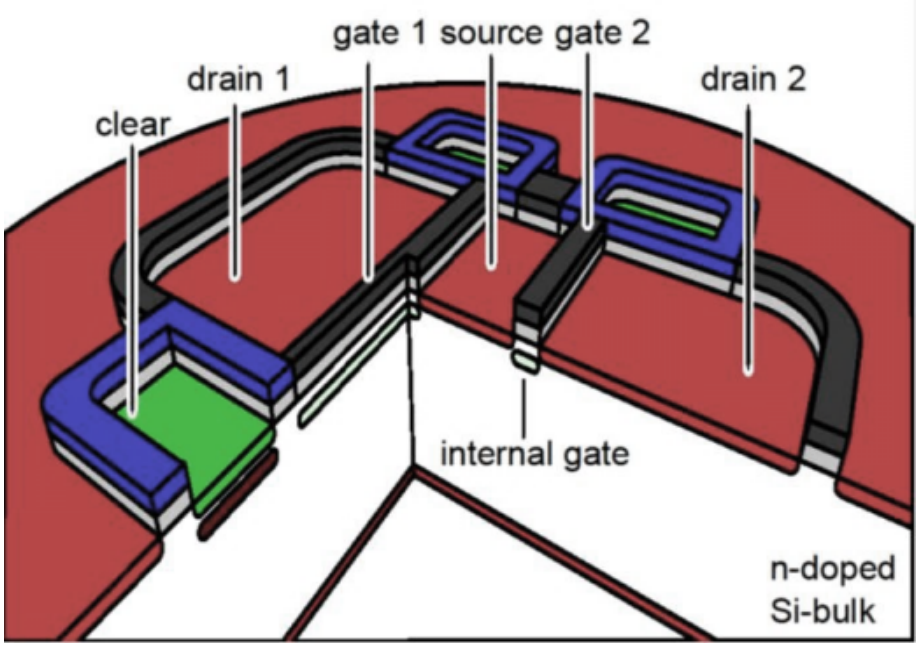

Deadtimeless DEPFET Infinipix
Superpixel with two subpixels
Subpixel A
Subpixel B
Charge sensitive node (Subpixel A)
Control voltage
Charge sensitive node (Subpixel B)
Detector Bulk

Infinipix



- Superpixel consist of two subpixels
- Charge is deviated to one of the subpixels by using the drain potential
- Only insensitive pixel are (and can) be read out
- Strong suppression of MISFIT induced background
- Elimination of broken pattern background due to Rolling Shutter effect
- Benefit larger in case of fast timing
- Optimum use case is **fully parallel readout**

Infinipix

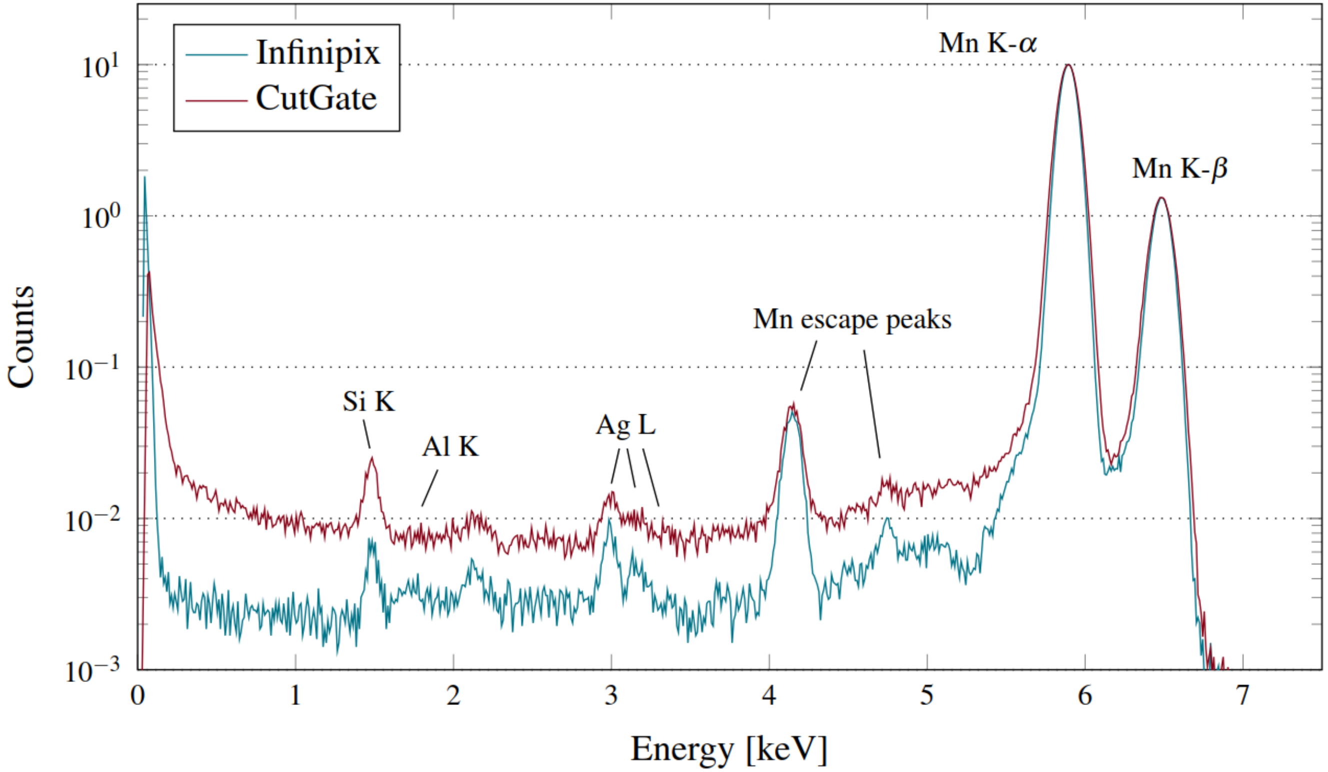


Matrix operation:

- Interconnection generates two independent subframes
- Interleaved storage of images in alternating subframes
- Charge integration in "sensitive" subframe
- Readout of insensitive subframe
- Only insensitive subframe can be read out

- **Critical parameters:**
  - Charge retention (similar to CHC)
  - Charge selectivity > 5 x10^{-4}
  - Switch speed < 100 ns

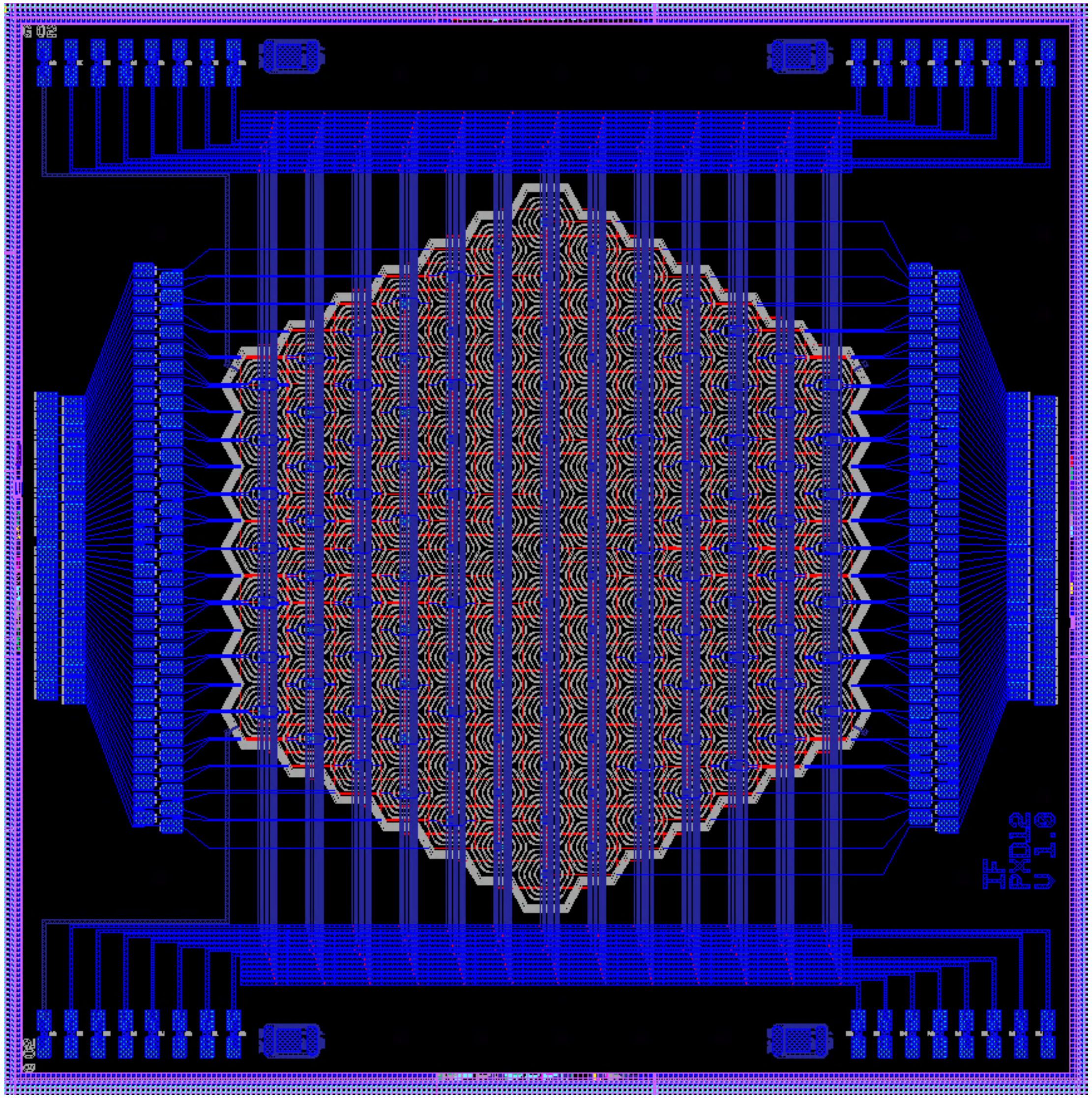
Infinipix



- **Performance:**
  - Spectroscopic performance comparable (~ 130 eV FWHM)
  - Drastically improved peak-to-background
  - Overcomes rolling-shutter effects

Measurement: J. Müller-Seidlitz, MPE

Infinipix



Infinipix vs. Turtle

vs.

- Two gates per (super-)pixel ✗
- Stronger sensitivity to bulk variations ✗
- Higher demand of routing resources ✗
- Probably larger pixels ✗
- Selective storage ✓
- Proven to work ✓

- No Superpixel structure ✓
- Less sensitive to bulk variations ✓
- Easier matrix integration ✓
- Probably smaller pixels ✓
- No selective storage ✗
- Simulation only, no working prototypes yet ✗

Idea

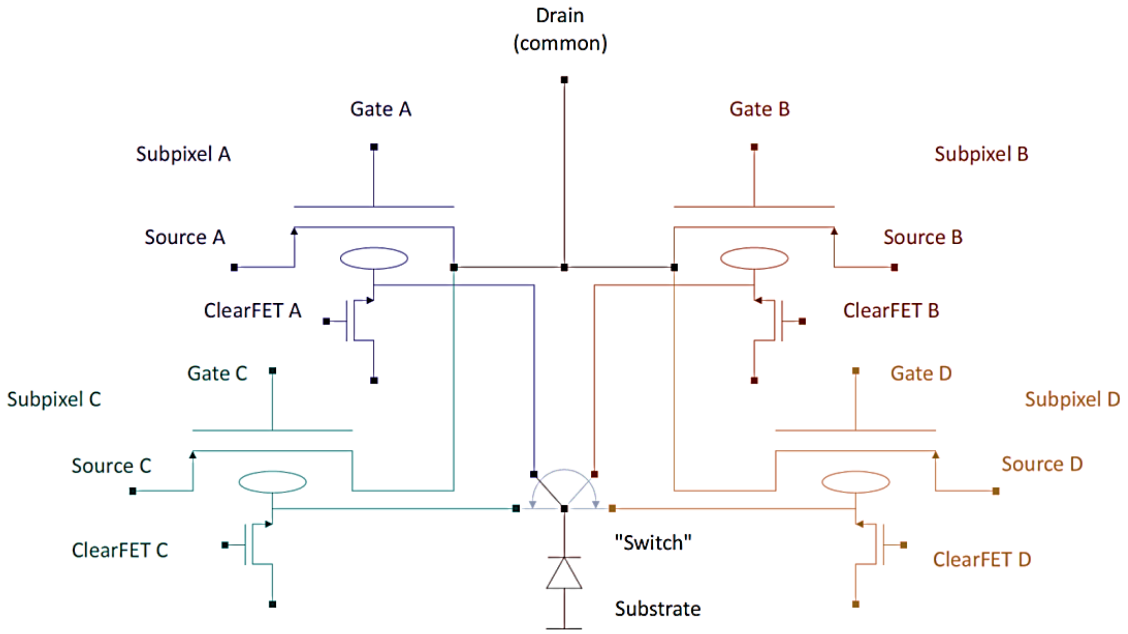
Why only two subframes?

Infinipix Quad (IQ) structures

Application driven:

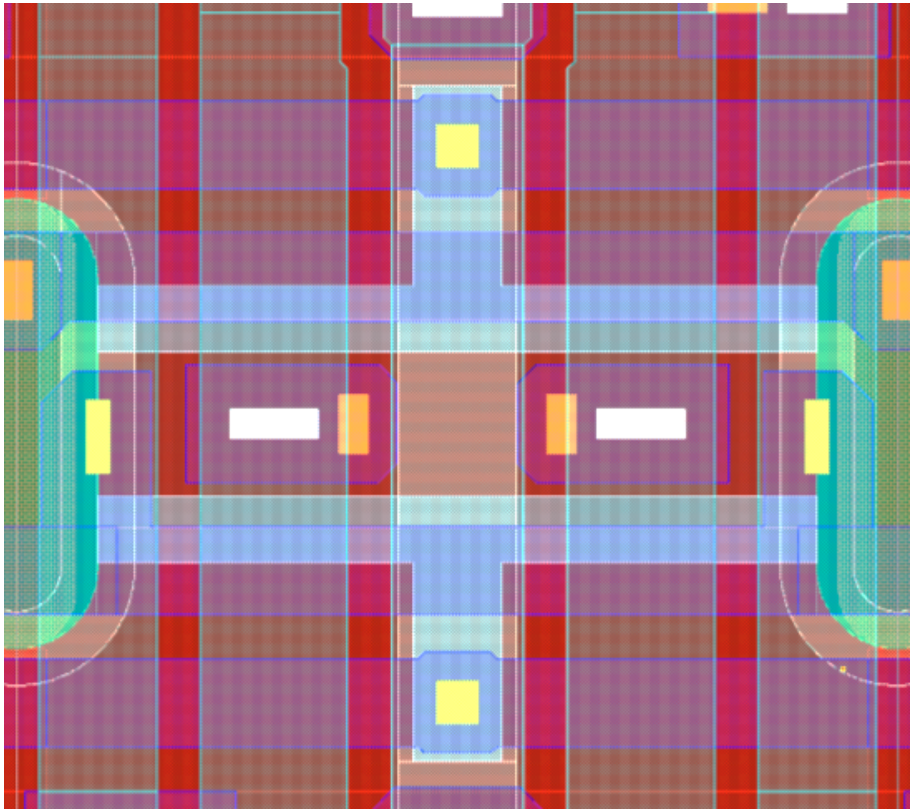
- Infinipix superpixel with 4 subpixels
- Suitable for future (solar) polarimeter (see next talk by A. Bähr)
- Integrated charge for each of four polarization states stored in one associated subpixel
- Switching between subpixels is fast (100 ns)

- Due to large charge handling capacitance, large numbers of images can be integrated
- Readout noise is accounted only once
- Very high duty cycle
- Very high modulation rate



IQ Structures

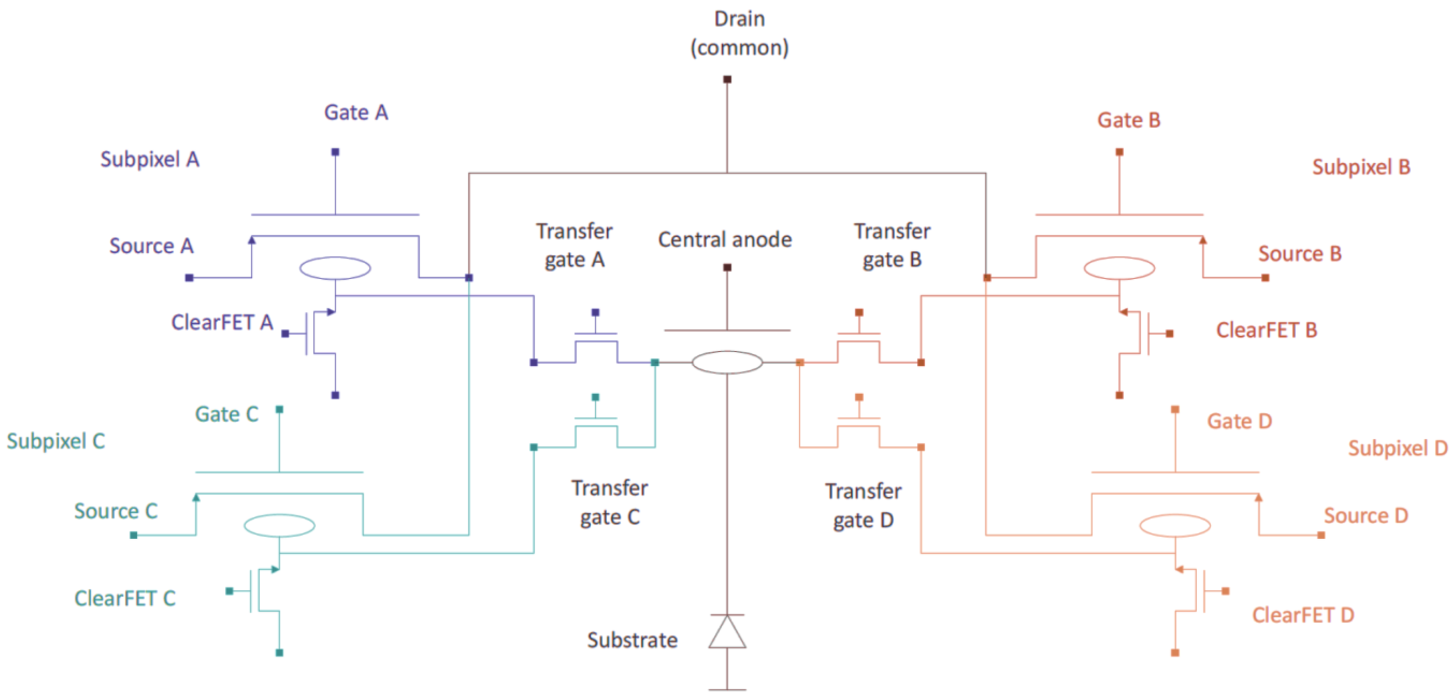
- **Simplified structure:**
  - Common clear
  - Two gates instead of 4
  - Two sources
  - Source follower
  - Device can be sensitive with Gate off
  - Shutter speed < 100 ns
  - Tested on small (32 x 64) superpixel prototypes
  - See next talk by A. Bähr
- **Critical parameters:**
  - Charge retention (similar to CHC)
  - Charge selectivity > 5 x10^{-4} ?
  - Switch speed < 100 ns
  - **New: Spatial conformity!**



"Standard" IQ (Infinipix Quad) structure

IQ-CA Structures

- Spatial shift of images due to the varying drain potential
- Effect can be eliminated in sensor, if pixel structure robust against this effect: **Focus implant / Deep storage**
- Have structure with **common central storage node** and transfer the charge collected during integration on-demand to respective storage DEPFET
- So-called **"Central Anode"** structure



R-NDR devices

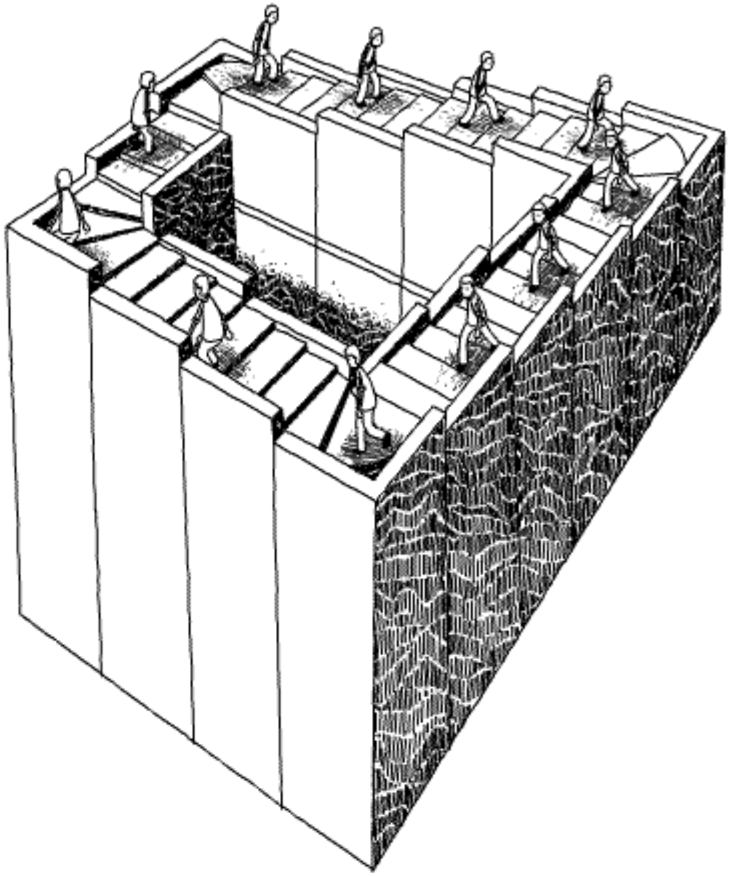
Repetitive-Non-Destructive-Readout

Beat noise limit using the central limit theorem!

Lower initial noise!

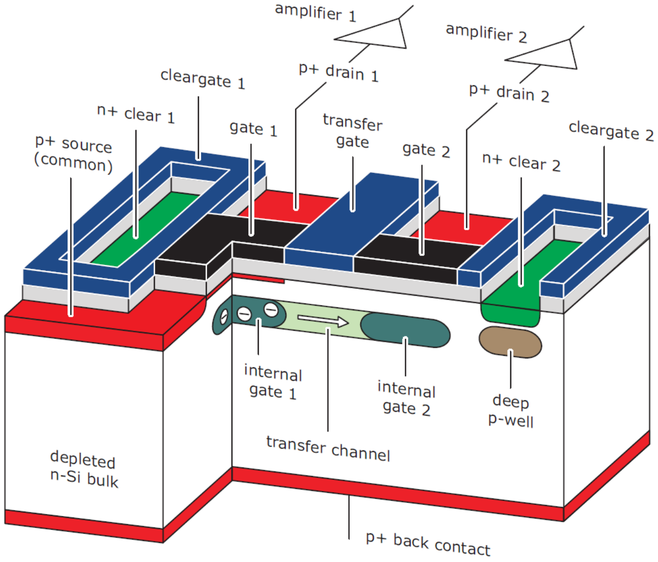
Achieve single electron / photon sensitivity!

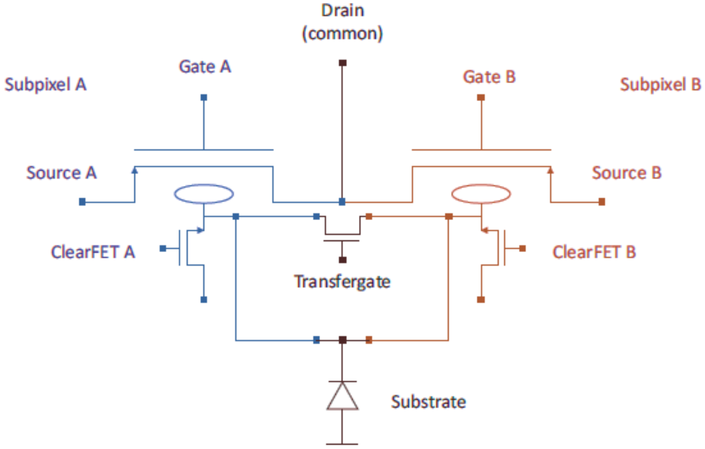
Non-destructive readout can be used for incremental measurements (NDIR)



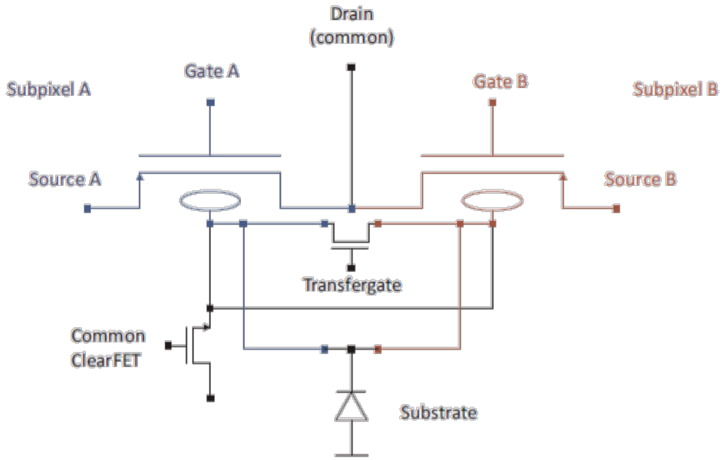
RNDR devices

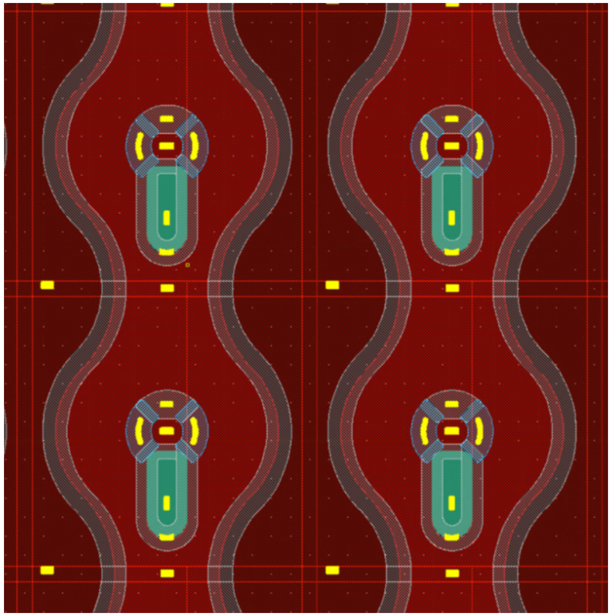
- DEPFET repetitive non-destructive readout (RNDR)
  - practical application of the central limit theorem
  - 2 DEPFET “sub”pixels in “super”1 pixel
  - intra-pixel charge transfer via transfer gate
  - allows for statistically independent measurements
  - elimination of 1/f-noise limit
  - noise reduction by $N^{½}$ @ N readings
  - sub-electron noise: 0.18 el. ENC
  - single electron distinction



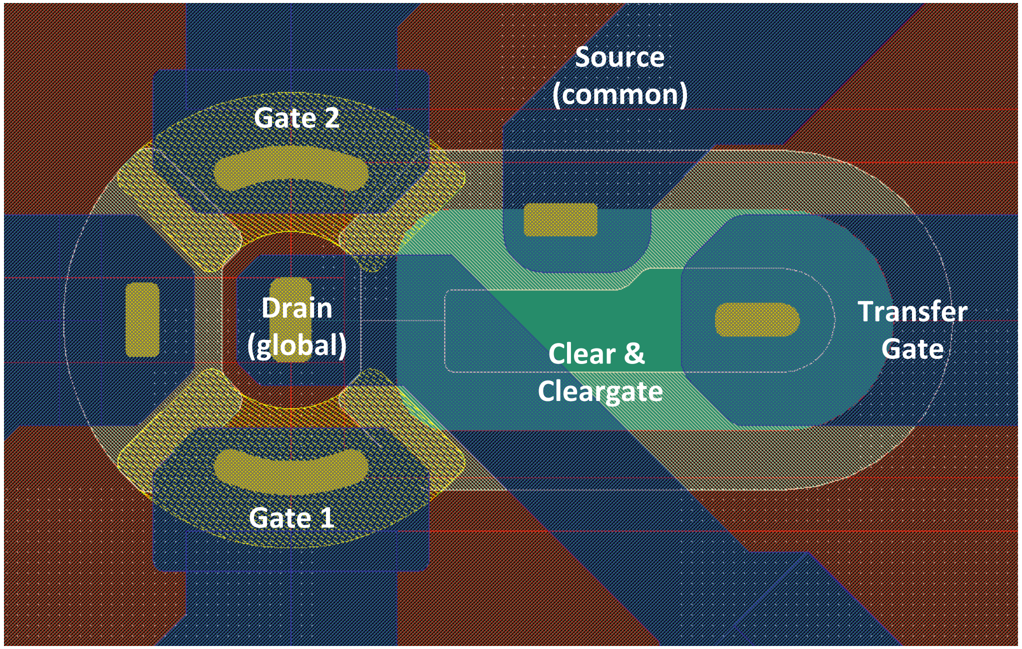


RNDR devices

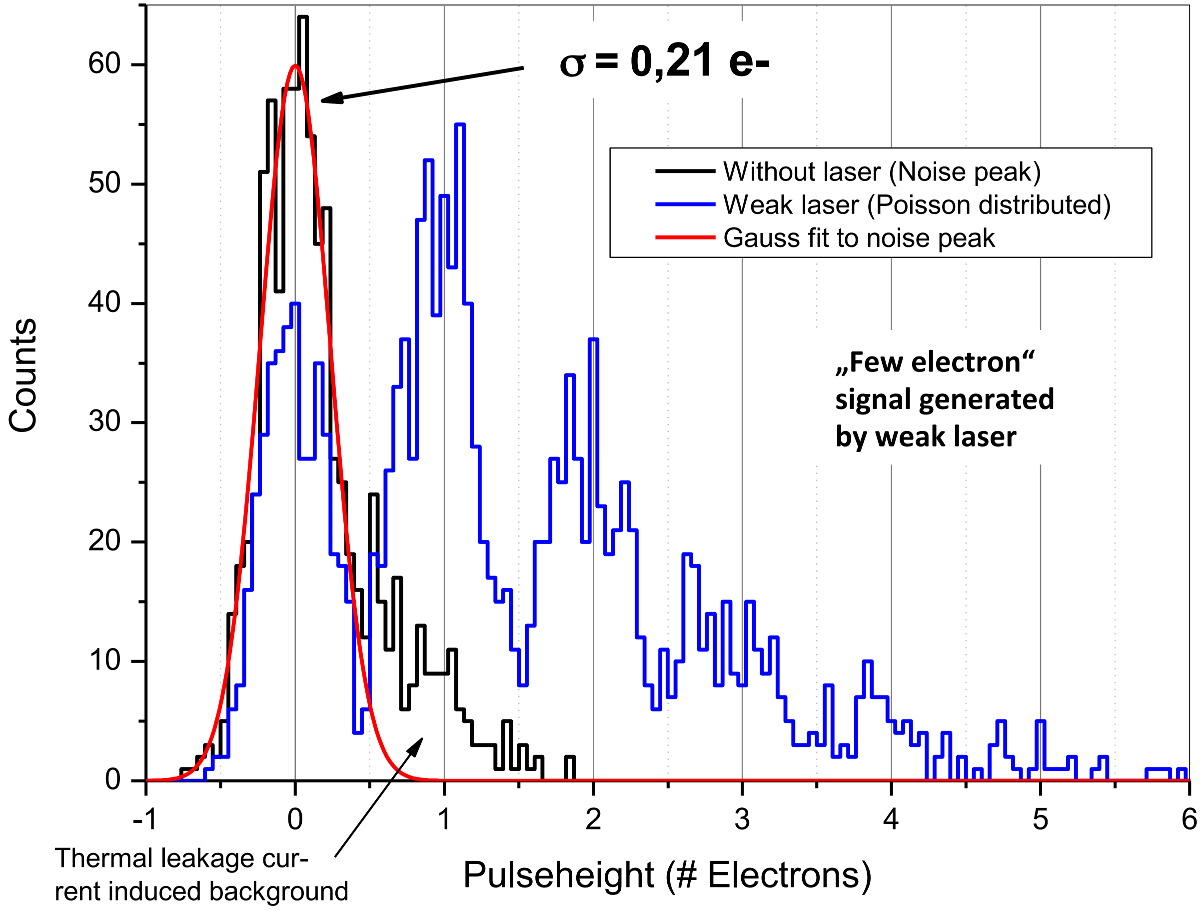




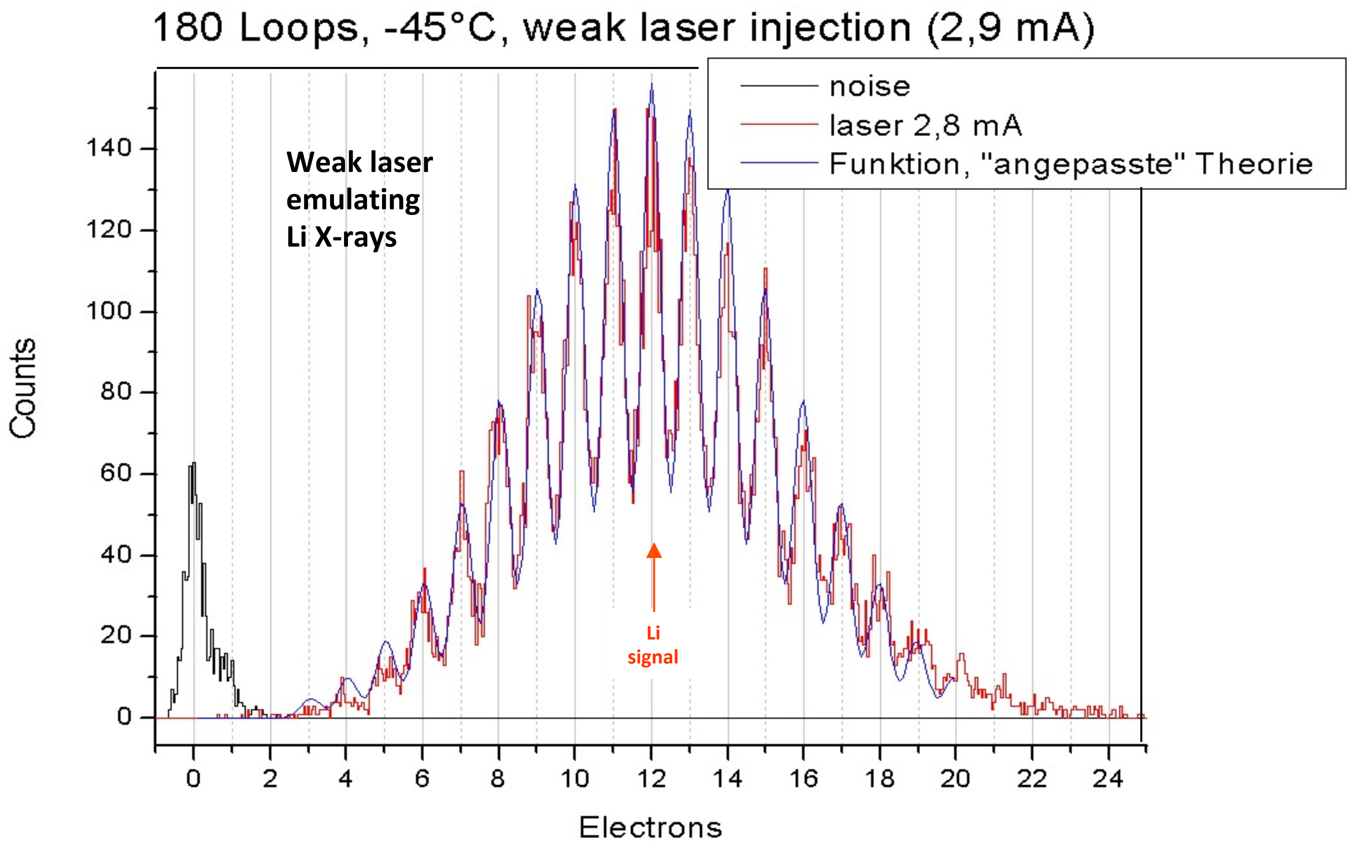
State-of-the-art "compact" circular RNDR pixel
Easy to integrate in matrix environment



RNDR devices



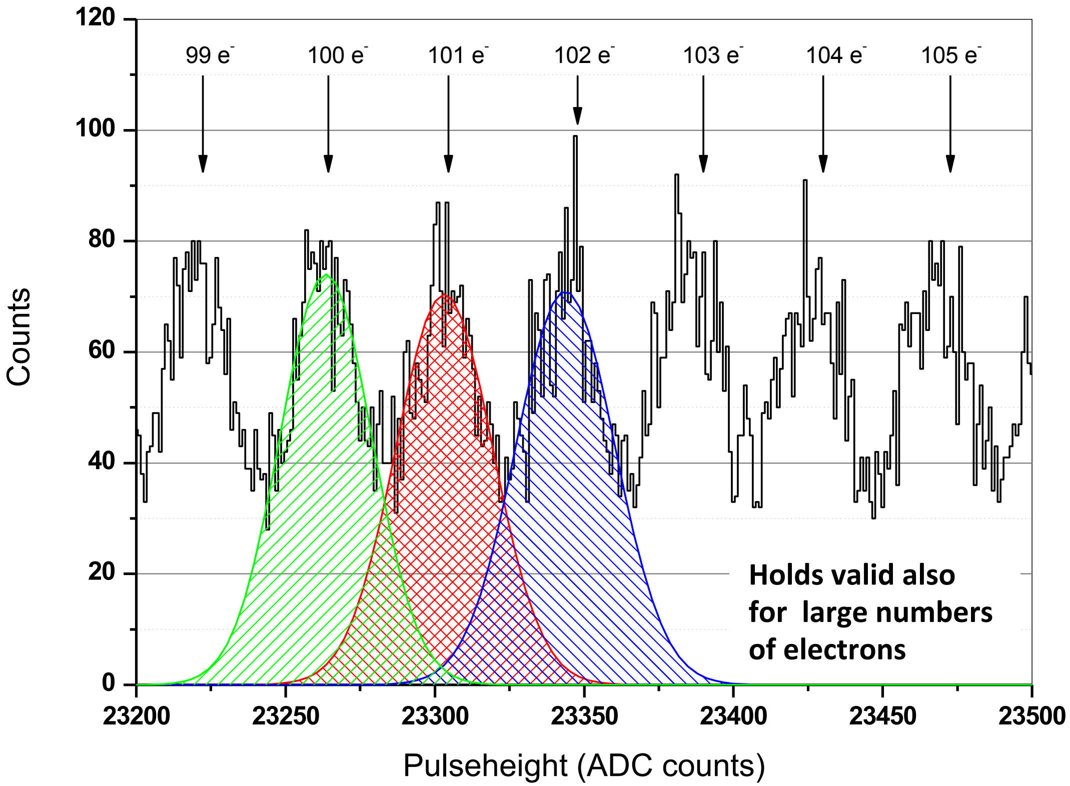
RNDR devices



Weak laser emulating Li X-rays

Li signal

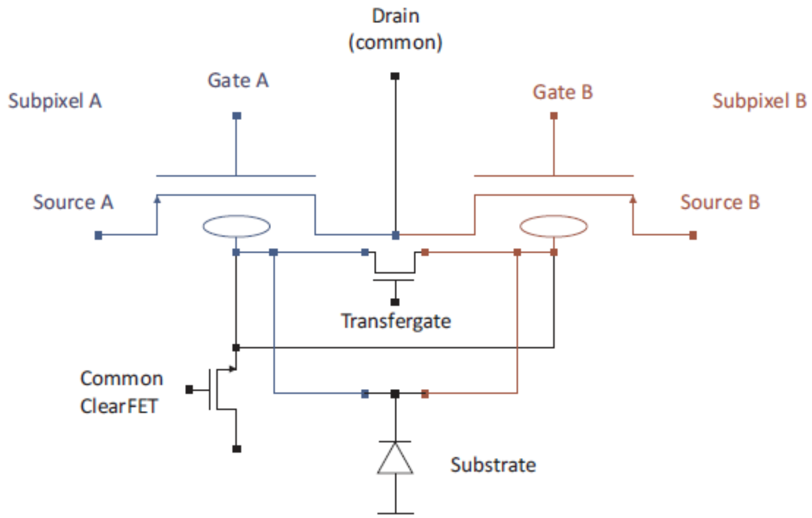
RNDR devices



Holds valid also for large numbers of electrons

Problem: Misfits again!

- DEPFET device is permanently sensitive
- Charge can enter internal gate during processing
- Bulk generated leakage current electrons
- Event charge ("Misfits")
- Weighted differently depending on arrival time
- Correction term to $n^{-1/2}$ (Baer's equation)



- Baehr's equation:

$$V(\bar{x}) = \frac{\sigma^2}{n} + \Delta\sigma^2 \cdot \left(\frac{1}{2} + \frac{1}{3} \cdot n - \frac{5}{6} \cdot \frac{1}{n}\right)$$

- Optimum number of cycles:

$$n_{opt} = \sqrt{3 \cdot \frac{\sigma^2}{\Delta\sigma^2} - \frac{5}{2}}$$

- Optimum effective noise:

$$ENC_{eff}^{opt} = \sqrt{\frac{\sigma^2}{n_{opt}} + \Delta\sigma^2 \cdot \left(\frac{1}{2} + \frac{1}{3} \cdot n_{opt} - \frac{5}{6} \cdot \frac{1}{n_{opt}}\right)}$$

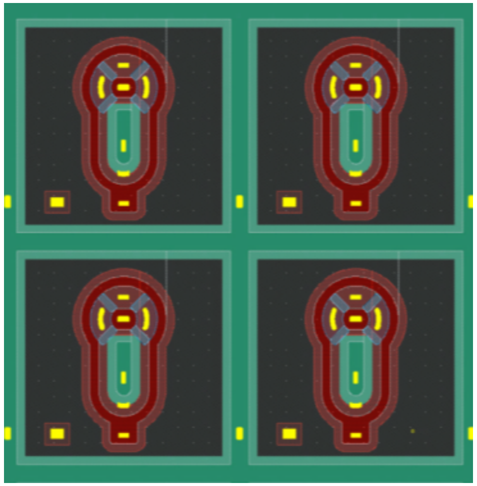
"Hybrid"DEPFETs

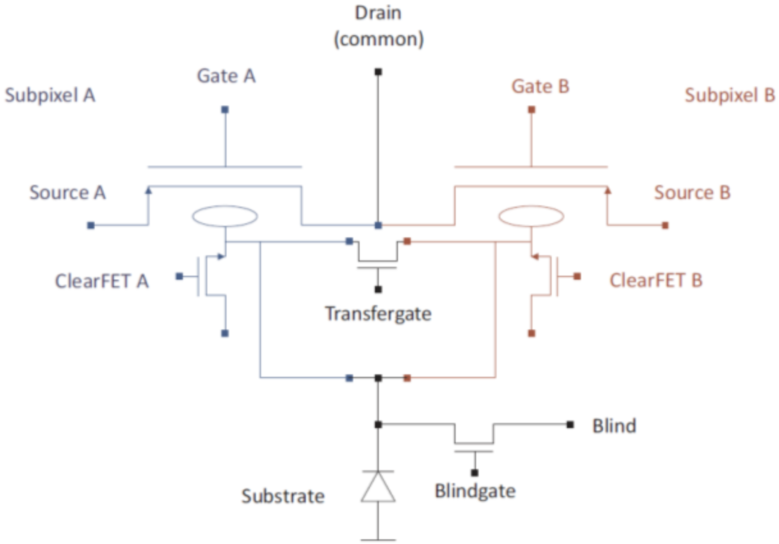
Combine different conceptual features

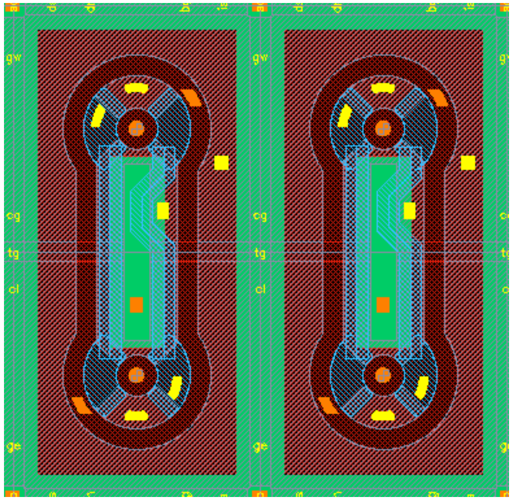
Create devices with multiple capabilities

GPIX RNDR

- RNDR pixel embedded in blindgate structure
- Global shutter
- Suppression of bulk leakage current
- RNDR process can take arbitrary time
- Single pixel / matrix device

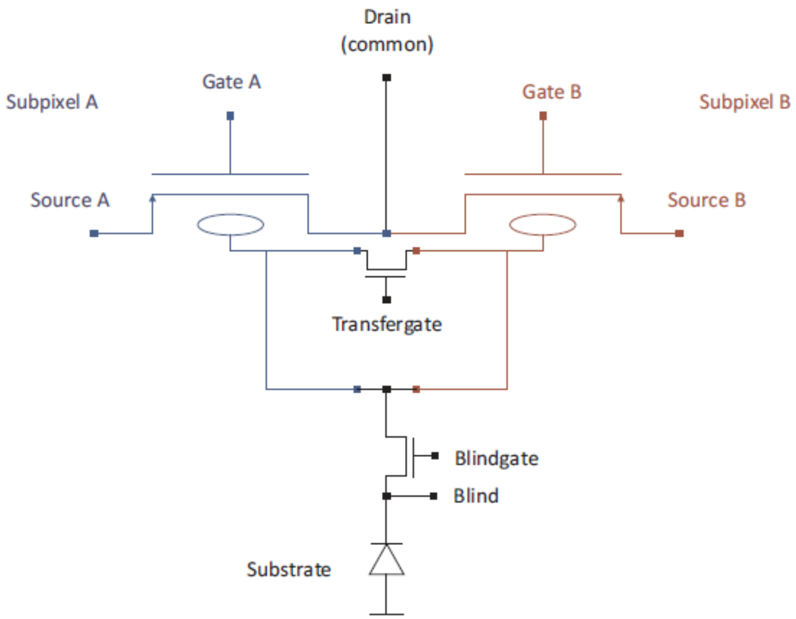


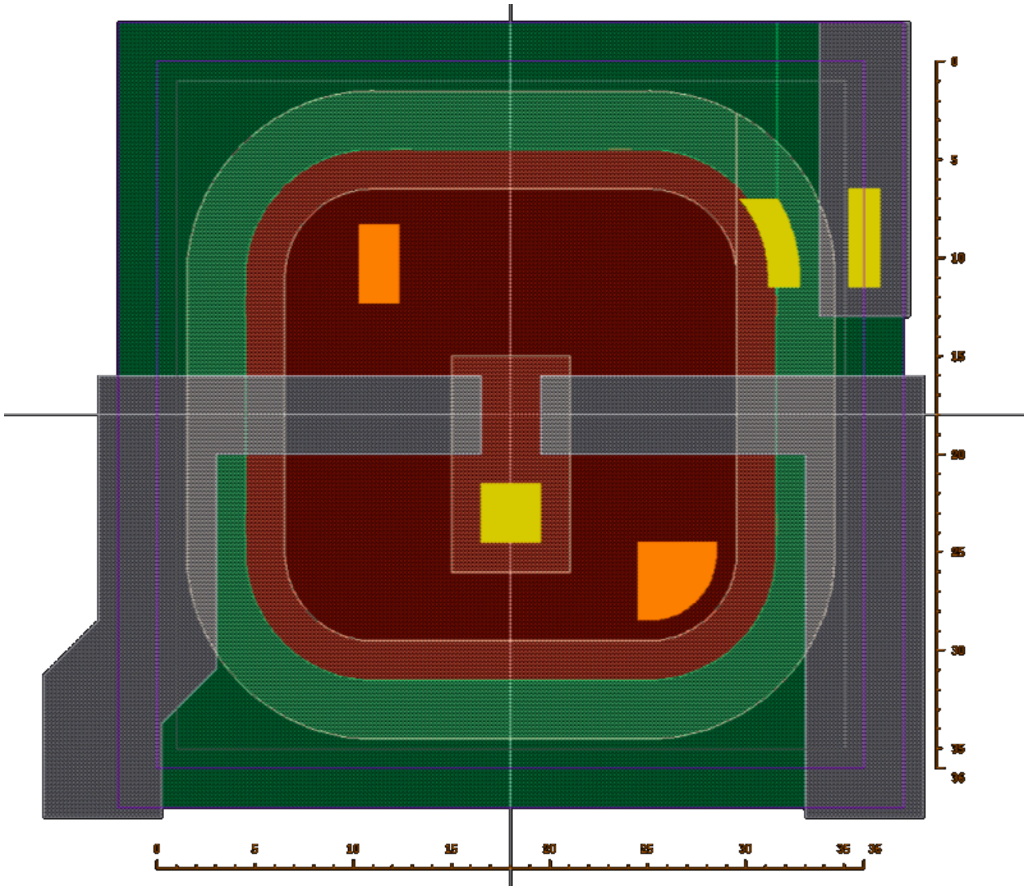




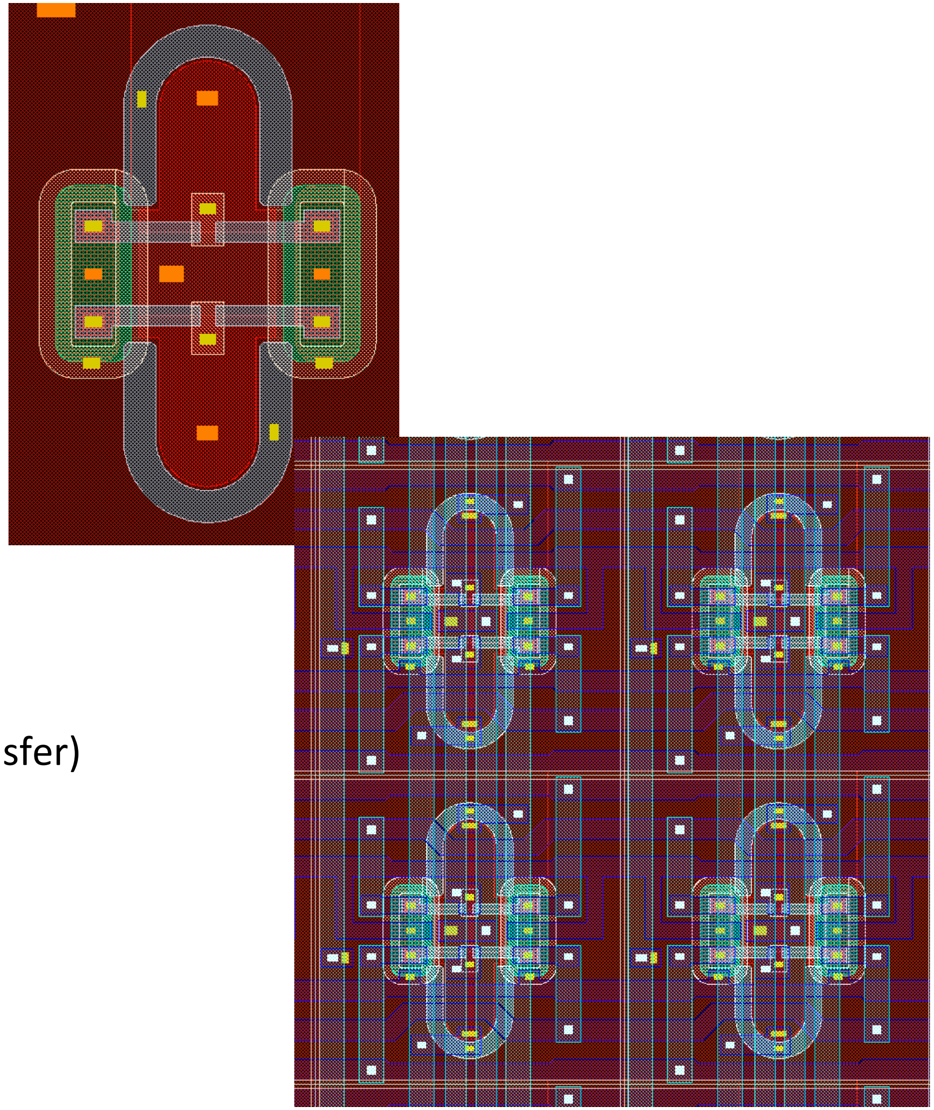
Infinipix RNDR

- Linear RNDR
- Global Clear variant
- Blinds also used for clearing
- 36 x 36 μm^2





Infinipix RNDR



Prototype structure:

- RNDR feature can easily be implemented
- Global transfergate
- Common clear

- **Critical parameters:**
  - Charge transfer efficiency
  - Charge retention (also during transfer)
  - Charge selectivity
  - Transfer speed
  - Initial noise

What next?

Processing improvements:

- Smaller structure / pixel sizes
- Higher precision / homogeneity
- Higher integration densities

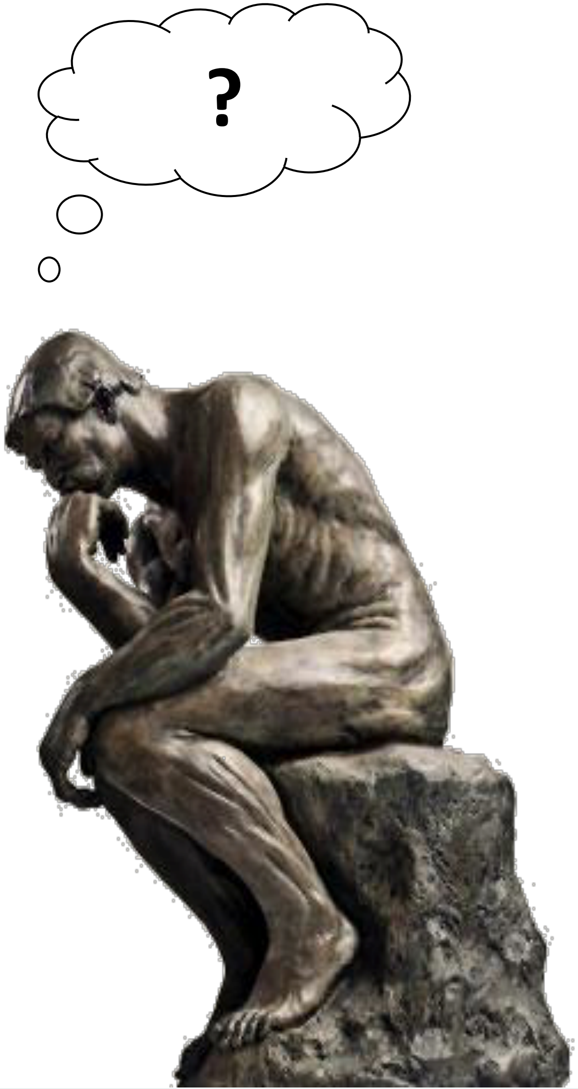
Technology improvements:

- Super-g_q devices
- Improved radiation hardness (!)

New devices:

- CCD 2020
- SESR
- "Hybrid" structures

New projects!



Conclusion

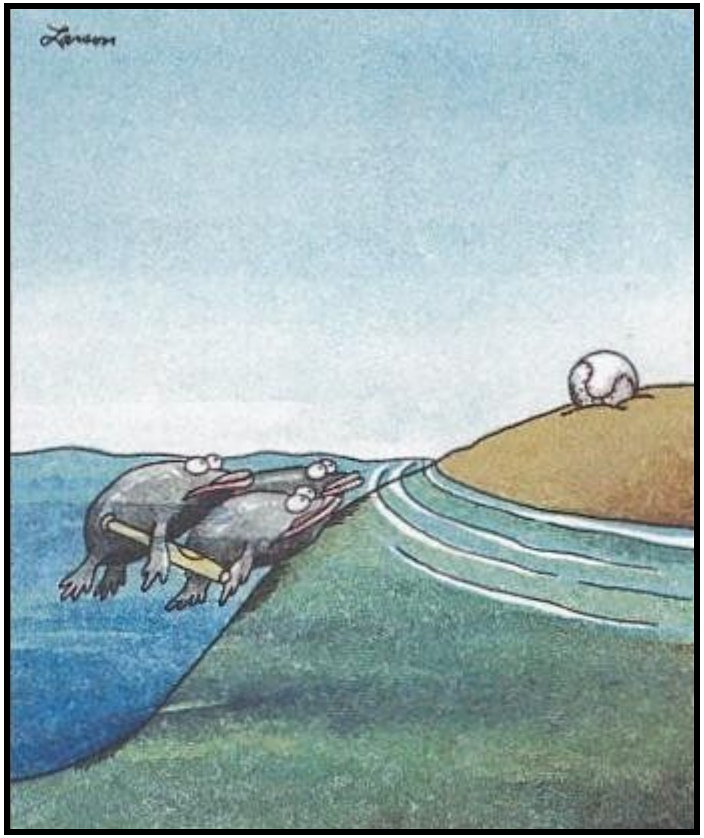
Constant evolution of DEPFET based devices

Elimination of traditional weaknesses

Enable new capabilities

New applications

At the verge of a new chapter



Another great moment in evolution