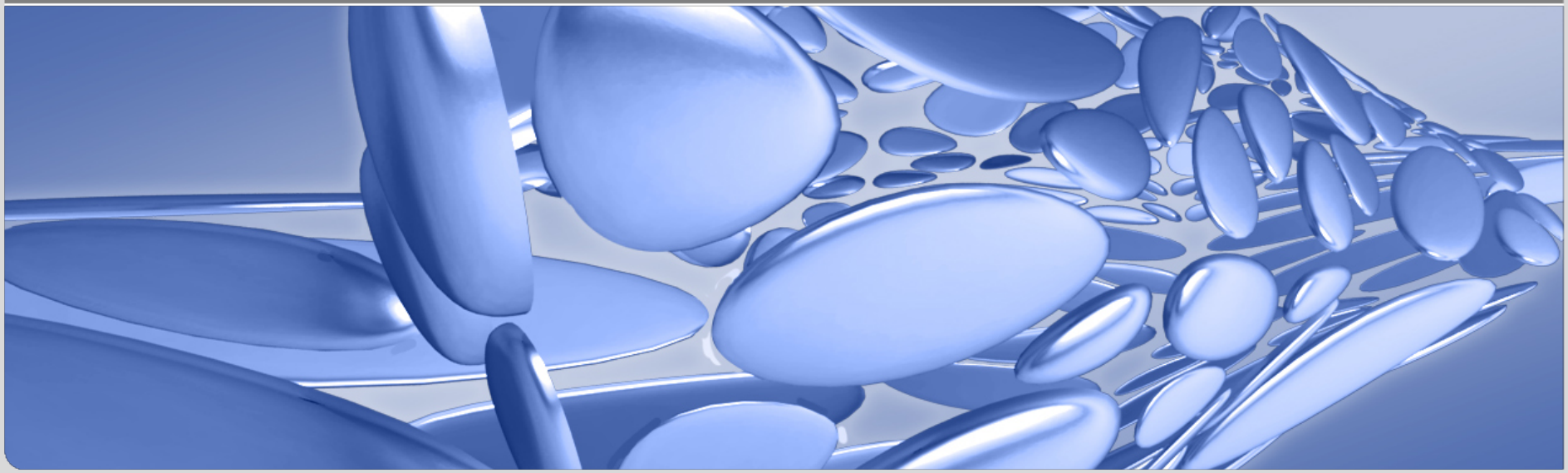
ASICs for DEPFETs and Drift Diodes

Ivan Peric



- DEPFET readout
- Possible developments (DCD)
- Lower power consumption: DCDC – DCD with SAR ADC
- Faster sampling rate: Motivation belle upgrades, try to cope with occupancy
  - Example 50ns instead 100ns (256 channels), faster is also possible (time interleaving)
- Implementation of fast LVDS links: motivation DCD to FPGA direct connection
  - Example: 1.6 G bit/s each, 8b10b, 16 such links are equivalent to 64 CMOS links (we have now)
- DCD with extended dynamic range: Motivation diffraction experiments (Electrons, x-rays)
  - Example sampling time 512ns – linear dynamic range ~16 000, generally: dynamic range = time^2
- SWITCHER improvements
  - E.g. with more channels
- Drift diode readout
  - Multichannel amplifier chip for drift diodes or drift diodes with JFET

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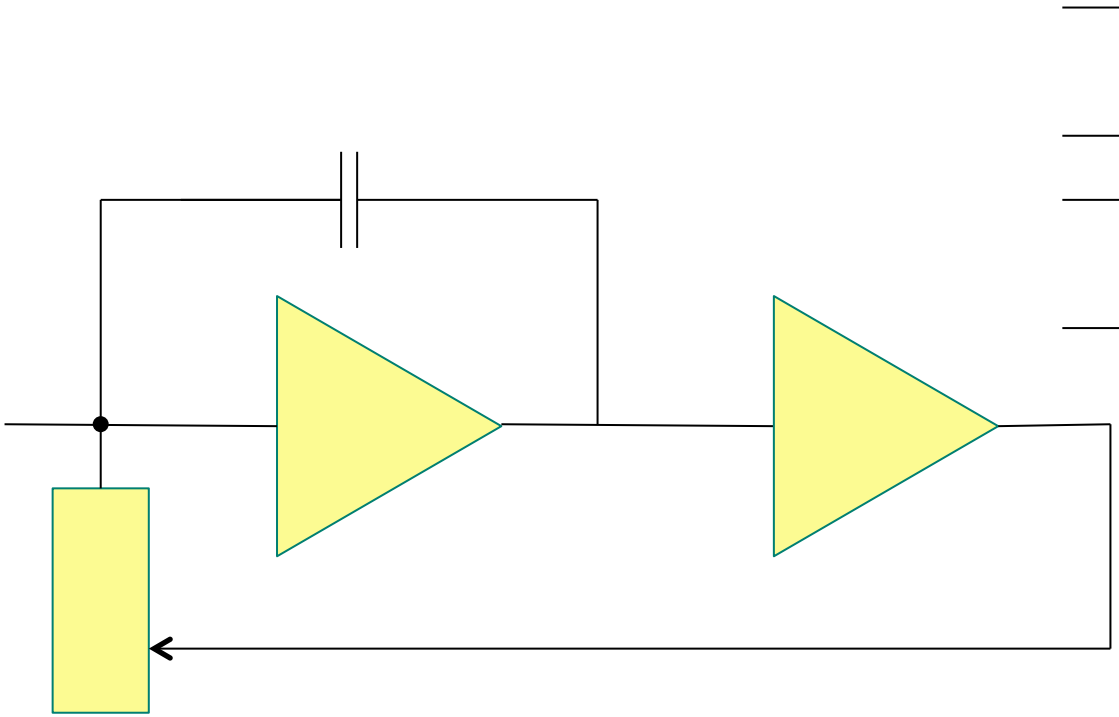
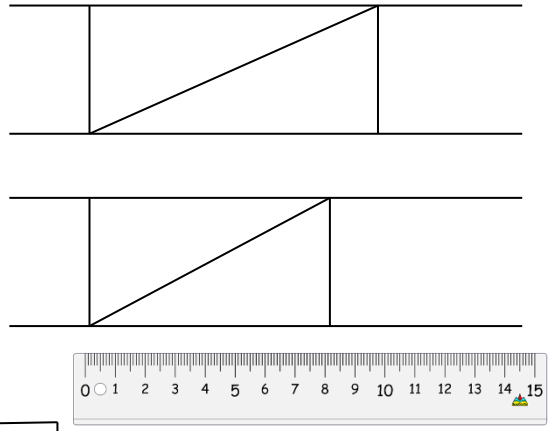
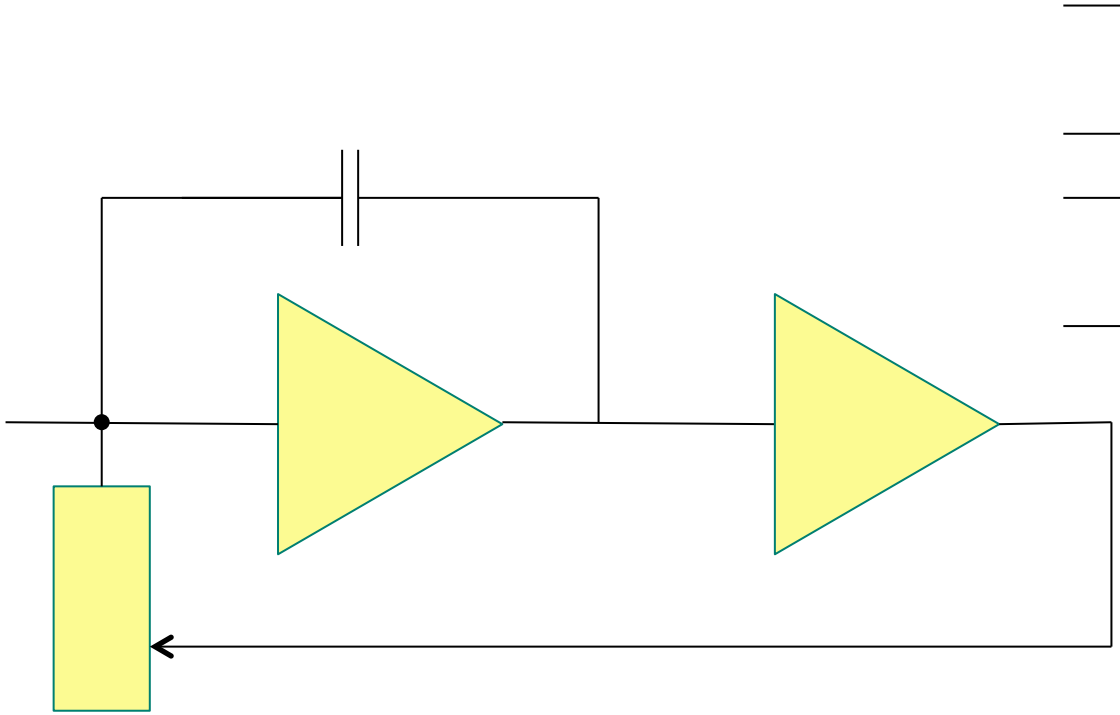
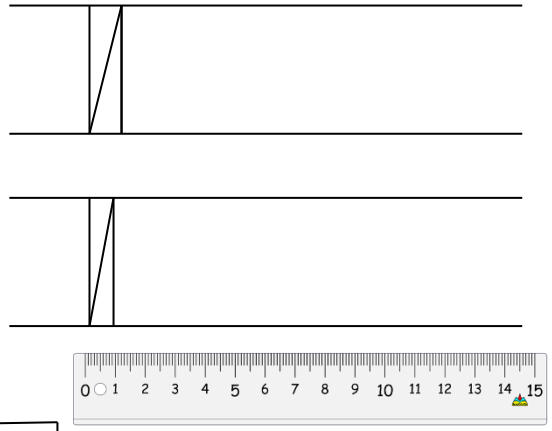
- Example: Readout with high dynamic range
- Implemented as (counting-integrating) pixel readout chip in UMC 180nm technology (the same as DCD)
- Working principle: integrator with charge pump (a kind of sigma-delta ADC)
- Combined time and pump number measurements



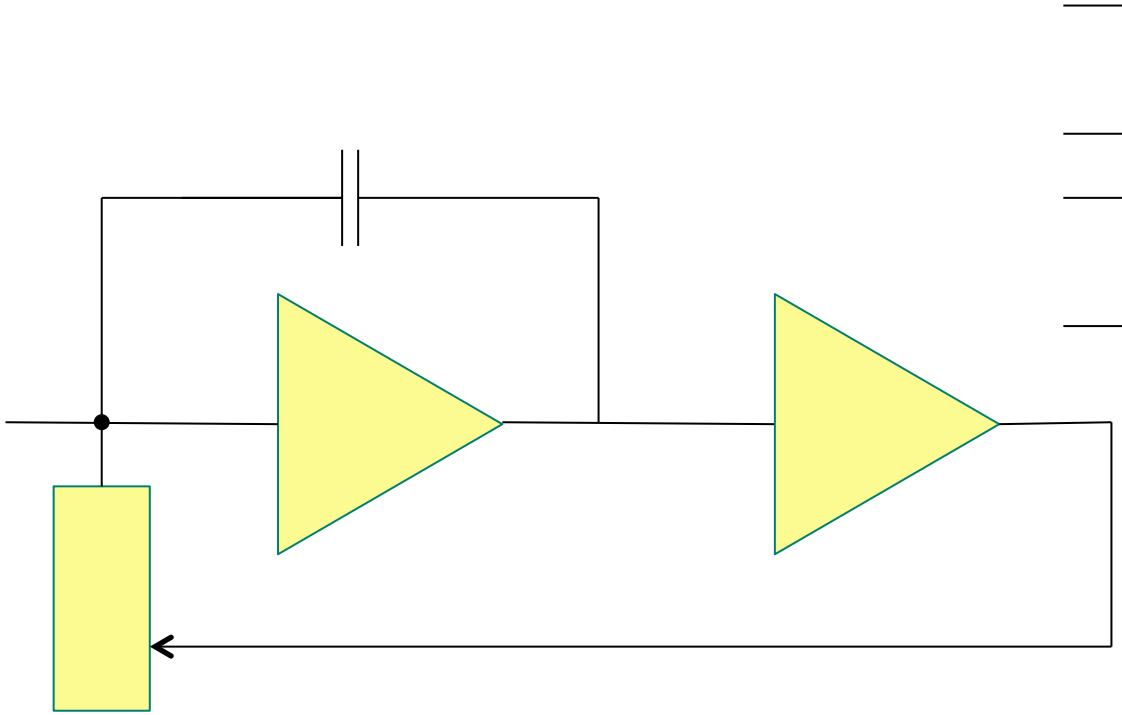


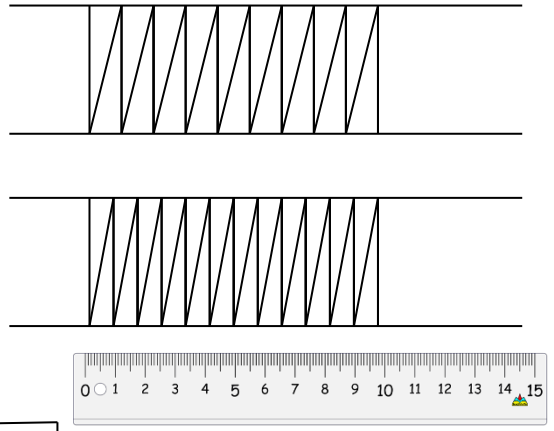
Small current measurement – time provides good accuracy





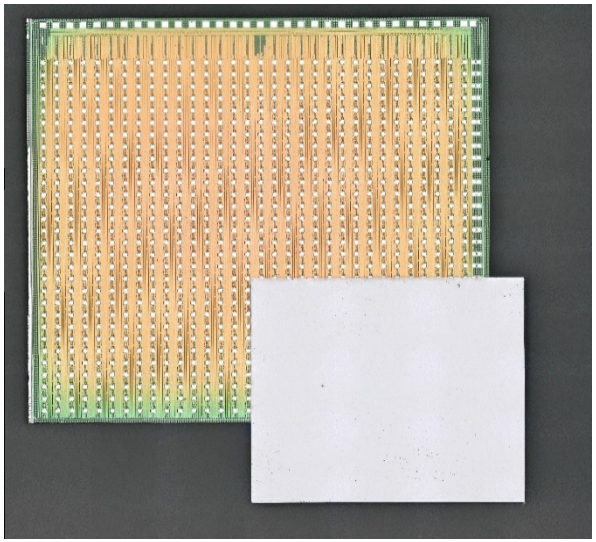
Large current measurement – poor accuracy if only time is measured





Large current measurement – good accuracy if both time and number of pulses are measured

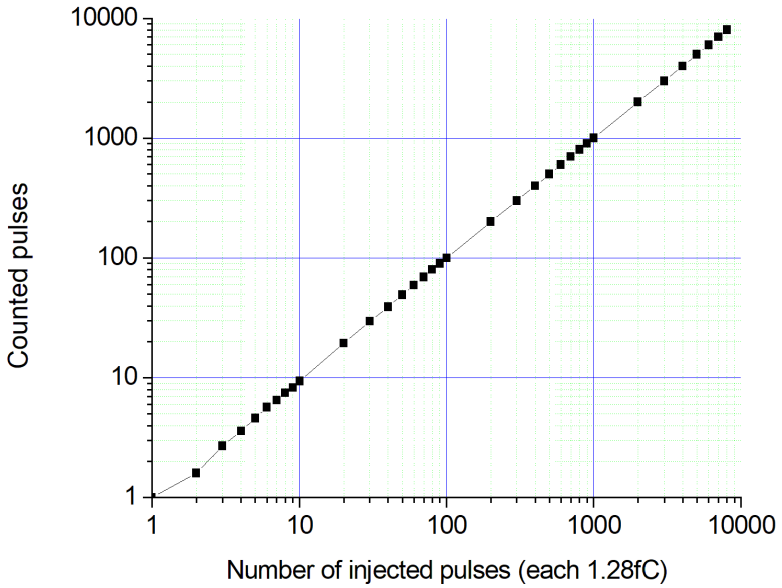
- Following slides show how the circuit can work
- PHOTON pixel readout ASIC
- Simultaneous counting and integrating
- Pixel size 150µm x 150µm
- Chip size 5 x 5 mm



Capacitively coupled sensor readout by PHOTON

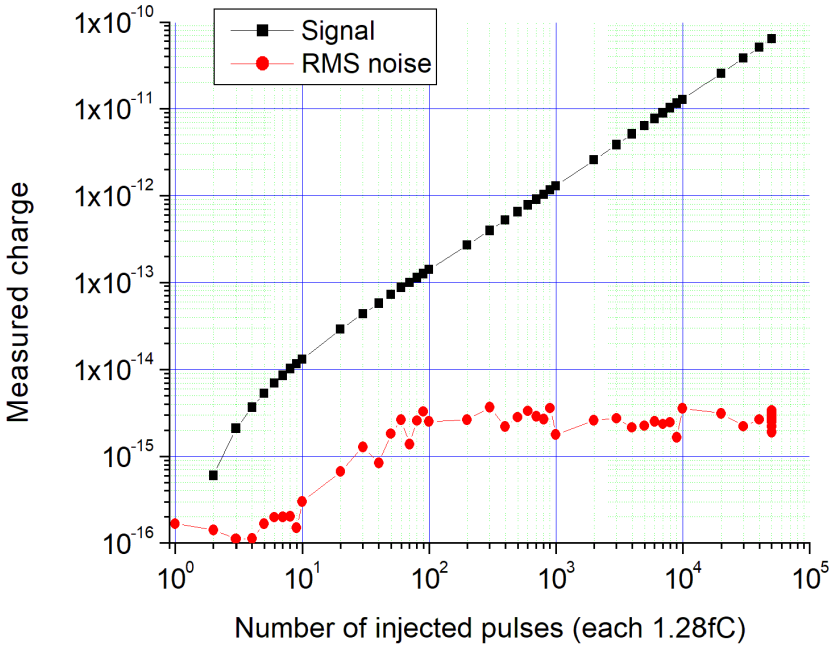
- Example measurement:
- Injection circuit emulate photon hits
- Measurement time: 6.5ms
- 1 – 50020 pulses
- Maximal signal: 64 000 fC

- 13 bit pixel counter



Number of counts vs. number of injected signals (2Mhz)

- High dynamic range integrator

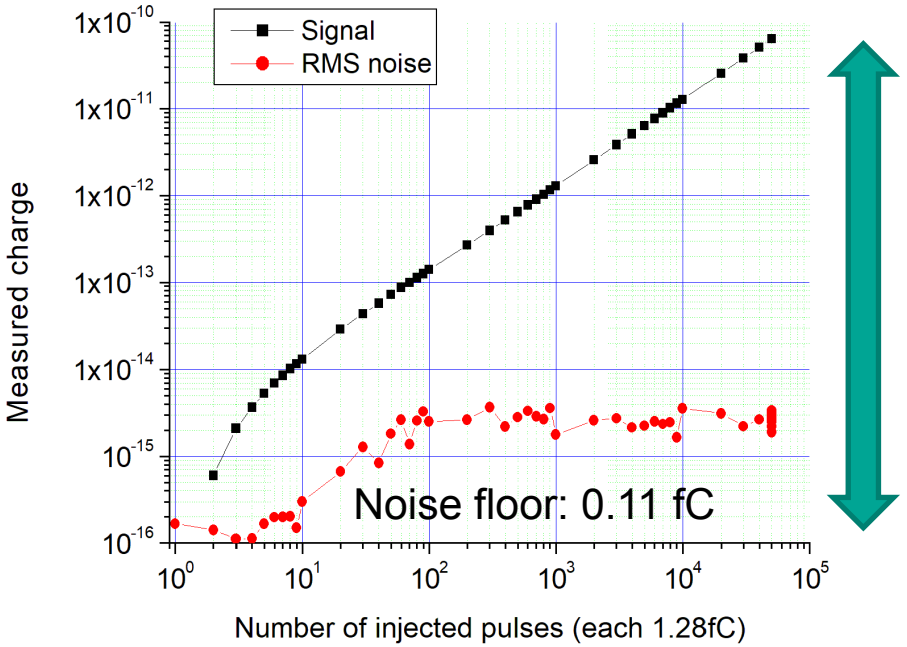


Measured charge vs. number of injected signals

- Dynamic range: 500 000

Maximal signal: 64 000 fC

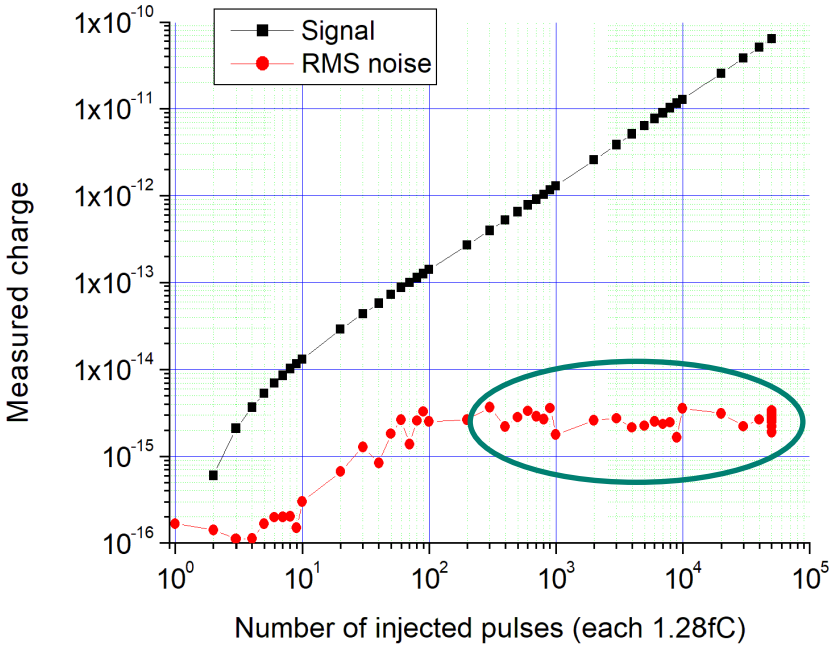
Signal 8nA



Noise floor: 16fA

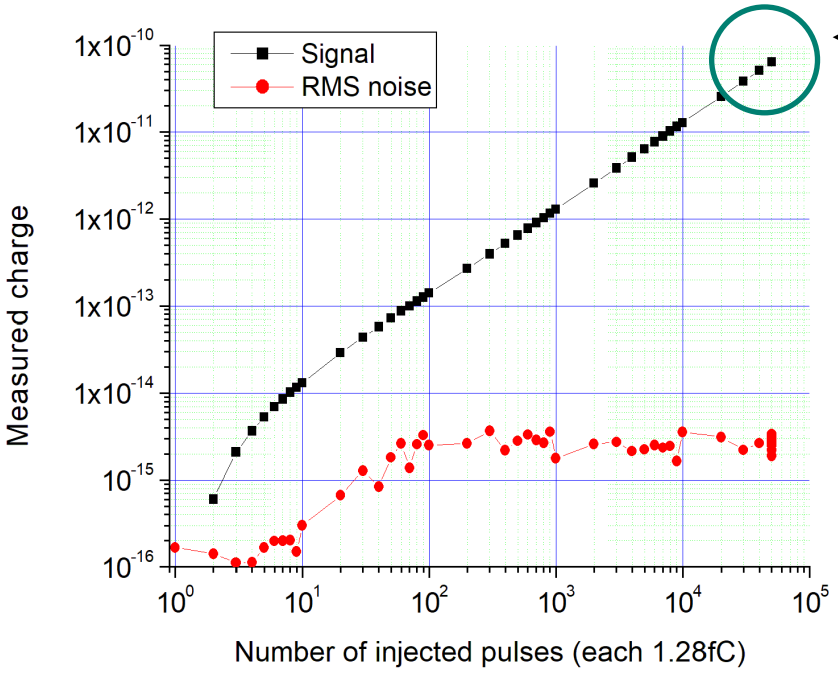
Measured charge vs. number of injected signals

- Noise stays constant

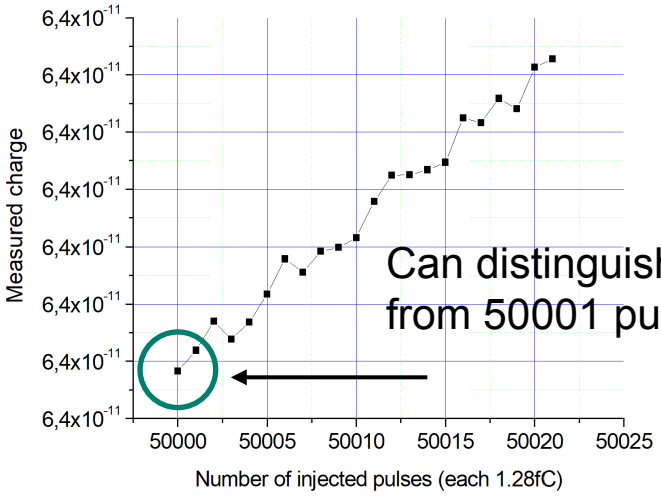


Measured charge vs. number of injected signals

- => High SNR



Zoom in to the high SNR range



Can distinguish 50000 from 50001 pulses.

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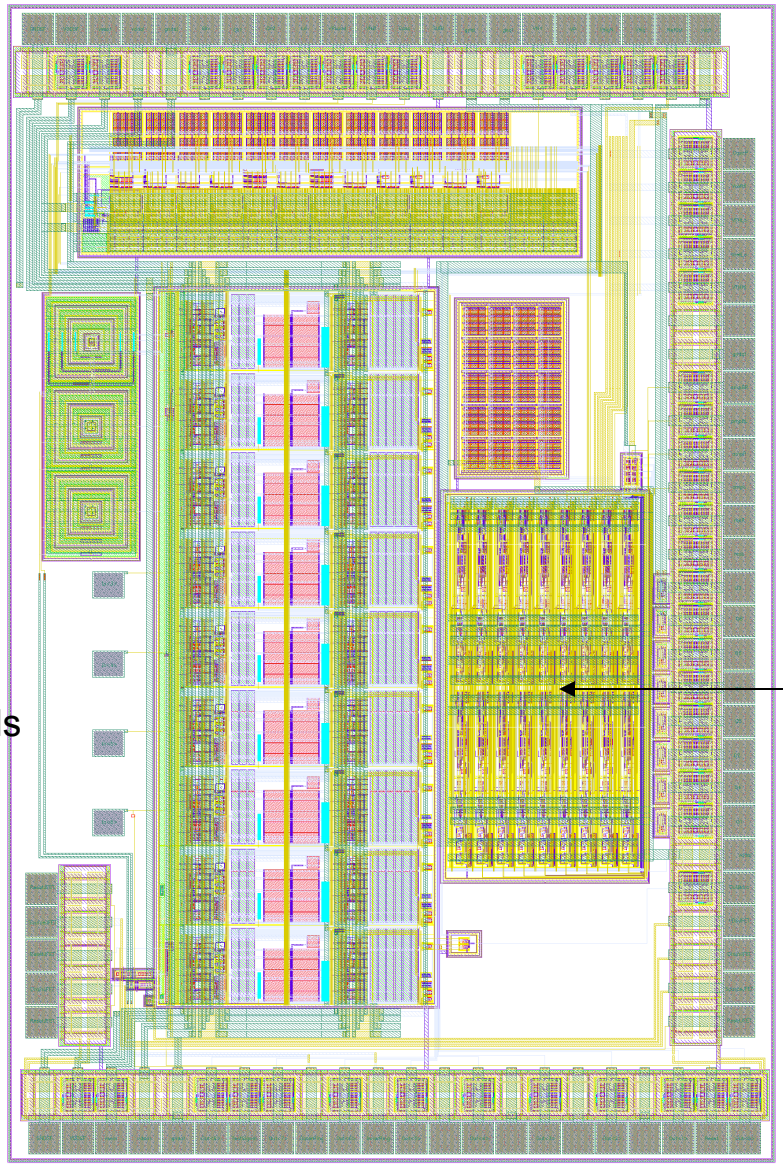
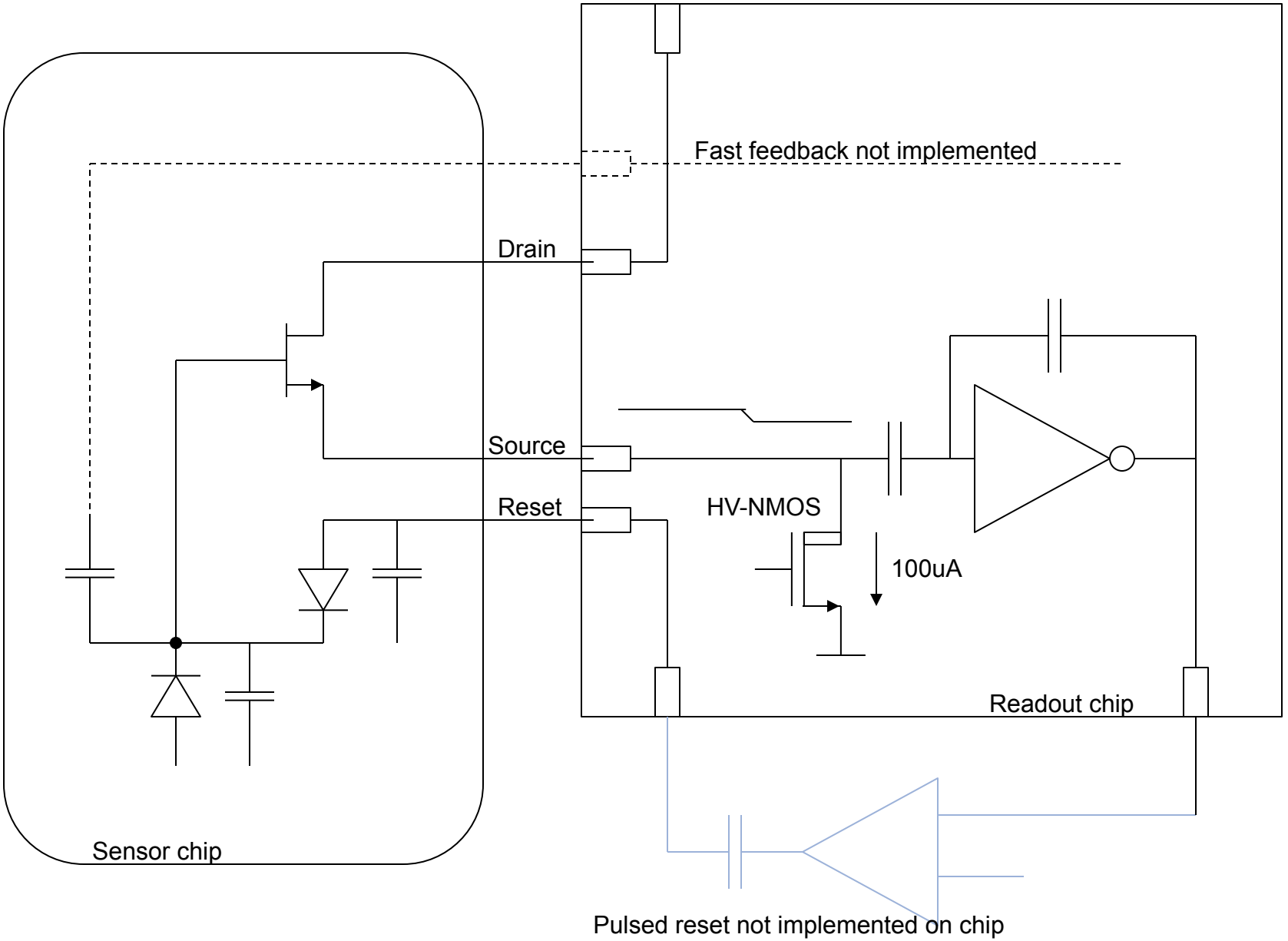

ADC
Passive SDD channels
JFET channels

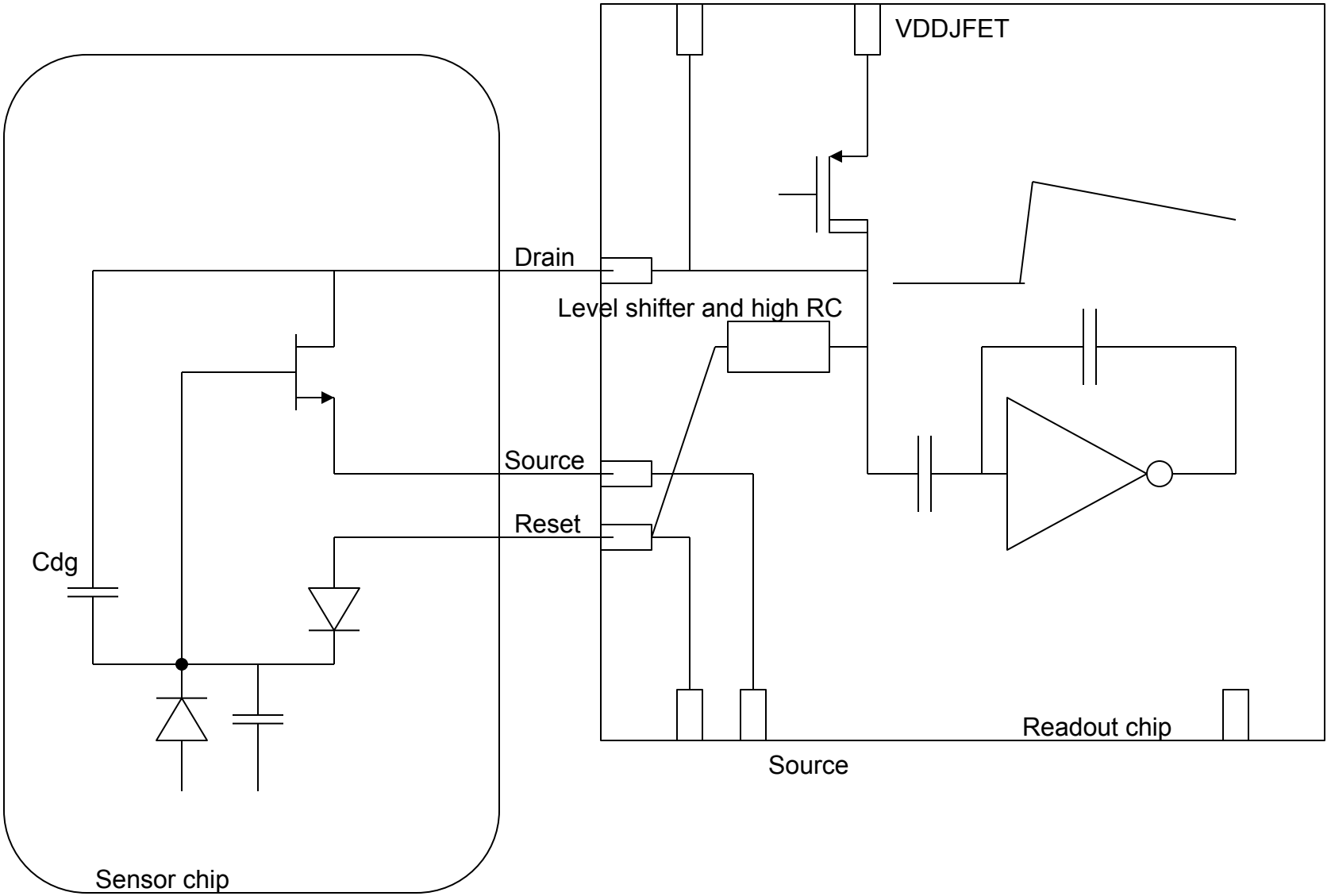
SDD Readout IC

- SDD Readout Integrated Circuit
- Features:
- 8 electronic channels: CSA with active/passive shaper
  - 1 channel for passive SDD with positive signal (hole collection)
  - 2 channels for passive SDD with negative signal (electron collection)
  - Constant current continuous reset
  - Pulsed (charge subtraction-) and continuous reset
- 2 channels for SDD with integrated JFET
  - The JFET-RO channels support 1. source follower readout and 2. common source readout with drain feedback
- 3 channels attached to on-chip sensors
- 2 passive- and one active- on-chip drift diodes
- One 9 bit pipeline ADC (extendable to provide more bits)

Readout channel 1 – source follower



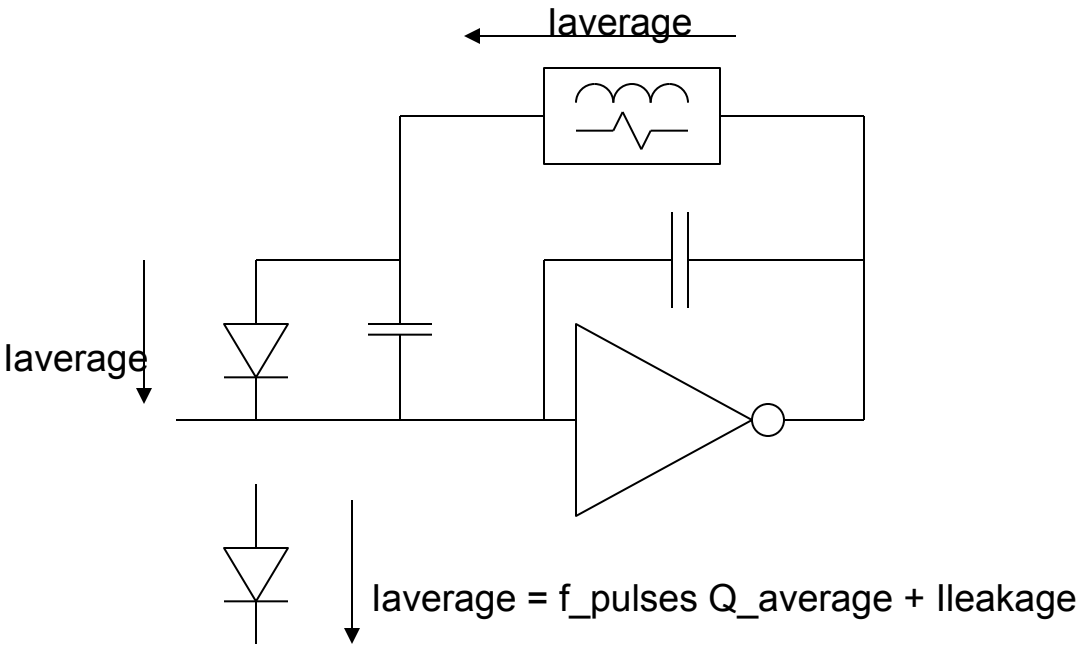
Readout channel 2 – common source



Common source readout

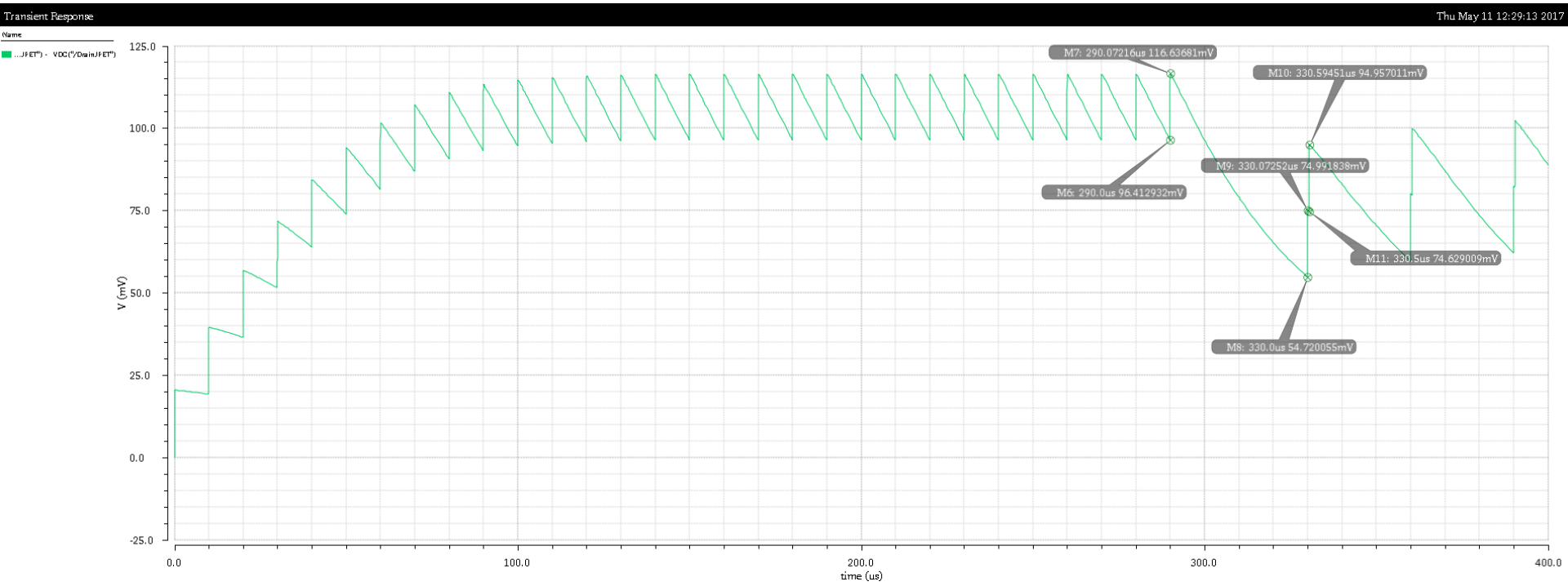
- Common source readout – advantages:
- Fast feedback can be implemented on detector chip – one line less needed
- Signals of higher amplitudes are transmitted – less sensitive to pickup of noise
- Easy implementation of constant current continuous reset
- No need for pulsed reset
- Possible disadvantage – nonlinearity of Cdg

- Constant current continuous reset “C3R”



C3 reset

- C3R simulation:
- Particle hits with average rate of 10µs, one time gap of 30µs, one time gap of 0.5µs (5% probability to happen)
- Comparison of amplitudes: 20.224mV, 20,272mV, 20.328mV -> small nonlinearity



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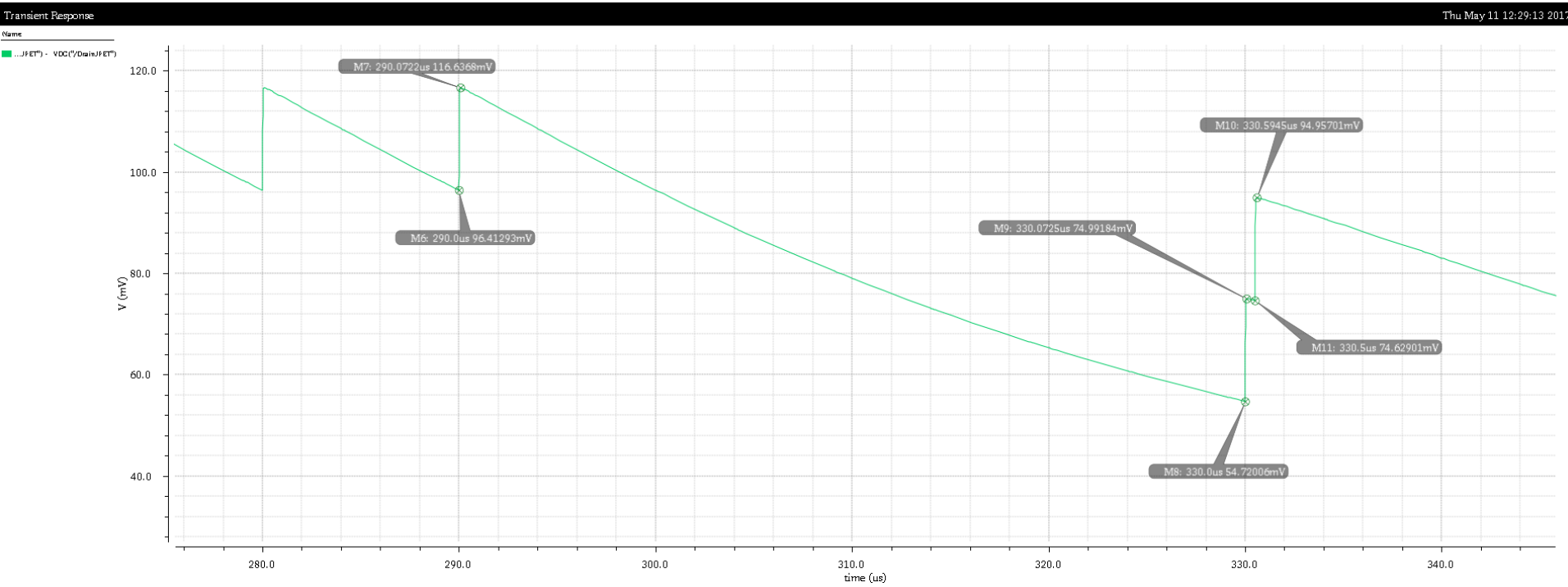
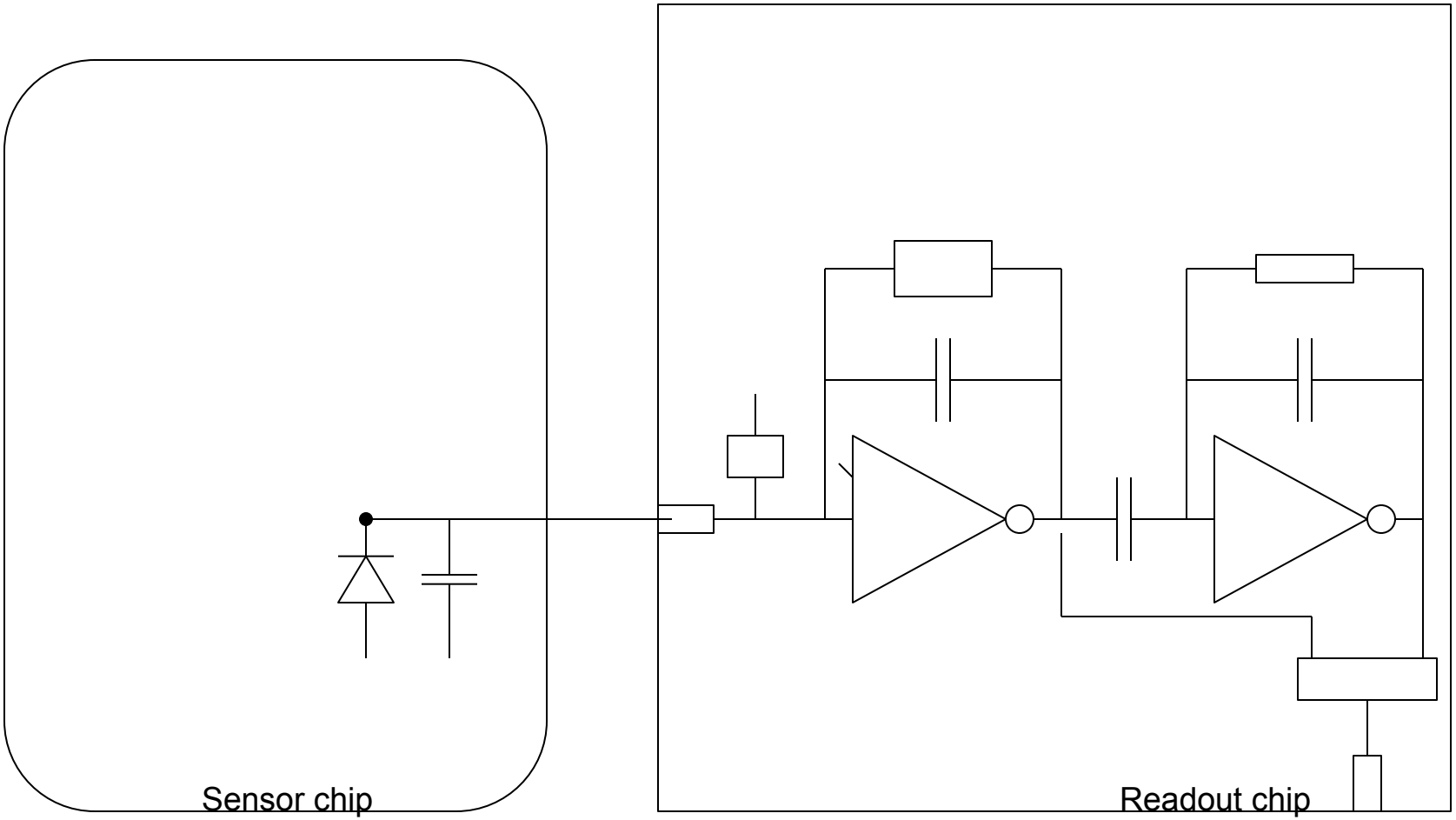
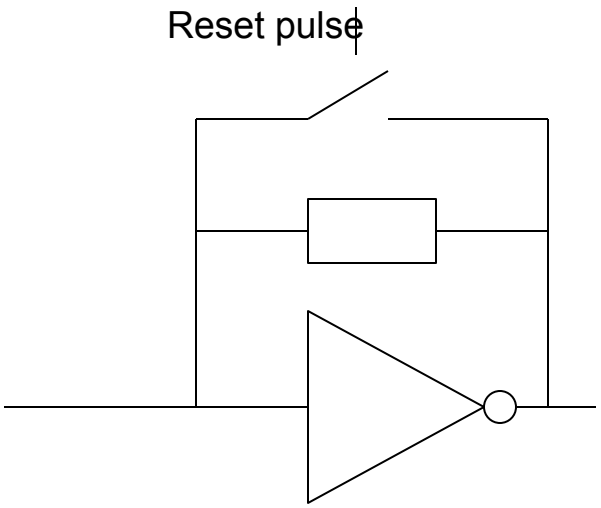


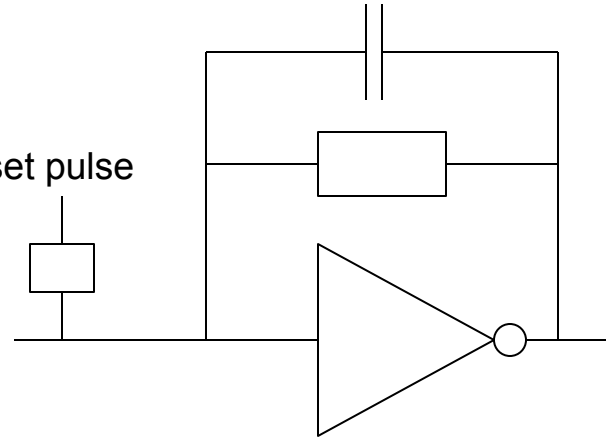
Readout channels 3-5



Charge subtraction reset



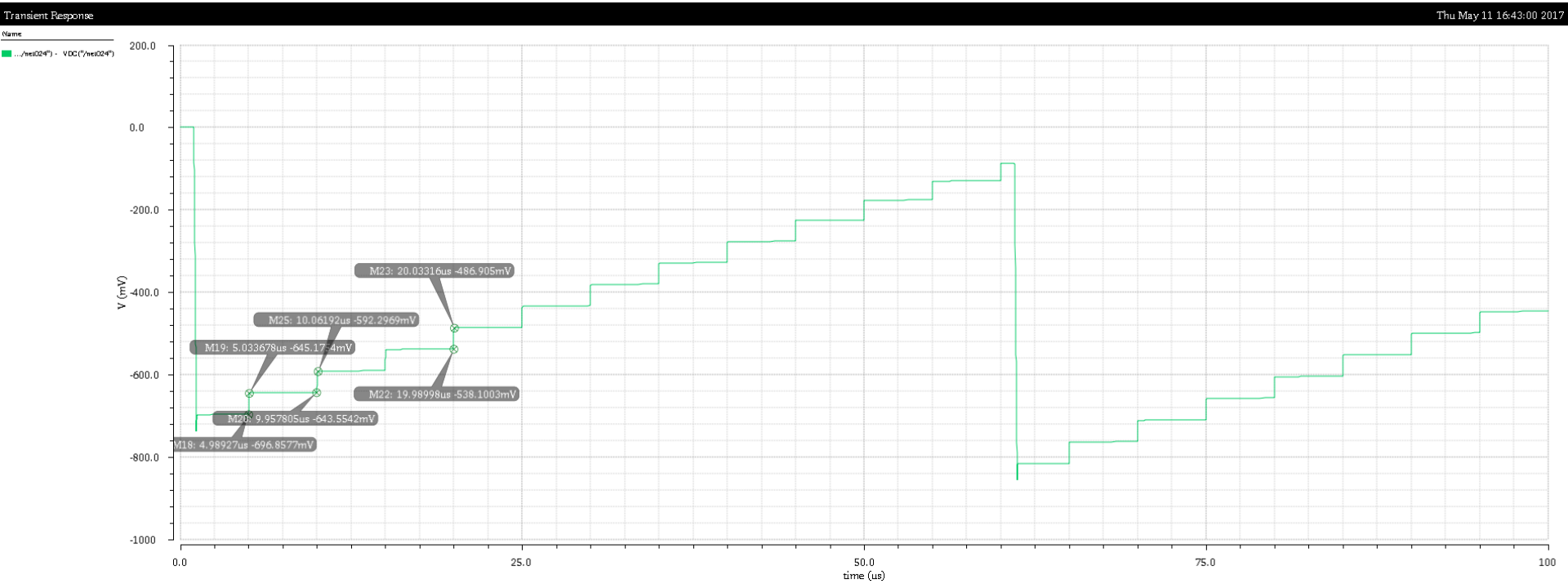
Not implemented



Implemented

Charge subtraction reset

- Charge subtraction reset: simulation
- Particle hits with average rate of 5µs
- Comparison of amplitudes: 51.7mV, 51.3mV, 51.2mV -> small nonlinearity



Charge subtraction reset

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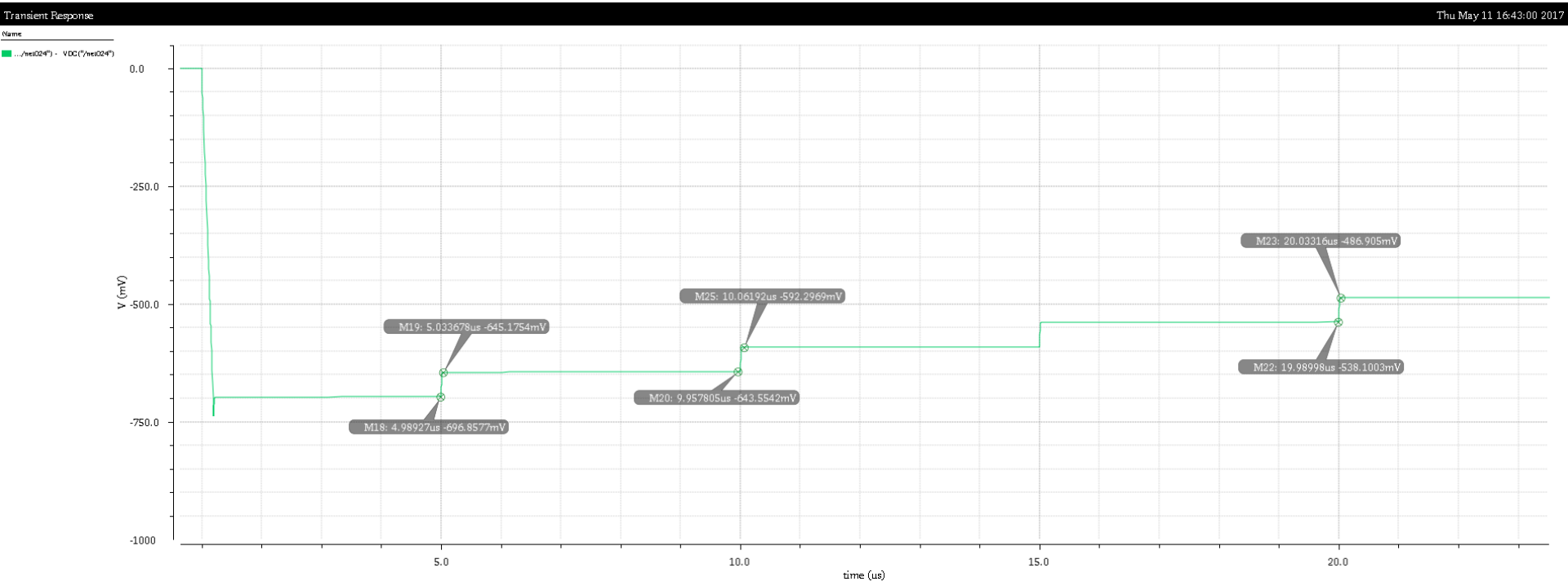
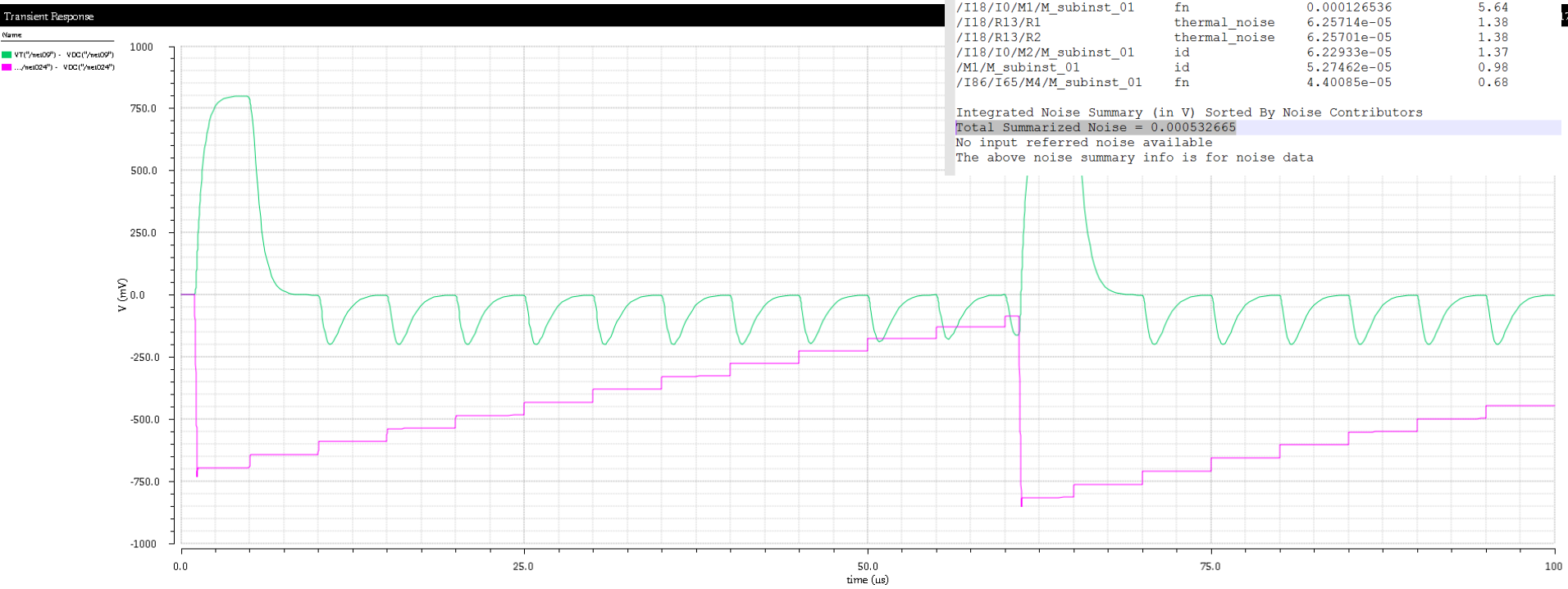


Charge subtraction reset

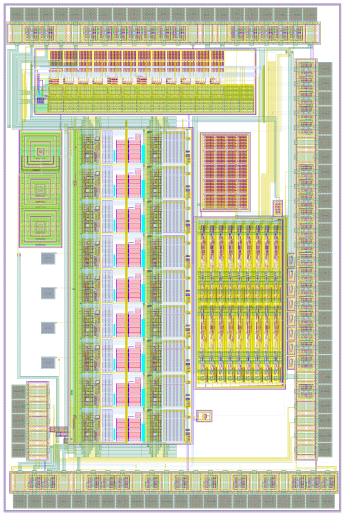
- Charge subtraction reset: simulation
- Particle hits with average rate of 5µs
- Noise after on chip analog shaper: 0.53mV, signal 200mV for 1660eV input, Cdet 100fF

Device	Param	Noise Contribution	% Of Total
/I18/I0/M1/M_subinst_01	id	0.000292307	30.11
/I18/M0/M_subinst_01	id	0.000242218	20.68
/I18/I0/M3/M_subinst_01	id	0.000215393	16.35
/I18/I0/M3/M_subinst_01	fn	0.000209019	15.40
/I18/I0/M1/M_subinst_01	fn	0.000126536	5.64
/I18/R13/R1	thermal_noise	6.25714e-05	1.38
/I18/R13/R2	thermal_noise	6.25701e-05	1.38
/I18/I0/M2/M_subinst_01	id	6.22933e-05	1.37
/M1/M_subinst_01	id	5.27462e-05	0.98
/I86/I65/M4/M_subinst_01	fn	4.40085e-05	0.68

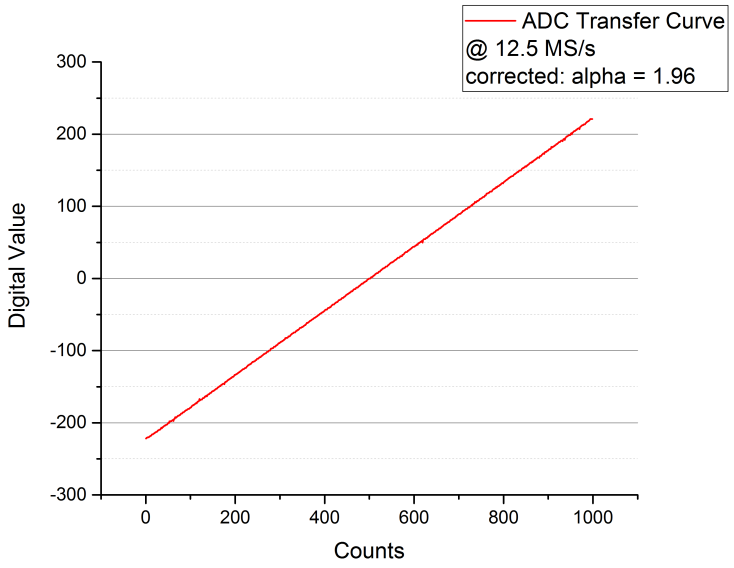
Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000532665
No input referred noise available
The above noise summary info is for noise data

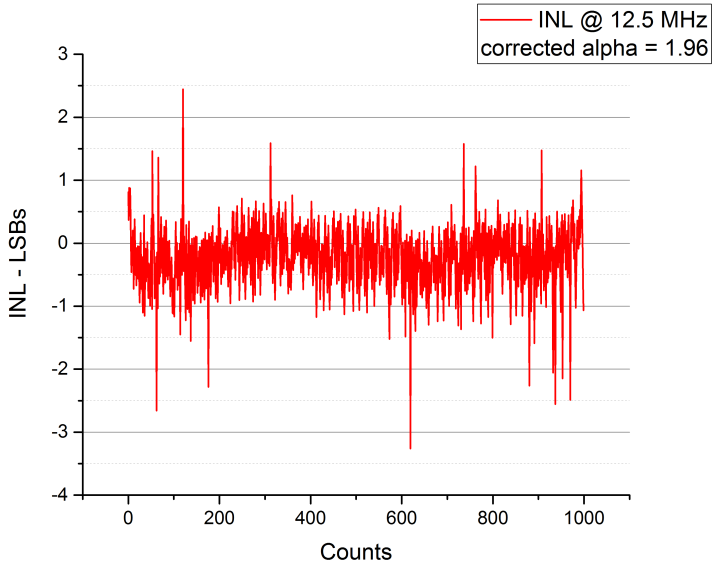


- 3 prototypes
- 8/9 channels (amplifier and shaper)
- Pipeline ADC (9-bit, 50MHz)



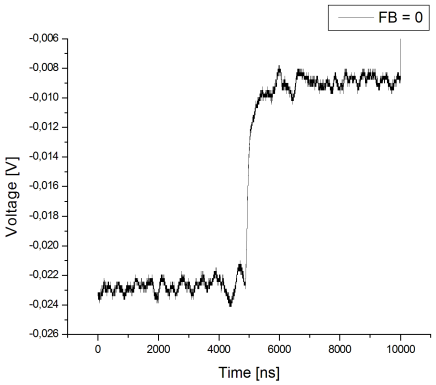
- Measurement results (first prototype)
- ADC works as expected

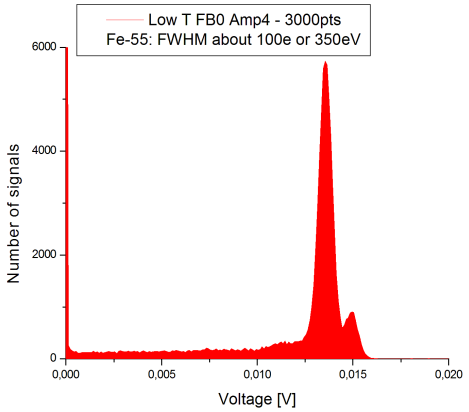




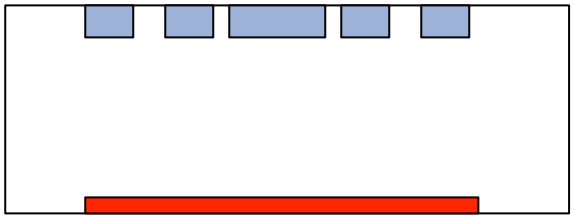
- Measurement results (first prototype)
- 7+1 channels, ceramic PCB, HLL drift diode with thin entrance window
- Readout system based on Atlys FPGA board, DAQ software in Scala, oscilloscope measurement (without external amplifier), waveform recording (as csv files) and offline (software-based) filtering
- Simple filtering used - average of the waveform calculated before trigger and subtracted from the average after trigger. This corresponds to a trapezoidal filter with a shaping time of about 6µs

- Fe-55 measurement, cooled in an normal refrigerator
- 100k waveforms recorded
- Digital filter applied
- Noise about 350eV FWHM
- Noise highly temperature dependent

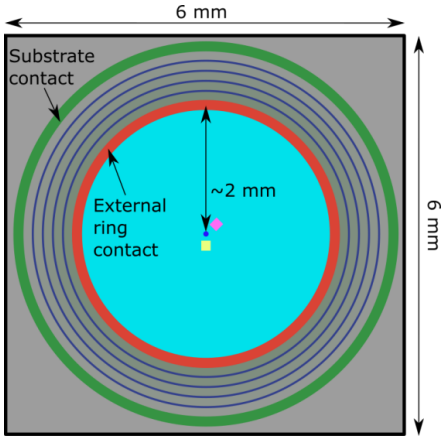




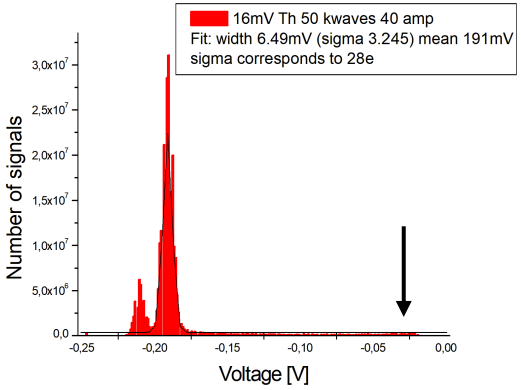
- Readout ASIC, third version
- 8+1 channels, normal PCB, FBK diode with thin entrance window
- Readout system based on Nexys FPGA board, DAQ software in C++(Qt), oscilloscope measurement (without external amplifier)
- On chip shaper used, maximum of the signal is histogrammed

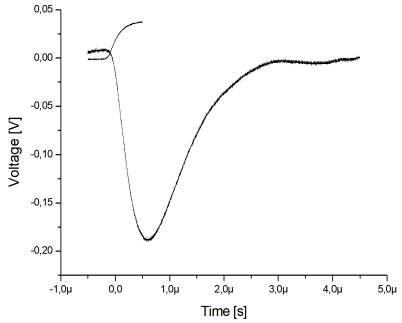


Thin entrance window



- Fe-55 measurement, room temperature
- 50k waveforms recorded
- Only waveform minimum recorded
- Noise about 240eV FWHM (28e)
- From noise peak 152eV FWHM (18e)
- Threshold 500eV





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- Faster sampling rate: Motivation belle upgrades, try to cope with occupancy
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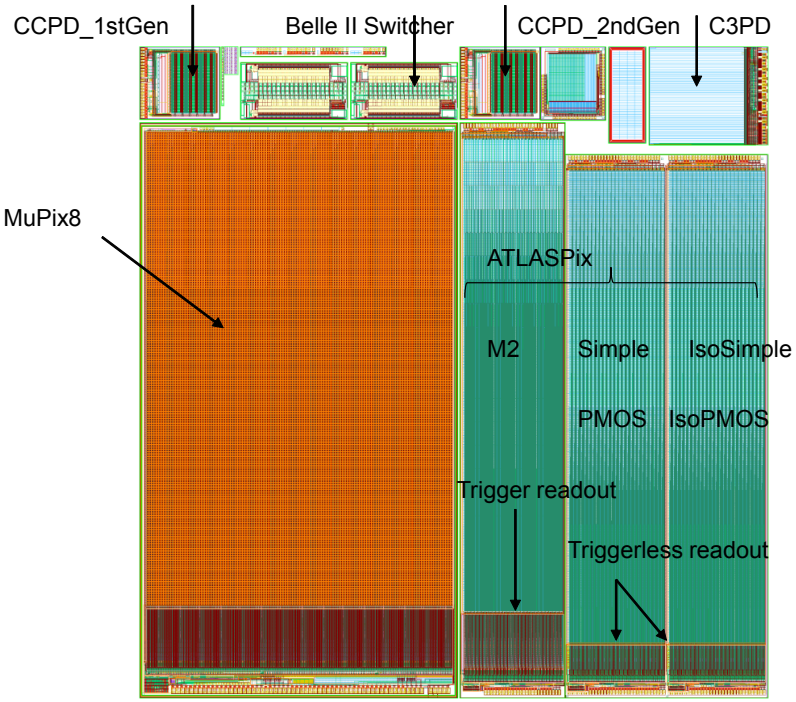
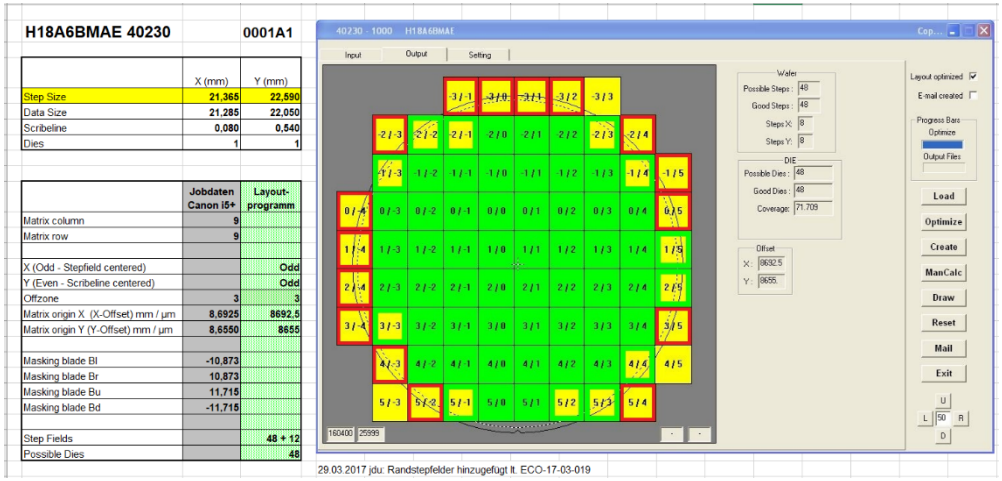
- Modified SWITCHER design - SWITCHERBa18
- Technology: AMS aH18 instead of AMS/IBM H18
- Changes: Al instead of Cu for metal layers
- Submitted as a chip on HVCMOS detector run
- 4 extra wafers on standard substrate ordered: cost 17.48k€
- 4 wafers with each ~56 reticles x 2 chips
- Wafers will be bumped at IZM – one wafer already sent to IZM



MuPix, ATLASPIX



H18A6BMAE 40230 0001A1

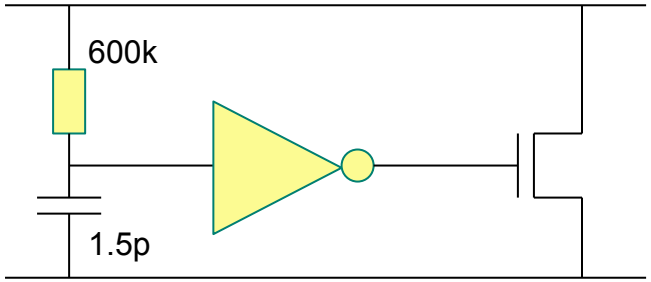
	X (mm)	Y (mm)
Step Size	21,365	22,590
Data Size	21,285	22,050
Scribeline	0,080	0,540
Dies	1	1

	Jobdaten Canon i5+	Layout-programm
Matrix column	9	
Matrix row	9	
X (Odd - Stepfield centered)		Odd
Y (Even - Scribeline centered)		Odd
Offzone	3	3
Matrix origin X (X-Offset) mm / µm	8,6925	8692,5
Matrix origin Y (Y-Offset) mm / µm	8,6550	8655
Masking blade Bl	-10,873	
Masking blade Br	10,873	
Masking blade Bu	11,715	
Masking blade Bd	-11,715	
Step Fields		48 + 12
Possible Dies		48

29.03.2017 jdu: Randstepfelder hinzugefügt lt. ECO-17-03-019

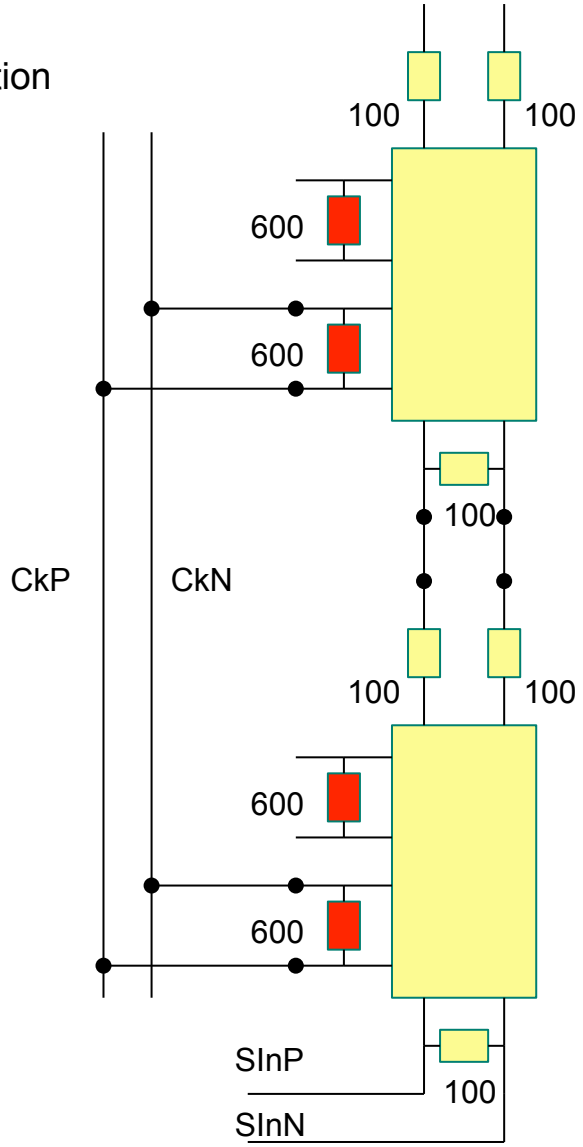
Modified SWITCHER design

- DC current consumption of a regulator halved
  - SUB DC current consumption: 2 x 360µA
- Clamp circuit added between vdd and gnd and between VddRef and SUB
- Changes in termination to allow functioning without JTAG
  - DAC LSB hard coded to 1 to work without JTAG
  - SerInN/P have hard coded 100Ω termination
  - GStrN/P, CStrN/P, CkN/P have hard coded 600Ω termination
  - Old SWITCHER design had programmable 50Ω termination
- Only one chip edge

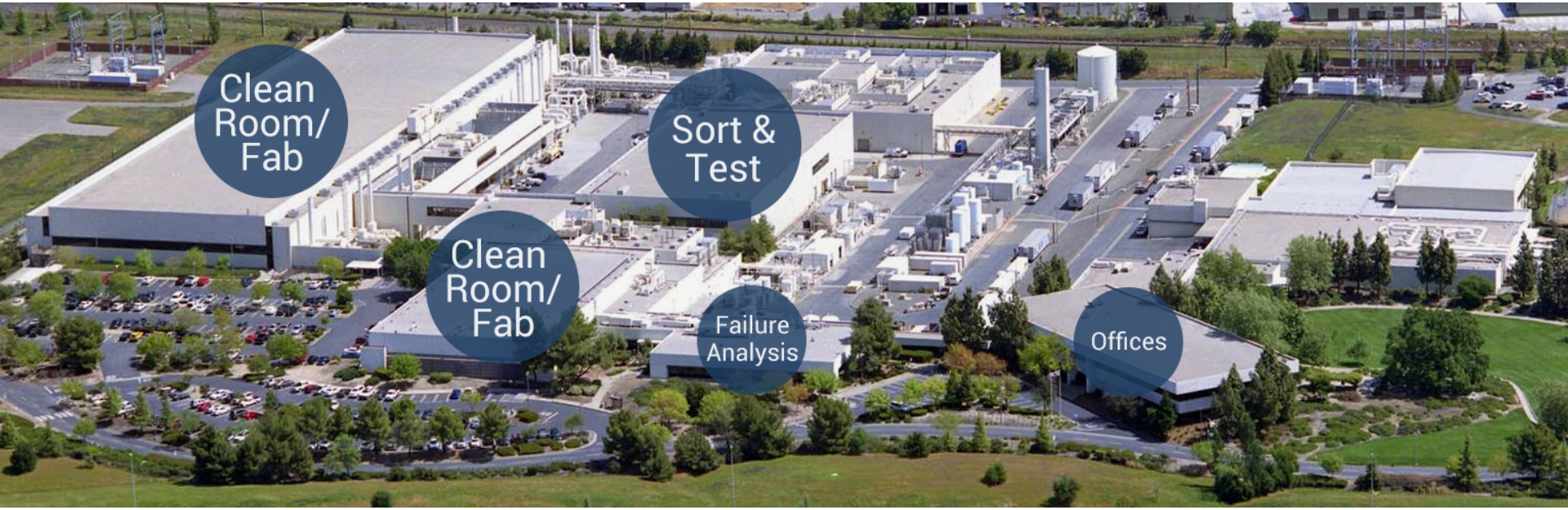


Modified SWITCHER design

- SerInN/P have hard coded 100Ω termination
- GStrN/P, CStrN/P, CkN/P have hard coded 600Ω termination



- H18 process – foundries AMS, GF/IBM, TSI
- If a new SWITCHER design is needed, it can only be submitted by TSI semiconductors
- TSI have licensed the H18 process, same layout can be submitted
- MPW and cheap engineering runs are available
- We have tested the process within HVCMOS sensor project
- It is difficult to find replacement for H18 technology, other 180nm HVCMOS processes (XFAB, ONSEMI, TSMC) use thicker gate oxides for HV transistors -> radiation tolerance may be worse



Summary

- DEPFET readout
- Possible developments (DCD)
- Lower power consumption: DCDC – DCD with SAR ADC
- Faster sampling rate: Motivation belle upgrades, try to cope with occupancy
  - Example 50ns instead 100ns (256 channels), faster is also possible (time interleaving)
- Implementation of fast LVDS links: motivation DCD to FPGA direct connection
  - Example: 1.6 G bit/s each, 8b10b, 16 such links are equivalent to 64 CMOS links (we have now)
- DCD with extended dynamic range: Motivation diffraction experiments (Electrons, x-rays)
  - Example sampling time 512ns – linear dynamic range ~16 000, generally: dynamic range = time^2
- SWITCHER improvements
  - E.g. with more channels
- Drift diode readout
  - Multichannel amplifier chip for drift diodes or drift diodes with JFET

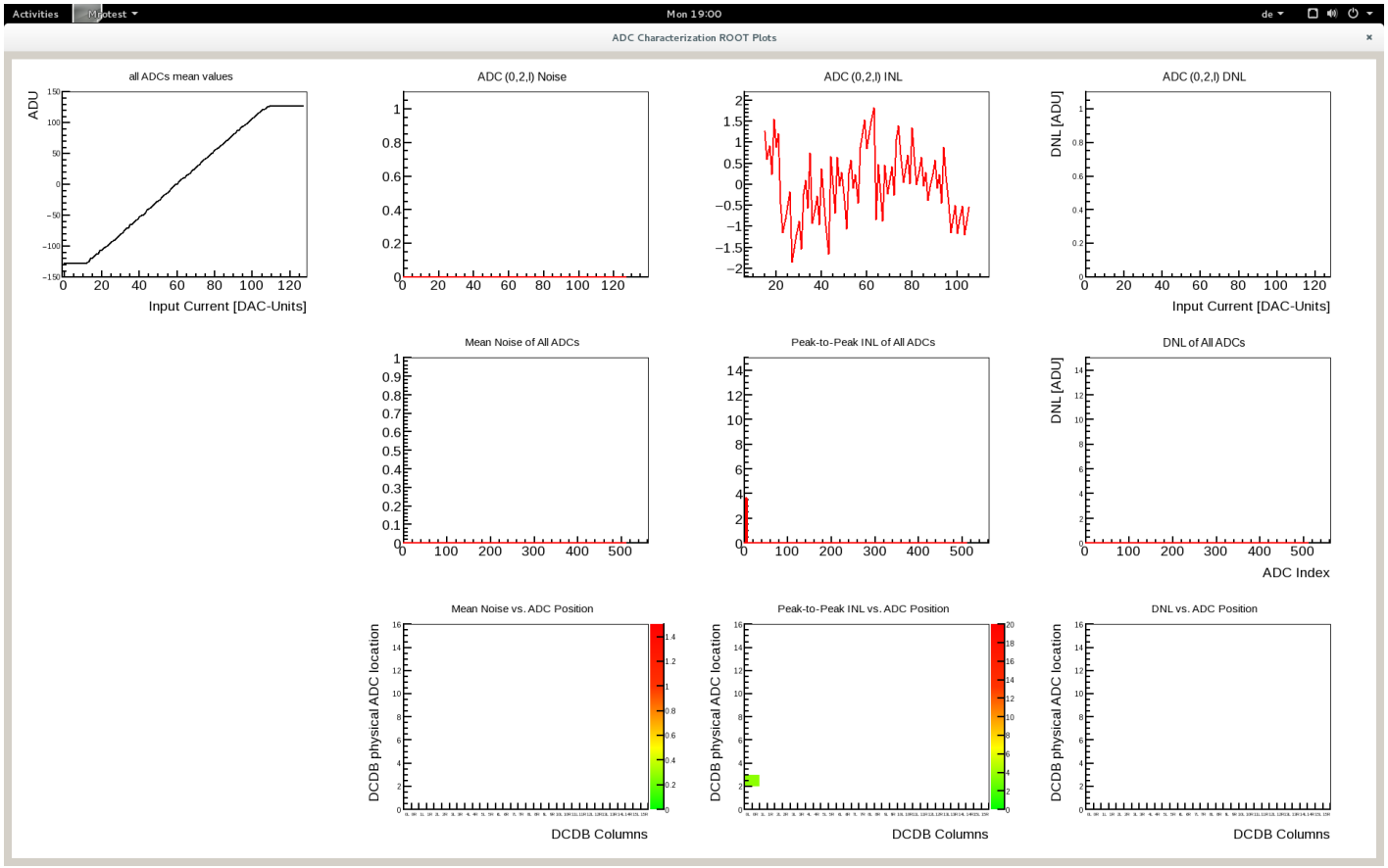
- Thank you

- Backup slides

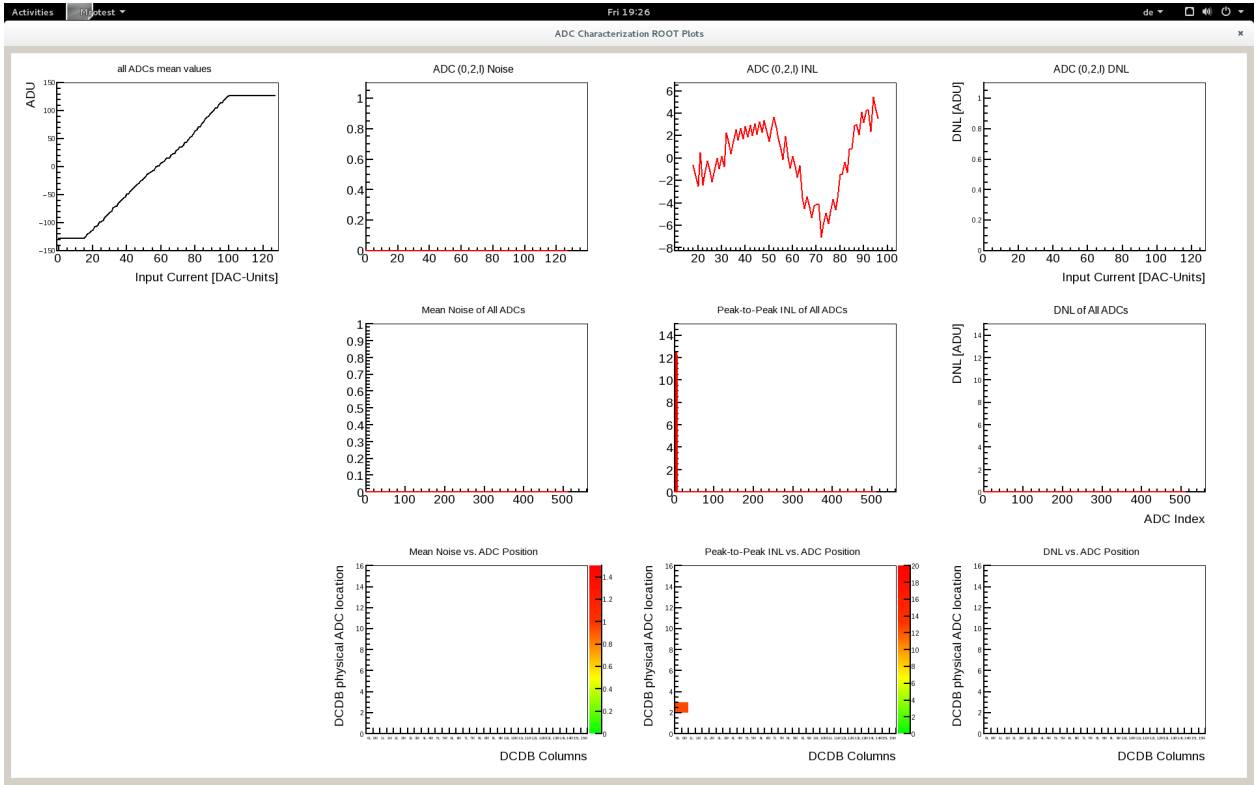
DCDC

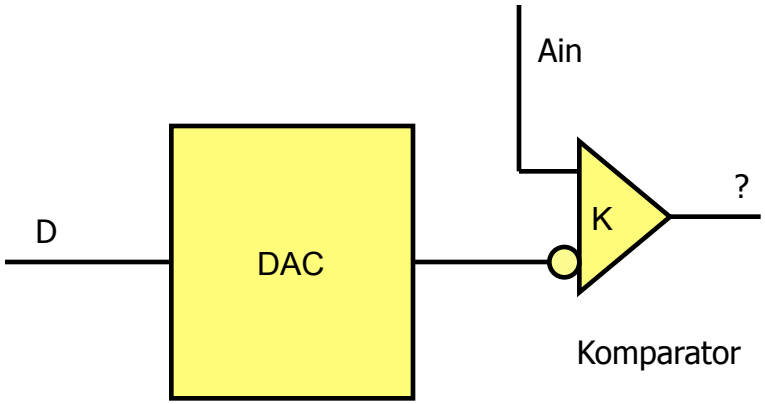
- DCDC chip is based on capacitive SAR ADC
- Front end is the same as for DCDB4.2
- DCDC is fully compatible (pins, configuration, readout) with DCDB4.2
- Several DAC settings are different (only three DAC settings needed for analog part of ADC)
- No RefIn current consumption (used as threshold)
- Radiation tolerant design
- It was measured on probe station with PC22
- Measurement frequency was between 100MHz and 320MHz
- Analog power consumption 75mA (where DCDBv2 has 300mA)
- Power consumption per chip about 350mW

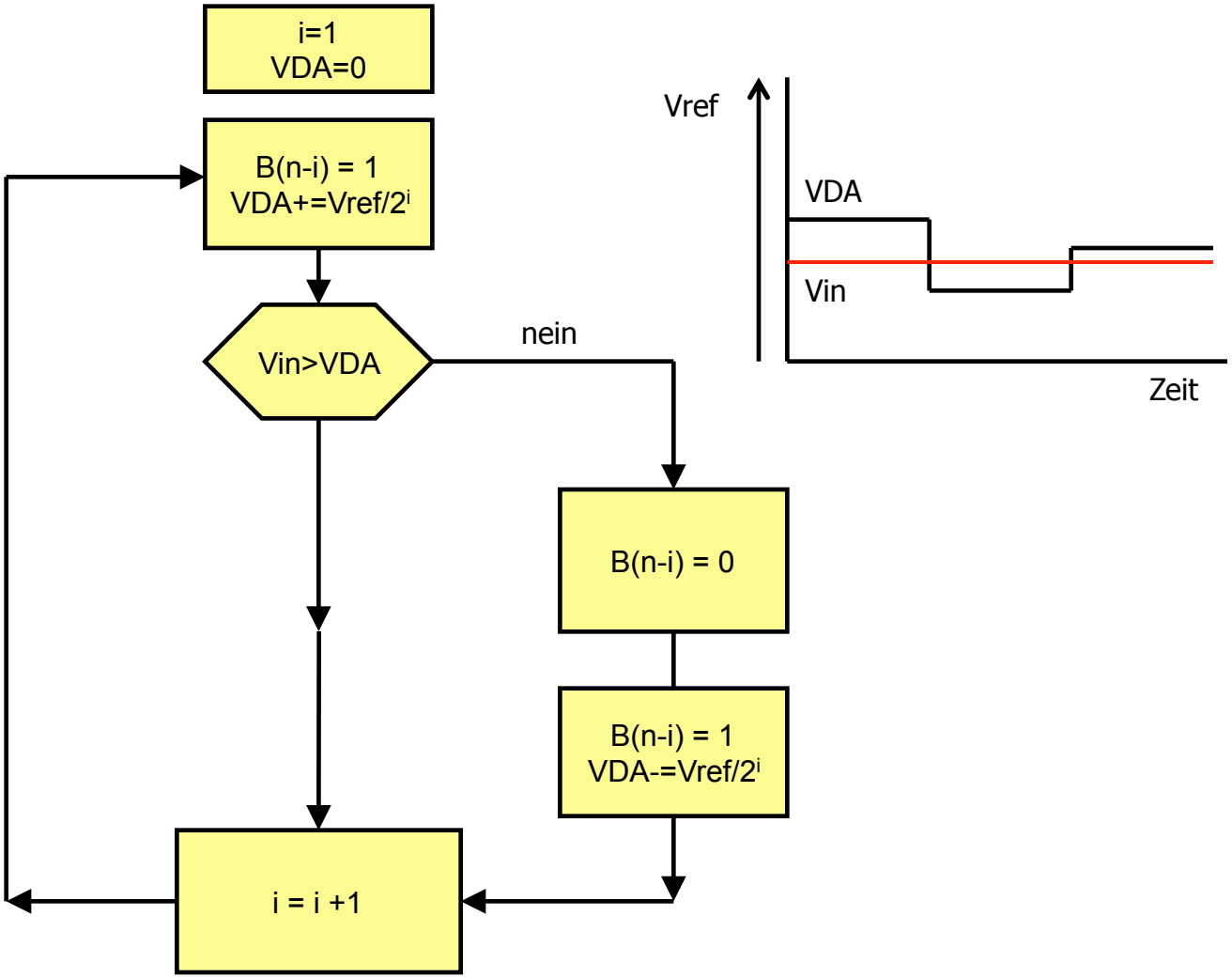
- Measurement with Heidelberg PC with SPARTAN FPGA – good linearity – 100MHz

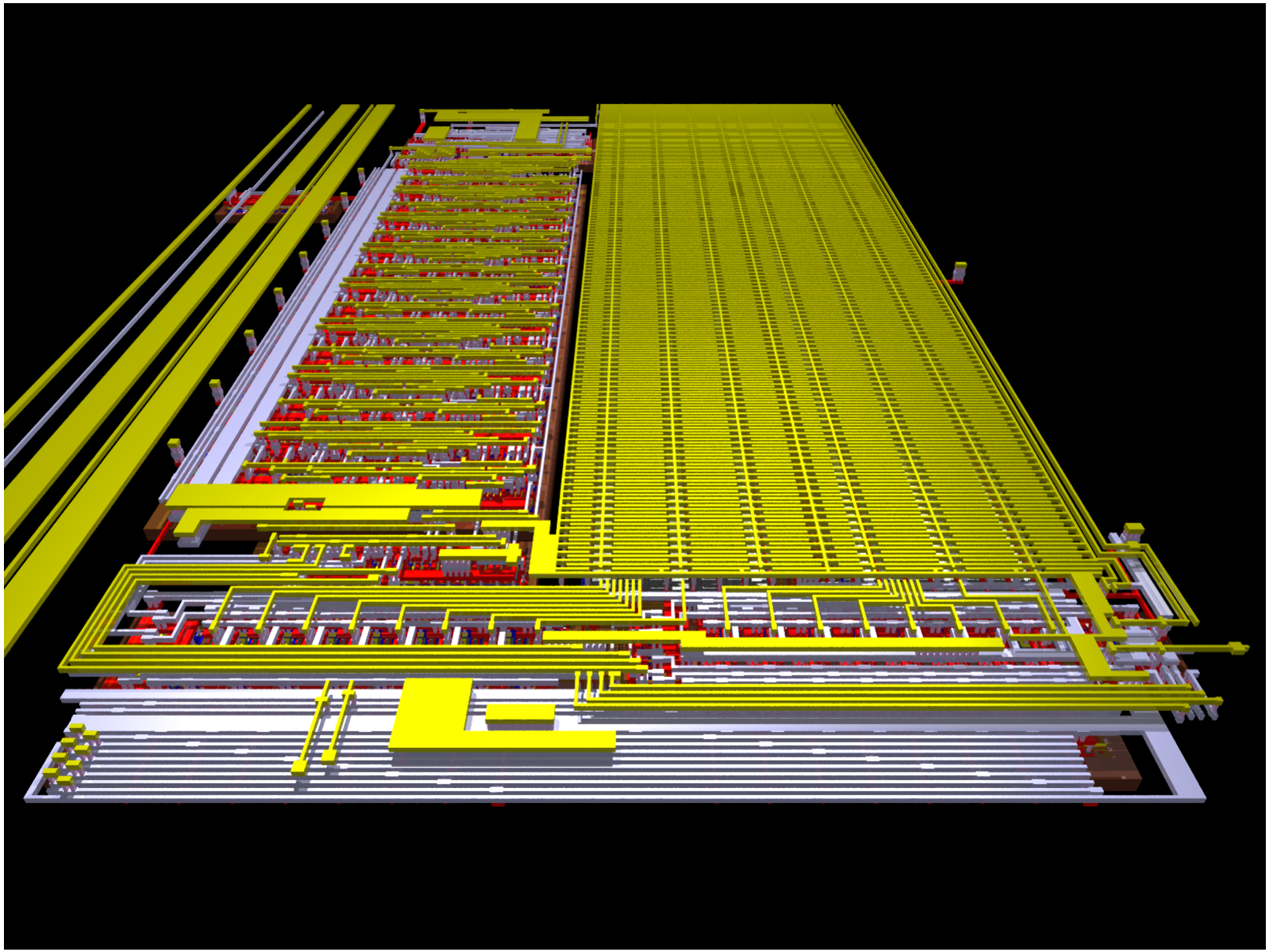


- Measurement with PTSL PC22 with faster NEXYS FPGA – 320MHz
- Nonlinearity is probably caused by the contact problems – not an issue of DCD and speed
- PC22 shows nonlinearities even at frequencies where Heidelberg PC makes nice linear ADC lines




Ain
D
DAC
K
?
Komparator


i=1
VDA=0
B(n-i) = 1
VDA+=Vref/2^i
Vin>VDA
nein
B(n-i) = 0
B(n-i) = 1
VDA-=Vref/2^i
i = i +1
Vref
VDA
Vin
Zeit



DCDC

- New DCD chip based on capacitive SAR ADC was successfully tested at probe station at full speed
- Front end is the same as for DCDB4.2
- DCDC is fully compatible (pins, configuration, readout) with DCDB4.2
- Several DAC settings are different (only three DAC settings needed for analog part of ADC)
- No RefIn current consumption
- Reduced power consumption by 500mW
- Radiation tolerant design