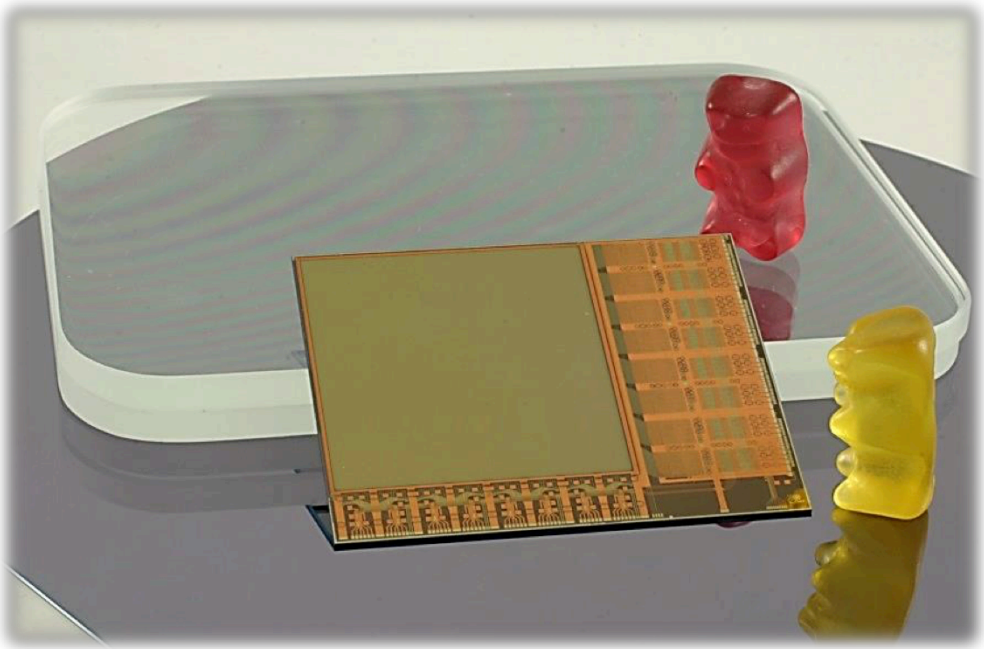
EDET Hardware Component Development Status

Ringberg castle, 12.3.2019

J. Treis
on behalf of the EDET collaboration
MPG Semiconductor Laboratory



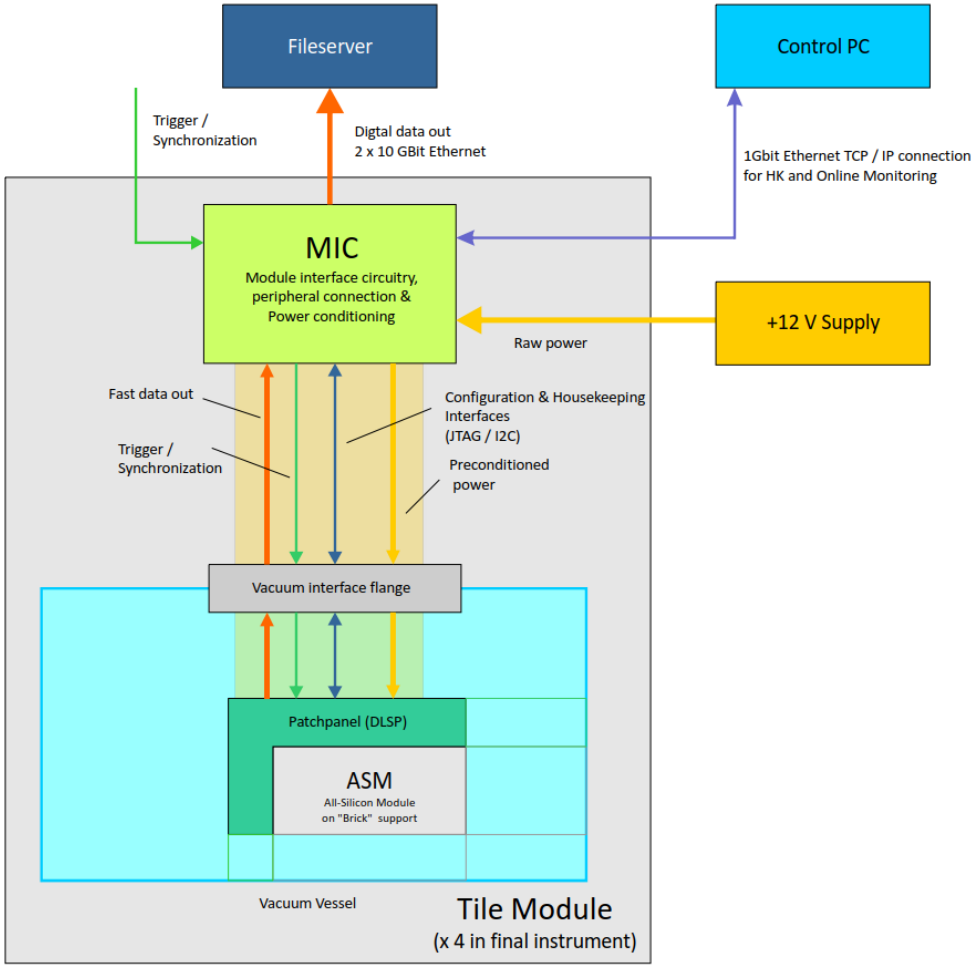
Contents

- System components
- Component development status
- Critical aspects
- Configurations
- Timeline estimate
- Summary & Outlook

System components

Module structure:

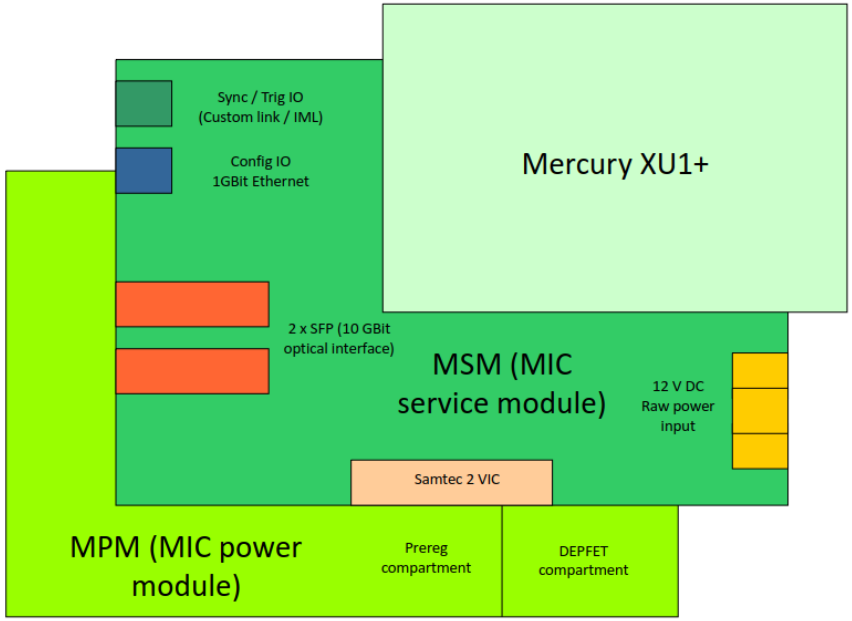
- ASM: All-Silicon module
- Brick support: Mechanical and thermal support for ASM and interface to main heatsink
- Patch panel: Wire bond adapter, local power conditioning and housekeeping circuitry
- Integrated with 3 other tile modules on main heatsink in vacuum vessel
- Vacuum interface flange with flexlead for electrical connection
- Connected to Module Interface circuitry for peripheral connection
- All hardware components of tile module
- Communication w/ control PC for housekeeping and online monitoring using 1 GBit Ethernet interface
- Trigger input from TEM and synchronization clock
- Fileserver system for fast data storage, data transfer using 2 x 10 GBit optical interface (UDP stream)
- Supplied with a single 12 V raw power supply

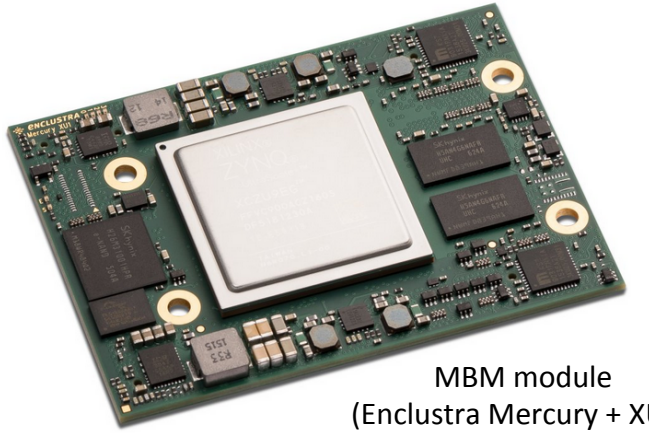


Module structure

Module Interface circuitry (MIC) :

- Peripheral interconnect based on modular stack of 3 modules
- **MSM:** Service module hosting physical interfaces & interconnects
  - Housekeeping & configuration
  - Fast data transfer
  - Trigger inputs
  - Connectors for Mezzanine cards
- **MPM:** Power module hosting Preregulators and biasing circuits for ASM
- Provides for supply of entire module using a two channel standard 12 V DC power supply
- **MBM:** Brain module based on powerful Zynq UltraScale FPGA from Xilinx
- Service functions, fast data transfer using MGBTs and potential data compression, buffering and preprocessing



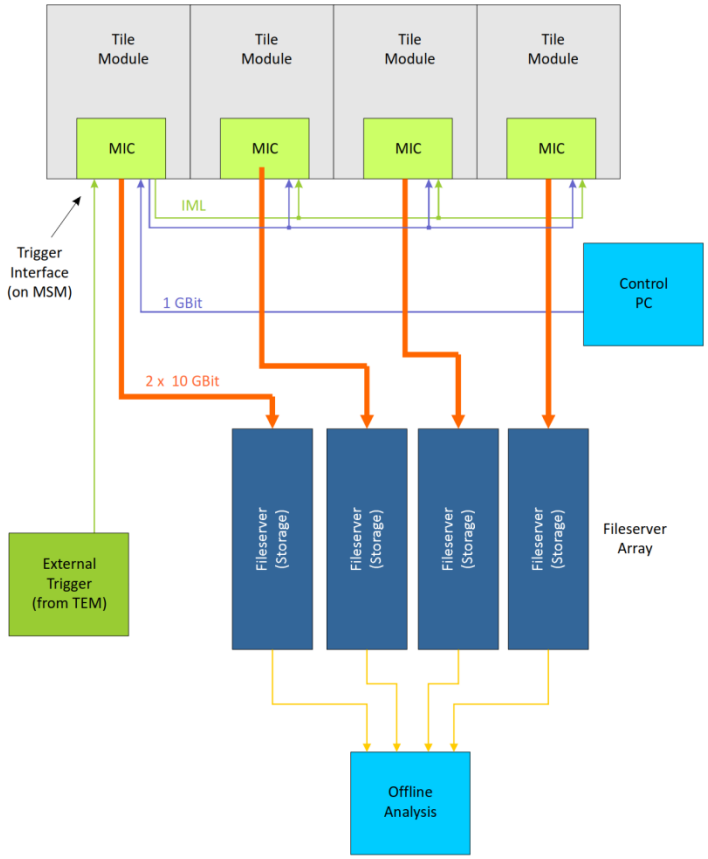


MBM module
(Enclustra Mercury + XU1)

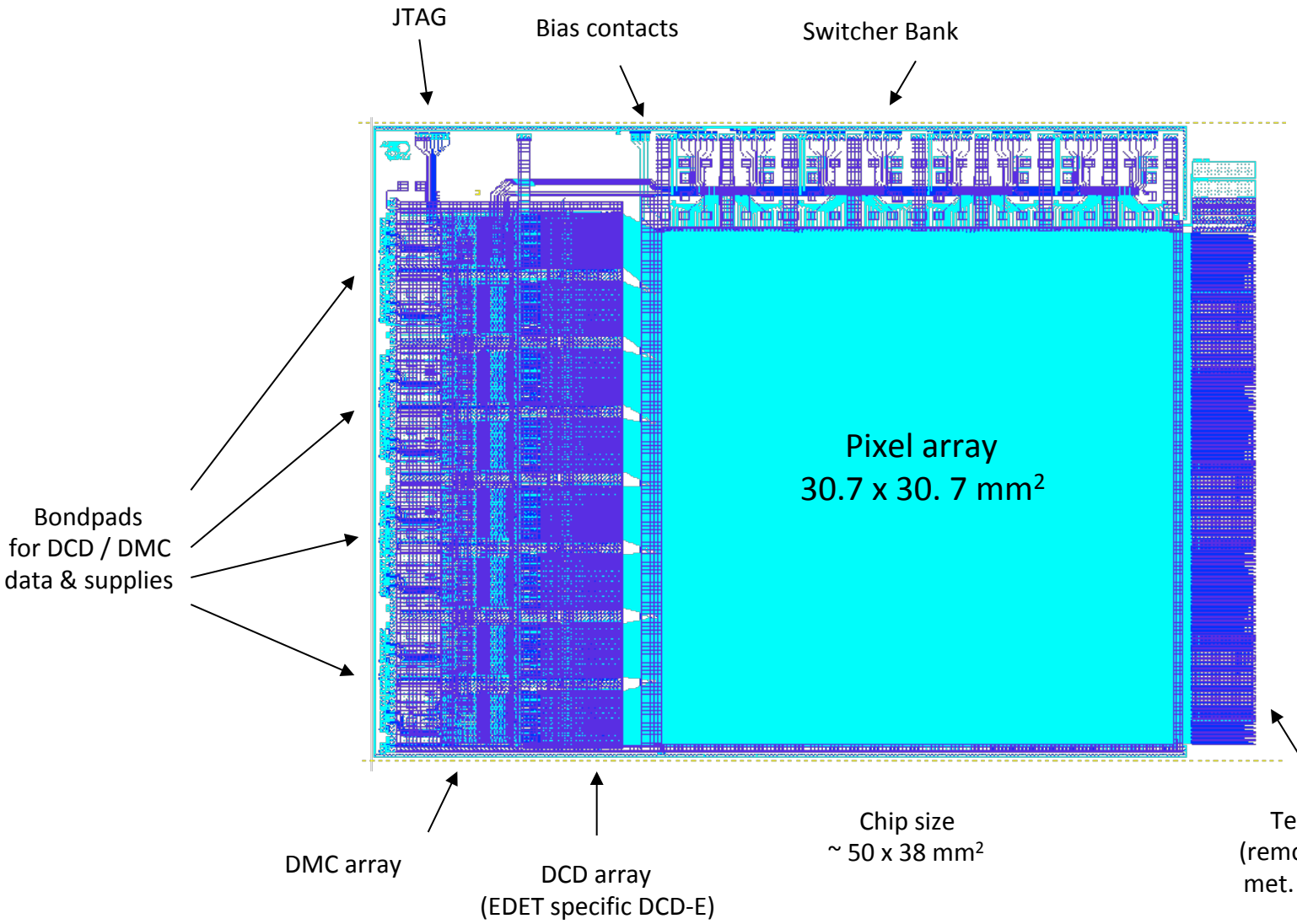
System structure

DAQ Concept:

- Complete system is formed by 4 identical, independent tile modules
- Configuration of modules via individual standard 1Gb Ethernet link
- Control PC does configuration, housekeeping and online Monitoring
- First, the trigger is distributed to the modules by trigger control unit based on MMC3 module
- Later, trigger from TEM is applied to one ("master") module
- Master distributes the trigger to slave modules using proprietary Inter-Module link (**IML**)
- Fast data is transferred to module-individual Fileserver storage using 2 optical 10 Gbit Ethernet connections
- Fileserver array makes data available for offline analysis
- Possible replacement of module-individual configuration link by IML based master-slave architecture in a later stage



Detector ASM



ASM Status

ASM pilot production finalized:

- Verify of characteristics of detectors (see talk by E. Prinker / M. Predikaka)
- Provide sufficient number of large modules to furnish full system
- Thick (450 µm) and thin (30 + 50 µm) wafers
- 3 dies populated with DHP ICs (more can be made at any time)
- Functional test possible as soon as rest of system components available

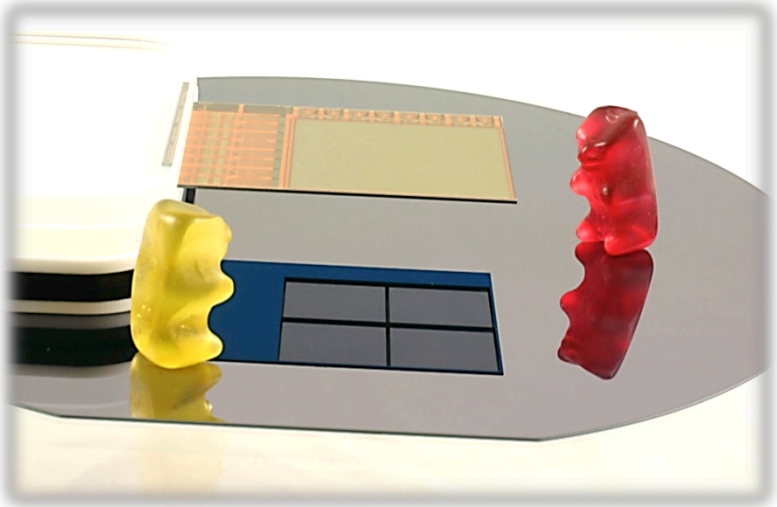
Critical aspects:

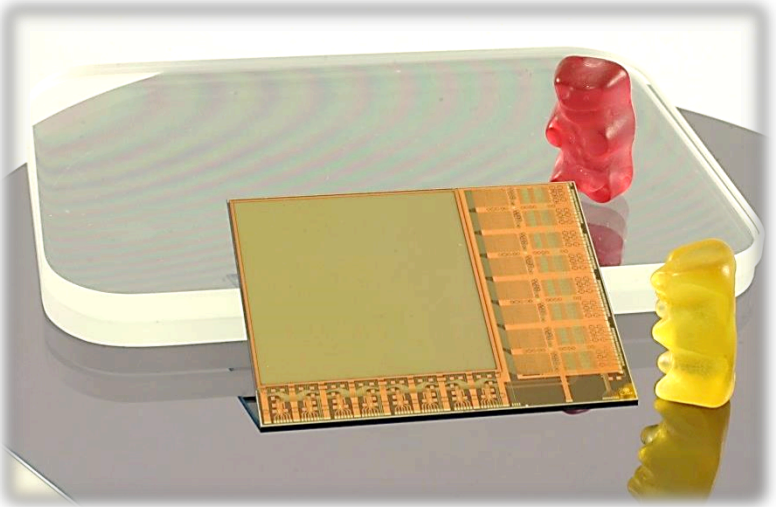
- Handling procedures
- Population w/ ASICs
- SMD population
- Single step process

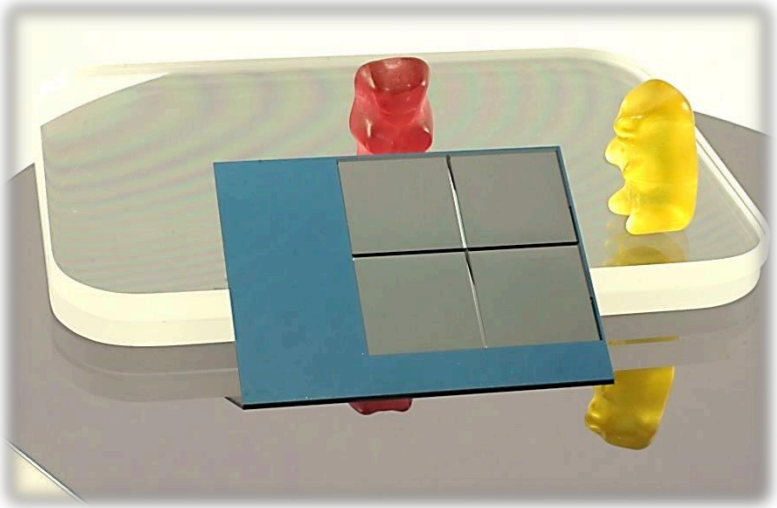
Final production:

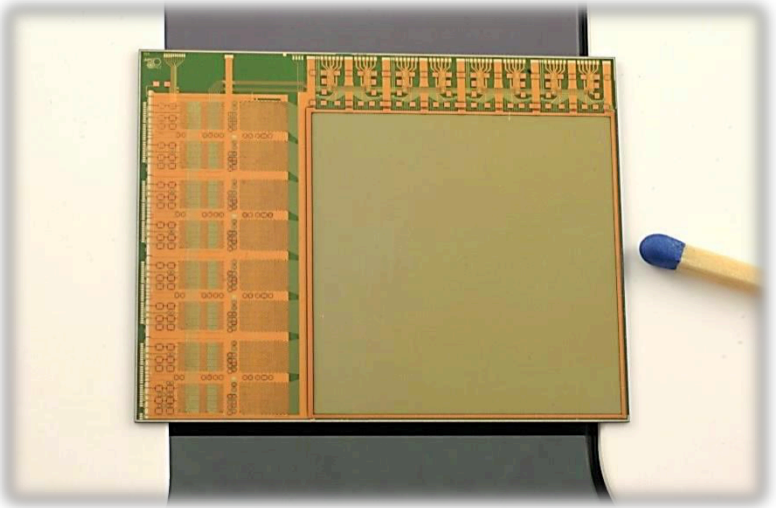
- In progress
- Will show response adapted to requirements
- Will fix (part of) yield issues w/ drain lines
- Will introduce 4 additional differential TX lines per DMC to enable full burst rate capability
- Supports additional DMC features

ASM Status

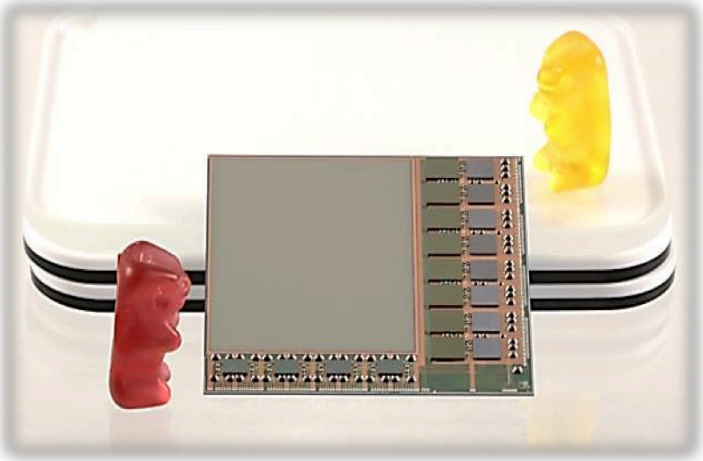


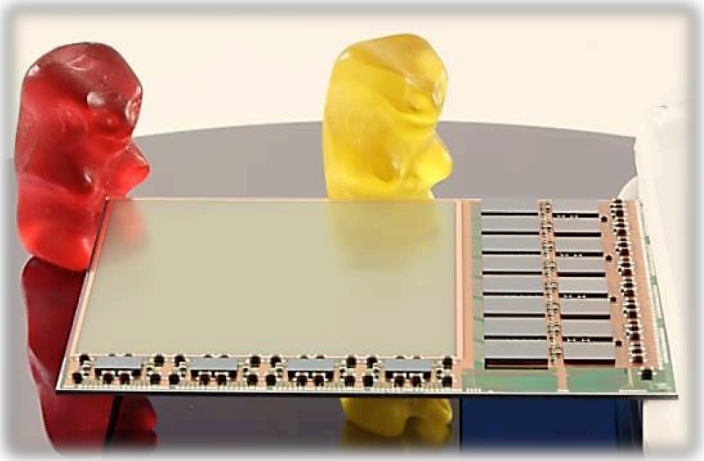


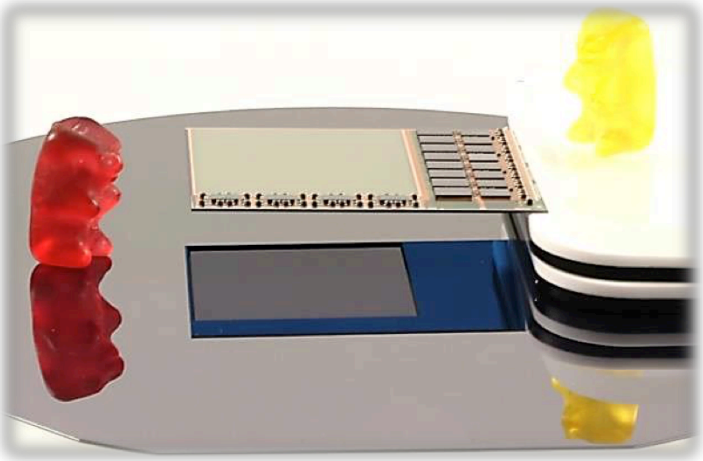


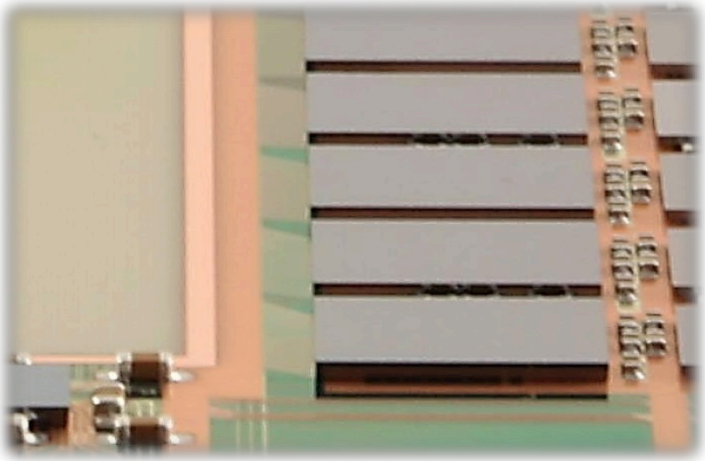


ASM Status









DLSP development

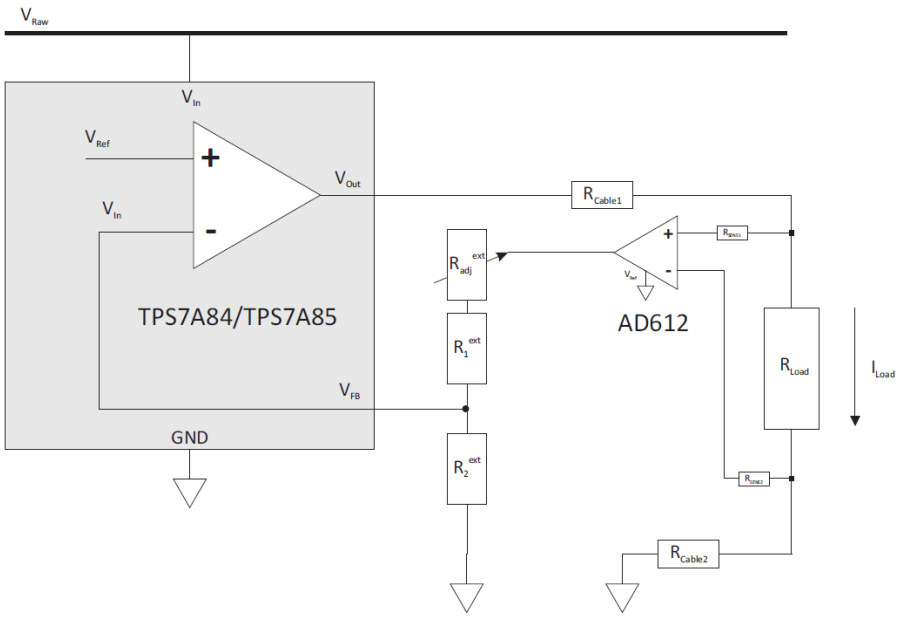
Status:

- Layout almost finished (few more days required)
- Preparatory discussions w/ vendors
- Fabrication + Population (~ 2 m)

DLSP development

Status:

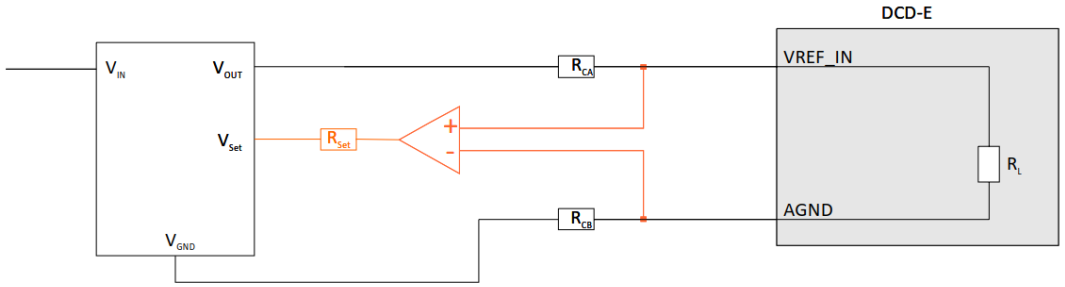
- High current LDOs required for nearly all ASM ASIC voltages
- High- and low side sensing mandatory because of finite ground resistance on ASM
- External sense amp circuit required using feedback input of regulator
- Circuit prototyped on breadboard and tested on PSP



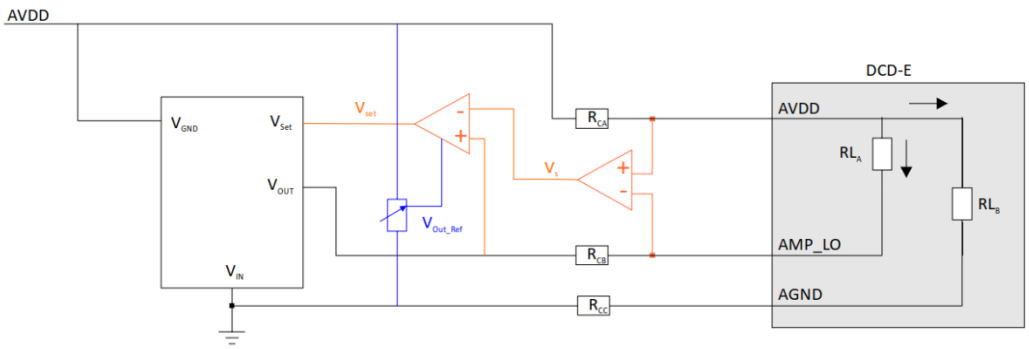
DLSP development

Status:

- Due to special requirements, different regulators required for AMP_LO (current sink from AVDD) and VREF (low voltage)
- Regulators require different feedback control mechanism
- Circuits prototyped and tested on PSP



LT3086



LT3091

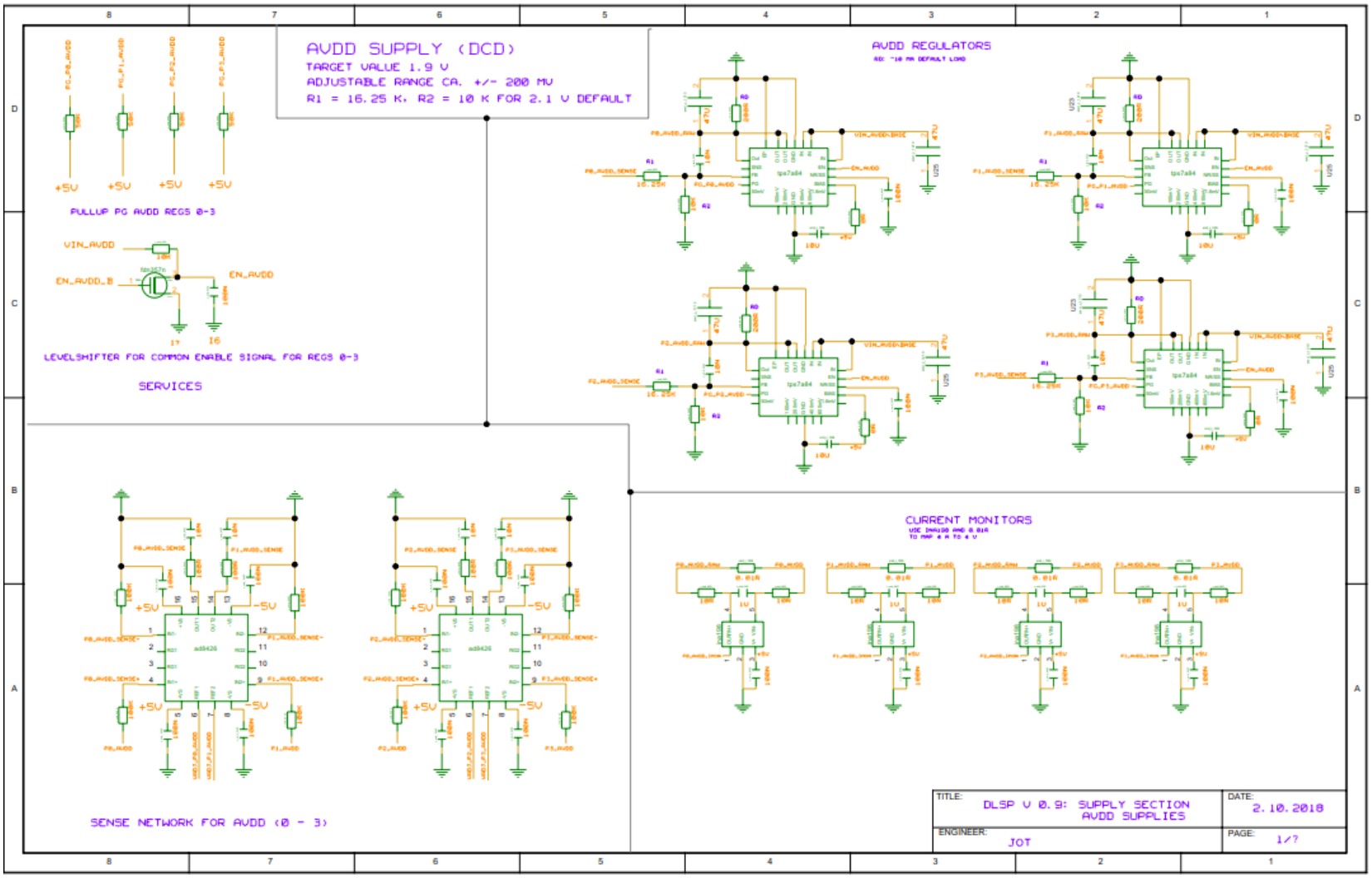
DLSP development

Voltage	Regulator	# ICs	# ASICs	Case	Area
AVDD	TPS7A85	4	2	3.5 x 3.5 mm^2 VQFN Package	49 mm^2
AMP_LO	LT3091	4	2	3 x 4 mm^2 DFN Package	48 mm^2
VREF_IN[1]	LT3086	1	all	5 x 4 mm^2 DFN Package	20 mm^2
DVDD	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
VDMC_IO	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
VDMC_CORE	TPS7A85	2	4	3.5 x 3.5 mm^2 VQFN Package	24.5 mm^2
Switcher_VDD[2]	TVL705	1	all	0.8 x 0.8 mm^2 DSBGA Package	0.64 mm^2
Sum		16			192 mm^2

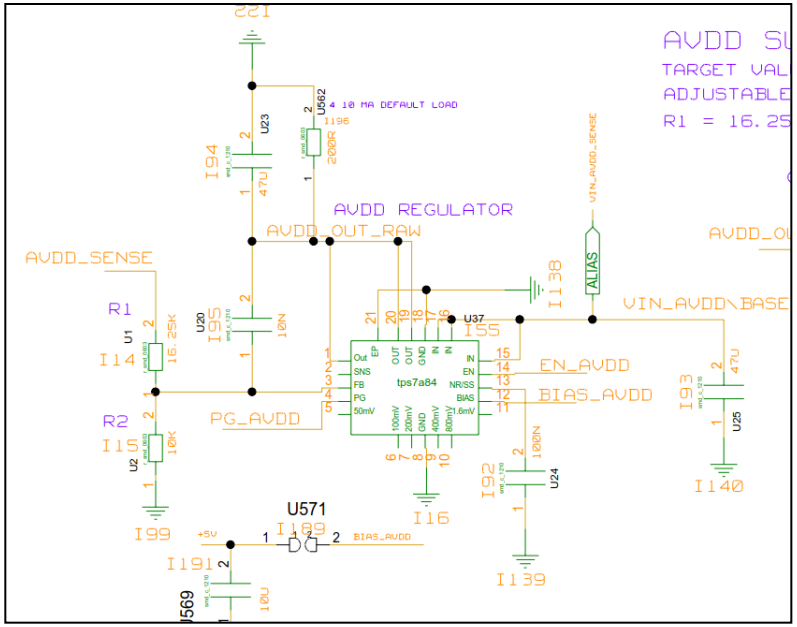
General considerations:

- Multiple number of regulators
- Limited space
- Smaller components
- Simpler circuits
- No frills
- Compromize wrt. test /debug functionality and spatial constraints

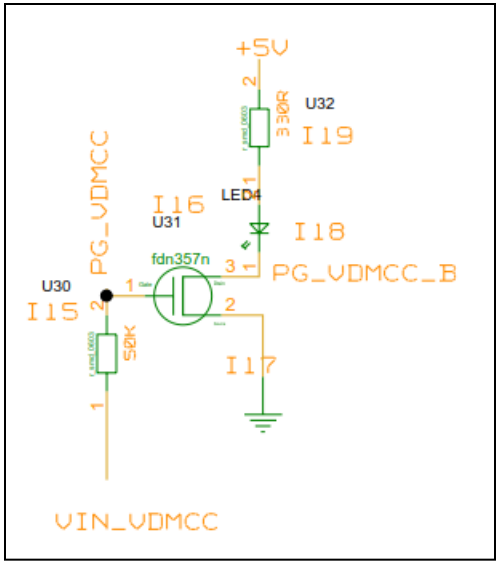
DLSP circuit

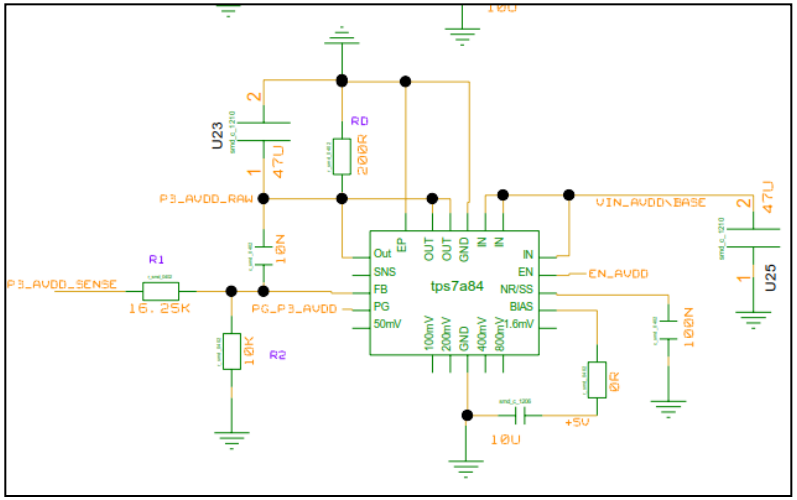


DLSP circuit

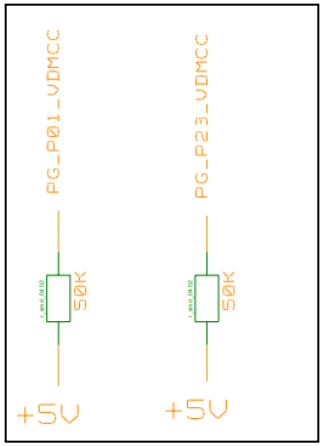


PSP

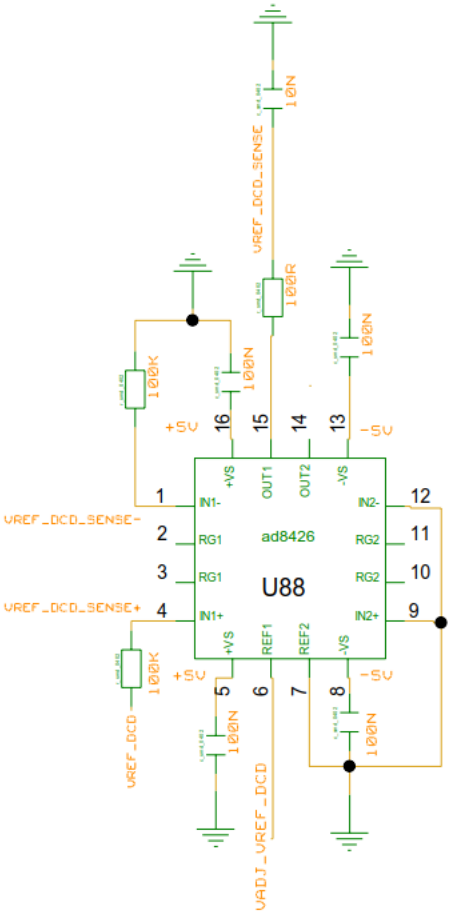


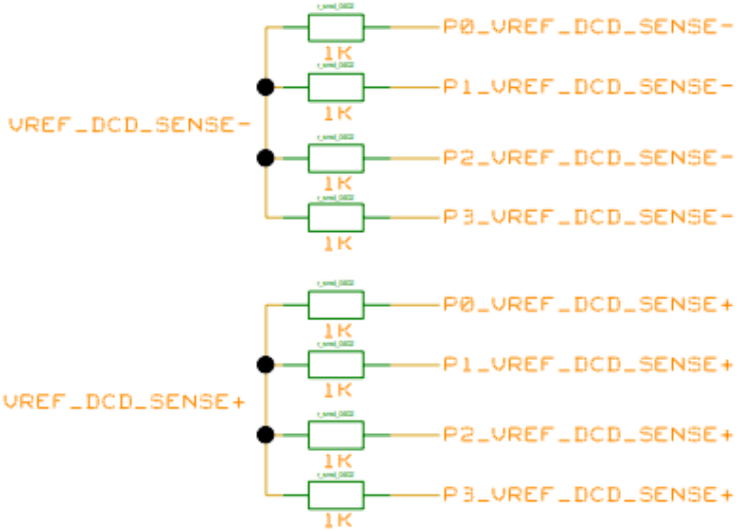


DLSP



DLSP circuit





General considerations:

- Shared regulators require shared sense lines
- Resistive connections to hi-Z input node of sense amplifier
- Small error current to "default" potential

DLSP Status

Status:

- Layout almost finished (few more days required)
- Preparatory discussions w/ vendors
- Fabrication + Population (~ 2 m)
- All circuits prototyped on breadboard and PSP
- **PSP test w/ detector still to be done**

Critical aspects:

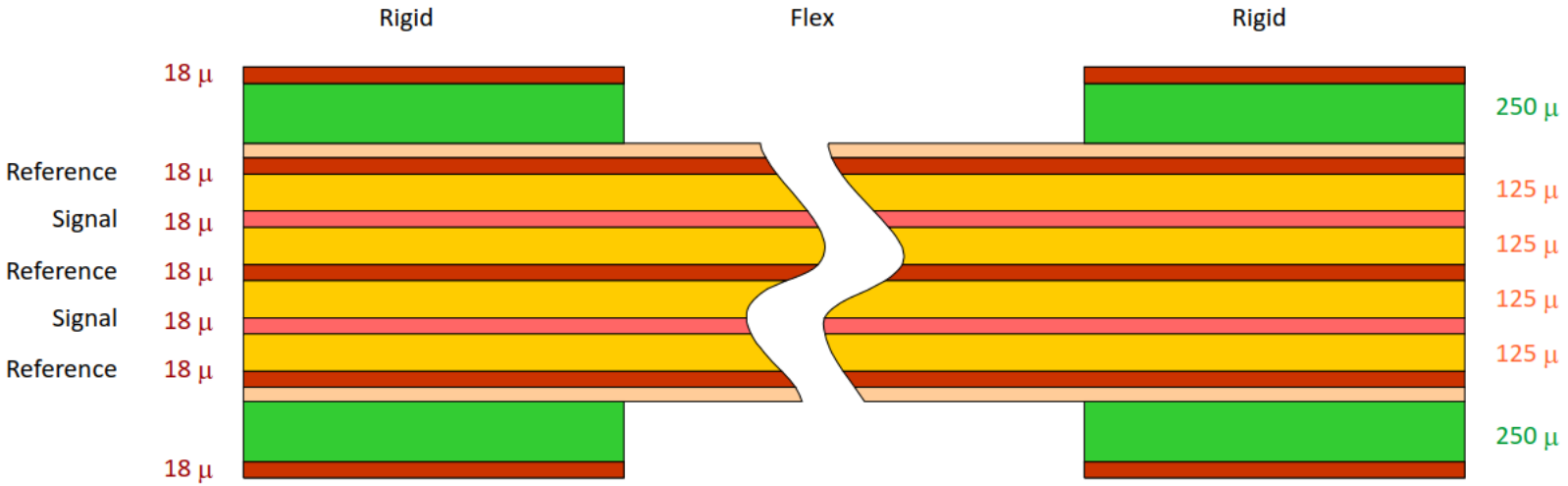
- Vias only to Flex layer surface
- Combination of densely populated rigid parts and flex layers
- Thermal management
- Interplay between ASM and LDOS / SenseAmps

Minor issues:

- Housekeeping / resolution of cuurent measurements

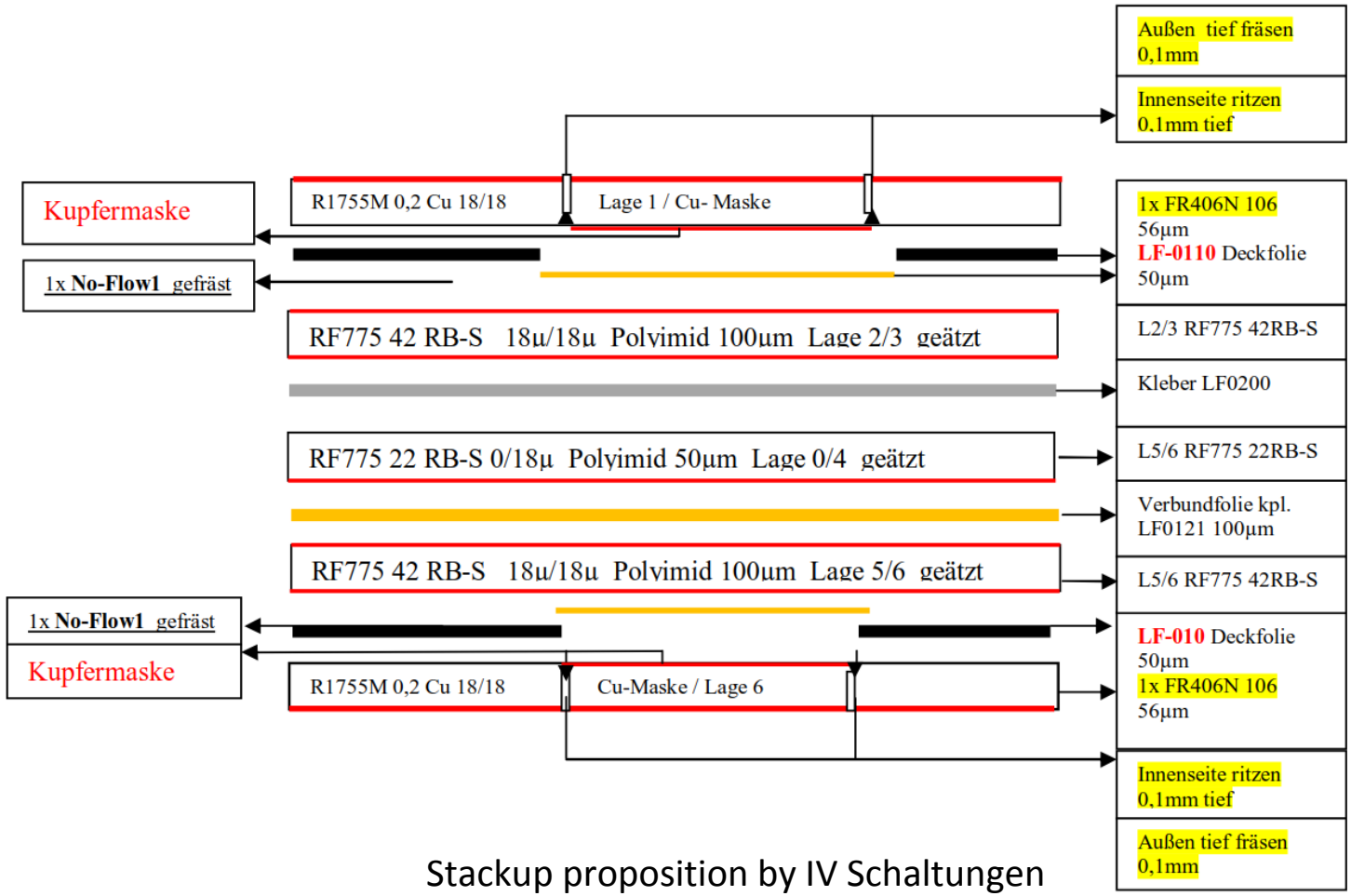
Still some work to be done…

VIC development



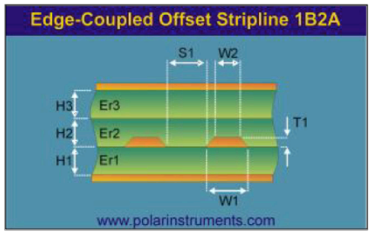
Wanted stackup

VIC development



Stackup proposition by IV Schaltungen

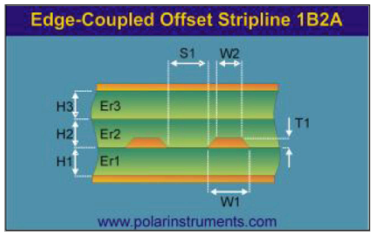
VIC development



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	100,0000	+/-	0,0000	100,0000	100,0000
Substrate 1 Dielectric	Er1	3,2000	+/-	0,0000	3,2000	3,2000
Substrate 2 Height	H2	50,0000	+/-	0,0000	50,0000	50,0000
Substrate 2 Dielectric	Er2	3,7000	+/-	0,0000	3,7000	3,7000
Substrate 3 Height	H3	50,0000	+/-	0,0000	50,0000	50,0000
Substrate 3 Dielectric	Er3	3,2000	+/-	0,0000	3,2000	3,2000
Lower Trace Width	W1	80,0000	+/-	0,0000	80,0000	80,0000
Upper Trace Width	W2	80,0000	+/-	0,0000	80,0000	80,0000
Trace Separation	S1	230,0000	+/-	0,0000	230,0000	230,0000
Trace Thickness	T1	18,0000	+/-	0,0000	18,0000	18,0000

Differential Impedance	Zdiff	99,82	------	99,82	99,82
Delay (Odd Mode) (ps/m)	D	6149,890	------	6149,890	6149,890
Odd Mode Impedance	Zodd	49,91	------	49,91	49,91
Even Mode Impedance	Zeven	51,12	------	51,12	51,12
Common Mode Impedance	Zcommon	25,56	------	25,56	25,56

"Standard" routing



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	100,0000	+/-	0,0000	100,0000	100,0000
Substrate 1 Dielectric	Er1	3,2000	+/-	0,0000	3,2000	3,2000
Substrate 2 Height	H2	50,0000	+/-	0,0000	50,0000	50,0000
Substrate 2 Dielectric	Er2	3,7000	+/-	0,0000	3,7000	3,7000
Substrate 3 Height	H3	50,0000	+/-	0,0000	50,0000	50,0000
Substrate 3 Dielectric	Er3	3,2000	+/-	0,0000	3,2000	3,2000
Lower Trace Width	W1	65,0000	+/-	0,0000	65,0000	65,0000
Upper Trace Width	W2	65,0000	+/-	0,0000	65,0000	65,0000
Trace Separation	S1	110,0000	+/-	0,0000	110,0000	110,0000
Trace Thickness	T1	18,0000	+/-	0,0000	18,0000	18,0000

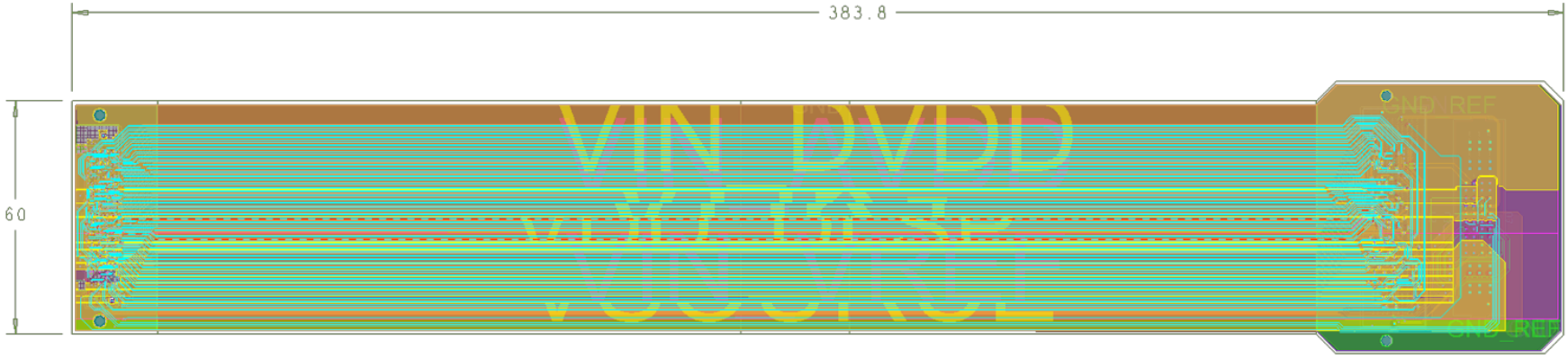
Differential Impedance	Zdiff	100,45	------	100,45	100,45
Delay (Odd Mode) (ps/m)	D	6168,226	------	6168,226	6168,226
Odd Mode Impedance	Zodd	50,23	------	50,23	50,23
Even Mode Impedance	Zeven	59,78	------	59,78	59,78
Common Mode Impedance	Zcommon	29,89	------	29,89	29,89

"Neck" mode

VIC development

Status:

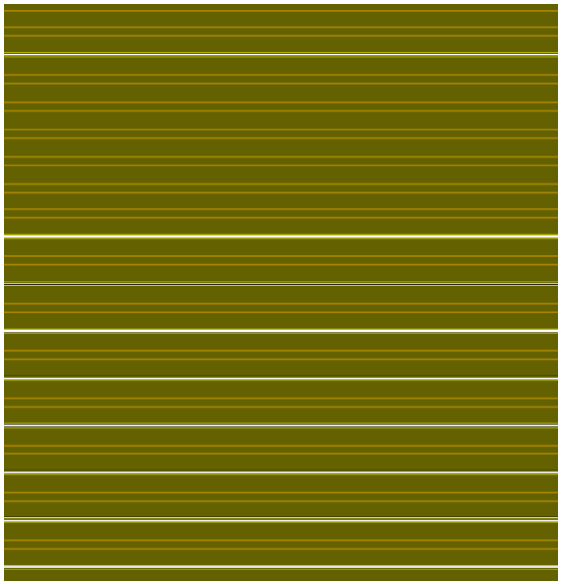
- Schematic completed
- Adaption of "MSM bracket" part of VIC done
- "Reference Ground" issue addressed
- Signal layers routed
- Power layers routed
- Optimized via connections
- Routing optimization: preference for DHP TX lines

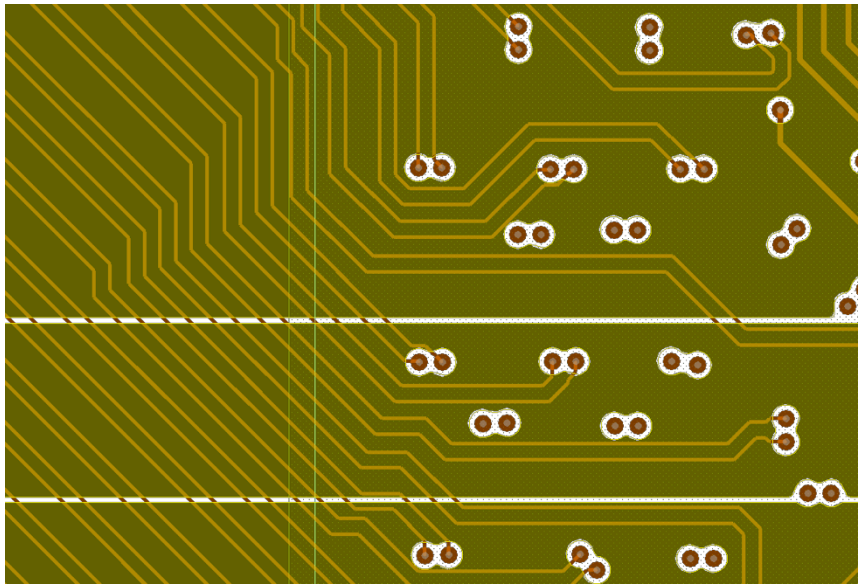


VIC development

Routing:

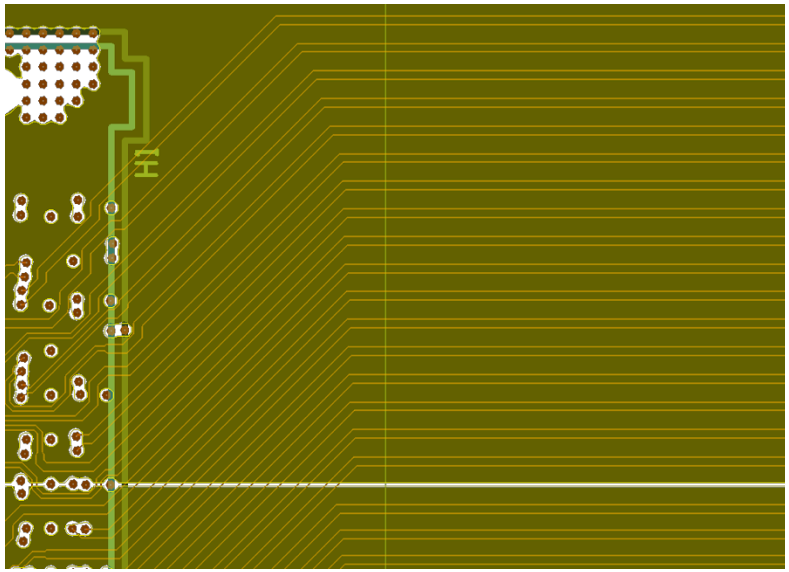
- All differential signals on layers 3 and 5
- 4 vias per differential pair
- Separation of DP ~ 0.6 mm
- Less separation distance in neck region
- Limit neck lenght as much as possible (yield issue)
- Distance from edges of reference planes 0.6 mm





- DPs crossing reference plane edges is unavoidable
- includes DHP TX lines
- Should these be given more priority?

VIC development

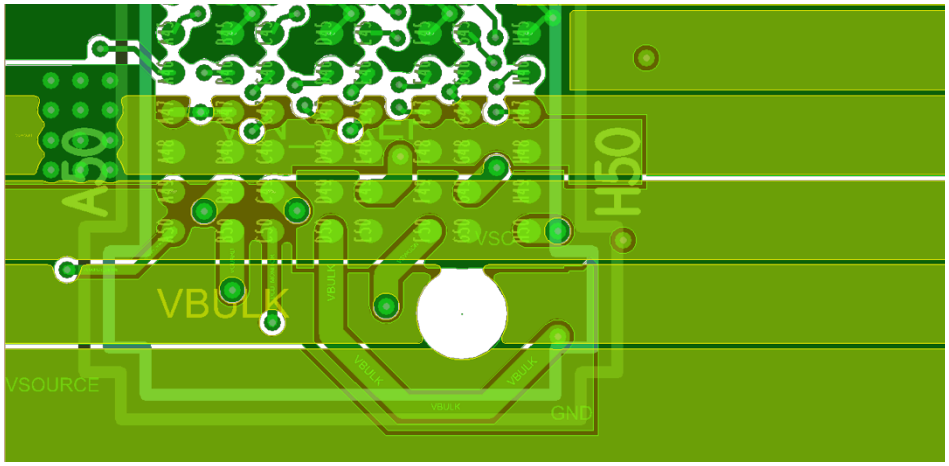


Power connection:

- Limited space for via placement for power connection
- Current rating for vias needs to be discussed with vendor
- Placement of via arrays in fanout mainly in vicinity of DLSP bracket

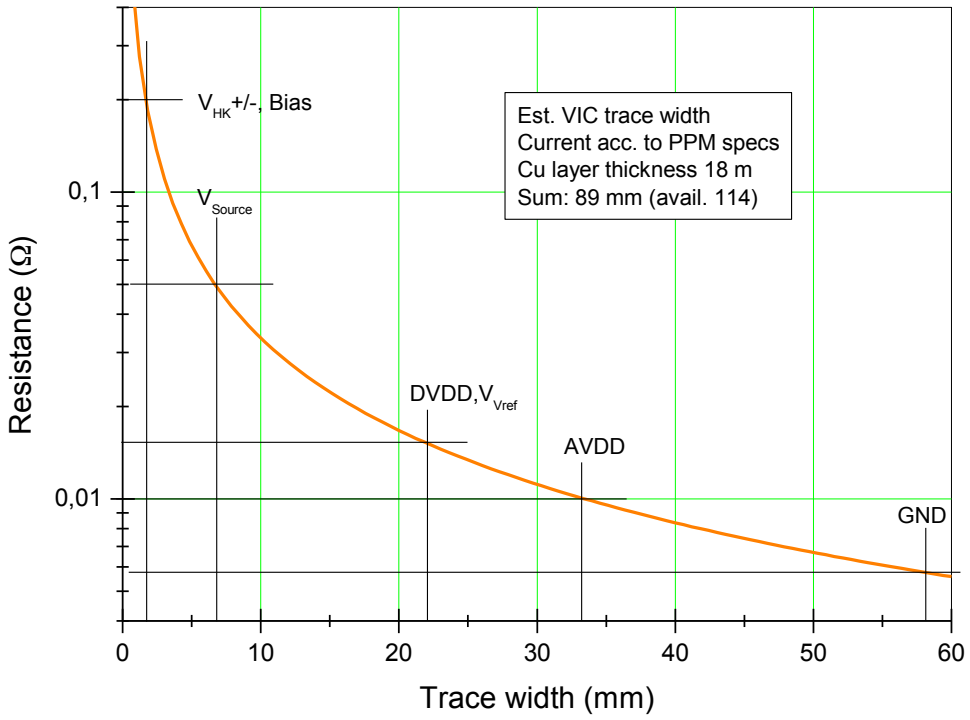
Fanout:

- Less separation distance in fanout region of mainly the DLSP bracket
- Using "neck mode" may introduce yield problems
- What has priority?
- Redistribution is considered



VIC development

Voltage	ΔU [V]	I_{max}[A]	R ≤ [mΩ]	w ≥ [mm]
GND (ret)	0.175	30	5.8	57
Vin_AVDD	0.1	10	10	33
Vin_DVDD	0.1	6.5	15	22
Vin_Vref	0.1	6	15	22
VDD_DLSP	0.1	2	50	7
VHK+	0.1	0.5	200	2
VHK-	0.1	0.5	200	2
VSource	0.1	2	50	7
VBias (10x)	0.1	10^{-3}	200	1
Vin_VSWSUB	0.1	0.1	200	1



Sufficient area on VIC available to keep requirement

VIC development

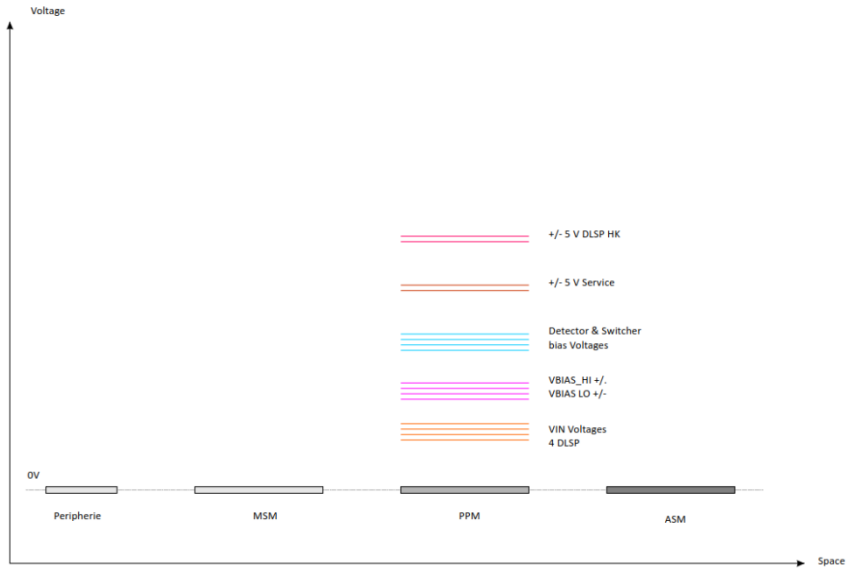
Grounding:

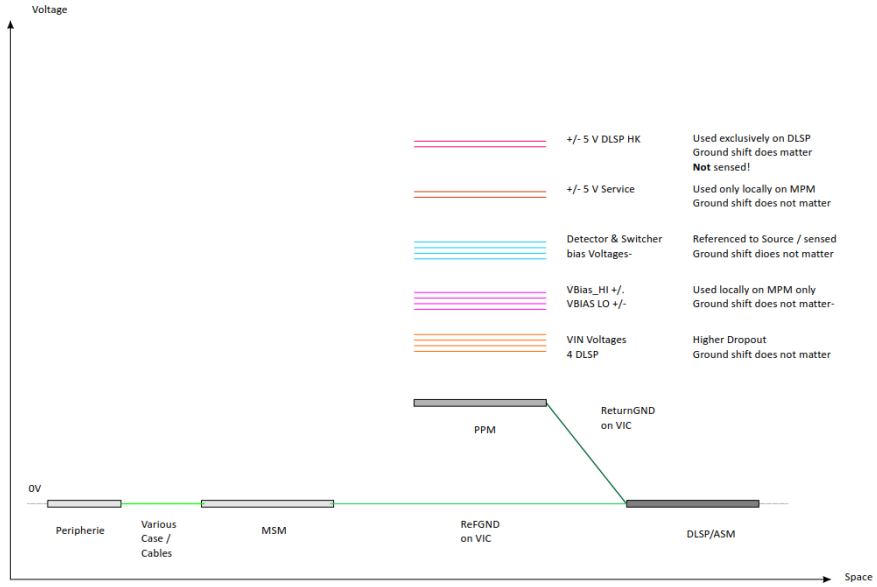
•Significant ground shift due to return currents

•18 µm copper cladding

•Requires separation between return ground (relevant for MPM) and and reference ground (MSM)

- Add. overvoltage for LDO input voltages from regulators required
- Sense lines for 5V HK voltages required





VIC development

Timeline:

- 2-3 days upon clarification of open questions
- Quote available
- ~ 5 k for lot of 10 specimen
- Layer stackup agreed upon with manufacturer (IV Schaltungen)
- Impedance testing to be requested
- 22 days of delivery time
- But: Sometimes quality issues with IV in the past

Anfragenummer: email **Bearbeiter:** R. Lehmann
Anfrage vom: 07.03.2019
Kontakt: Herr Koffmane

LP-Nummer: **VIC_20190304**
Artikelnr.Kunde:
Artikelnr. IV:
Ausführung: STARRFLEX (Flex-Rigid)
Materialstärke: 1,50 mm **Kupfer IL:** 18 µm **AL:** 30 µm
Lagenzahl: 8
Einzelendmaß: 70,00 x 383,80
Nutzenendmaß: 90,00 x 405,00 1-fach
Zulässige Schlechtteile im Nutzen: 0
Ausführung: Lötstopplack zweiseitig
bleifrei Fräsen
Chem. Nickel/Gold
Bleifrei
Elektr. Test

IPC-Klasse II

Lieferzeit 22 AT
Zahlung 30 Tage rein netto
Versand ab Werk
Lieferbedingung +/-10 % oder 1 Stück, wenn nicht auf der Bestellung vermerkt

PREISKALKULATION

Rüstkosten je Los: €

Preisstaffelung Preis je Einzel-LP:

max. Abrufe	Menge	Einzelteilpreis €
1	10	394,78

zuzüglich Expressaufschlag::

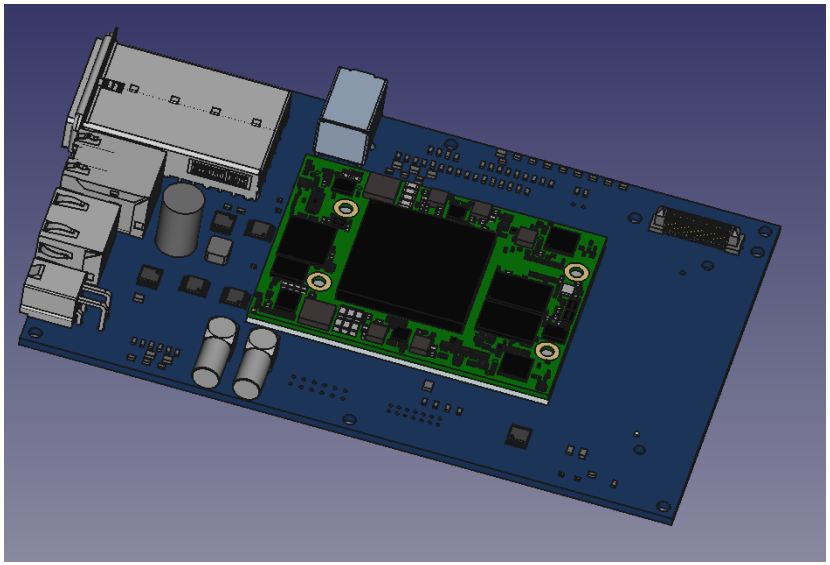
Einmalkosten	€
Nebenkosten	1.100,00

Angebotsgültigkeit: 8 Wochen
Erstellungsdatum: 07.03.2019

MSM development

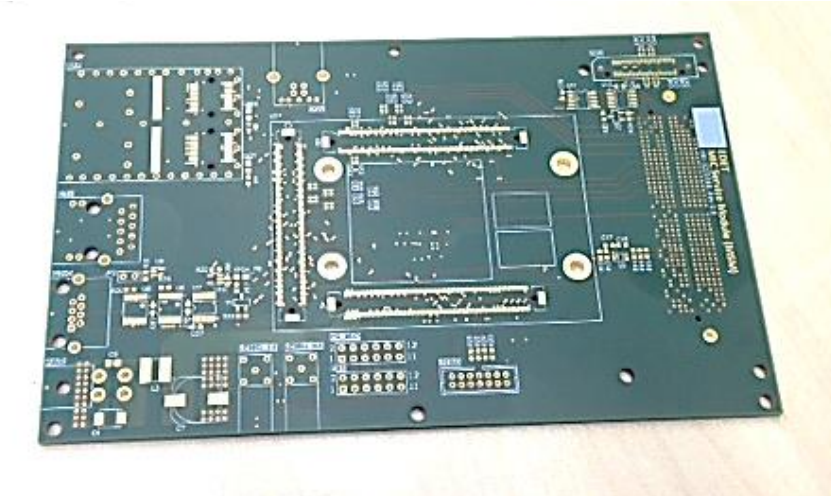
Status:

- PCB fabrication successful
- Practical impedance testing: Nice match
- Waiting for delivery of populated components
- Also possible platform for prototype
- Delivery in week 22



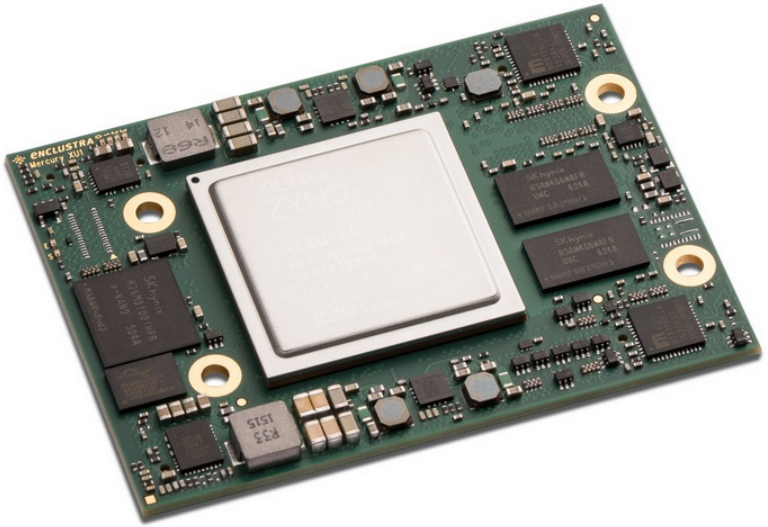
Critical aspects:

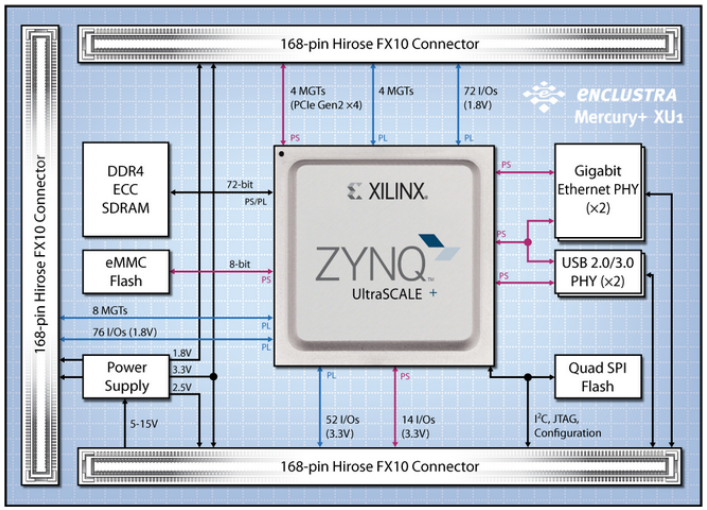
- Functional test for all interfaces
- DHP Aurora link
- Pin assignment for optimum data synchronization / return clock management



MBM "development"

- Commercially avaliable Mercury XU1+ by Enclustra
- Xilinx® Zynq Ultrascale+™ MPSoC
- Up to 8 GB DDR4 ECC SDRAM
- 64 MB QSPI flash
- 16 GB eMMC flash
- PCIe® Gen2 ×4 endpoint
- 16 × 6/8/12.5 Gbit/sec MGT
- Variety of interfaces
- Up to 747,000 LUT4-eq
- 294 user I/Os
- 5 to 15 V single supply
- Small form factor (74 × 54 mm)





Status:

- Sufficient stock
- Few casualties
- First batch had quality issues (were replaced by enclustra)
- Firmware development in progress (see talk by M. Polovykh)

MPM development

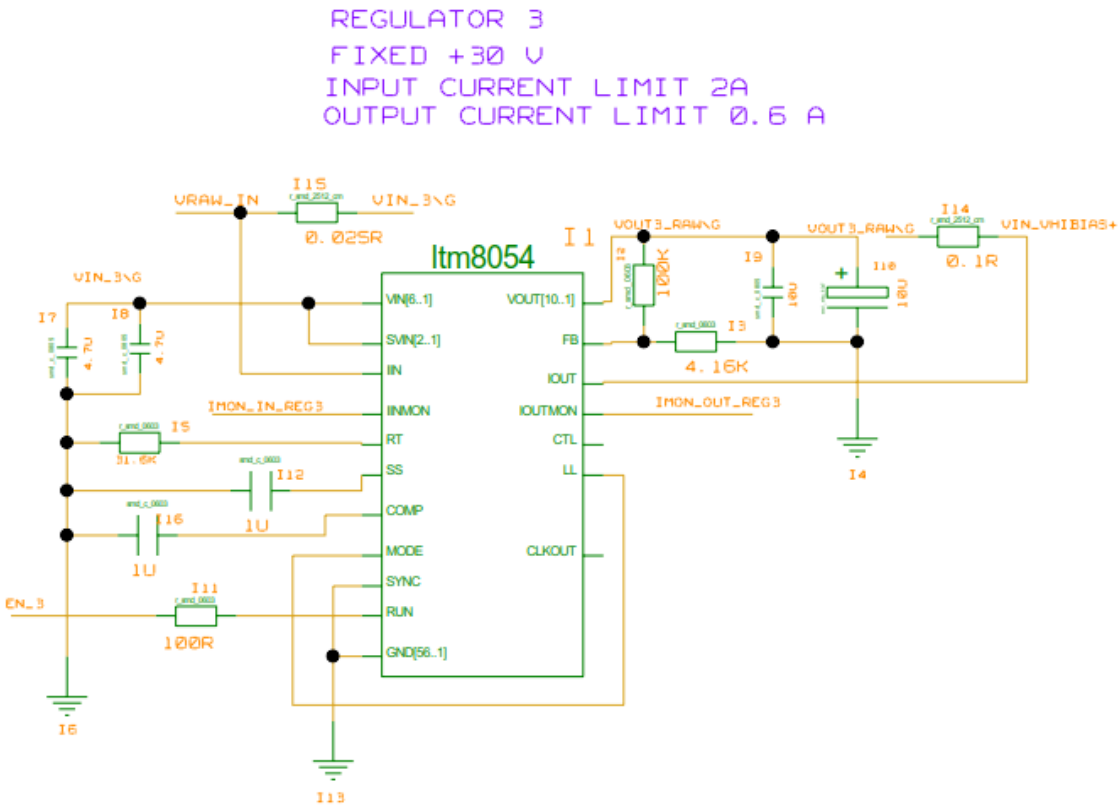
Key aspects:

- MPM not mandatory for large module (i.e. Quadrant) operation
- Can be substituted by Lab supplies during transition period
- PPM prototype has been designed to cope w/ requirement of large modules
- PPM is much closer to MPM than PSP to DLSP
- Re-arrangement of components

MPM development

Key aspects:

- Fixed regulators
- Using feedback inputs for adjustment
- No (!) sensing, keeps VIC simpler
- Provide for sufficient overvoltage



MPM development

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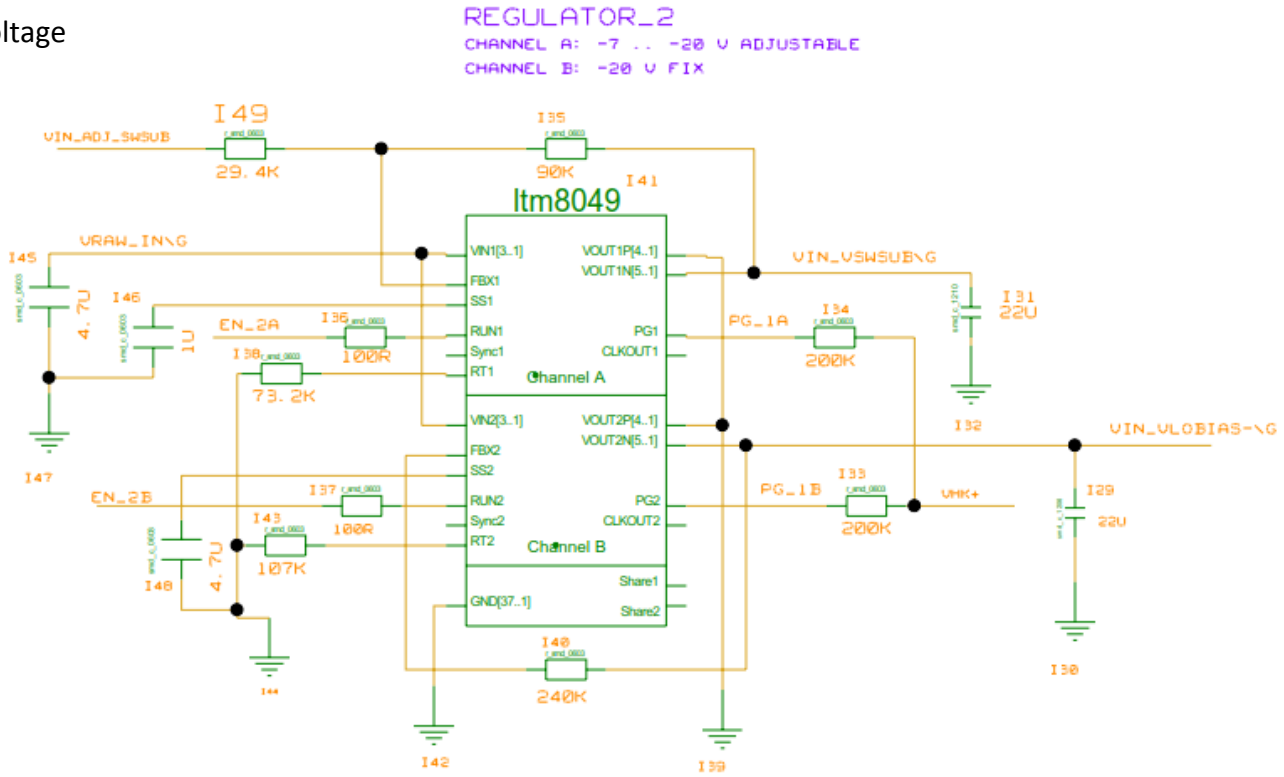


Steps towards final MPM

To dos:

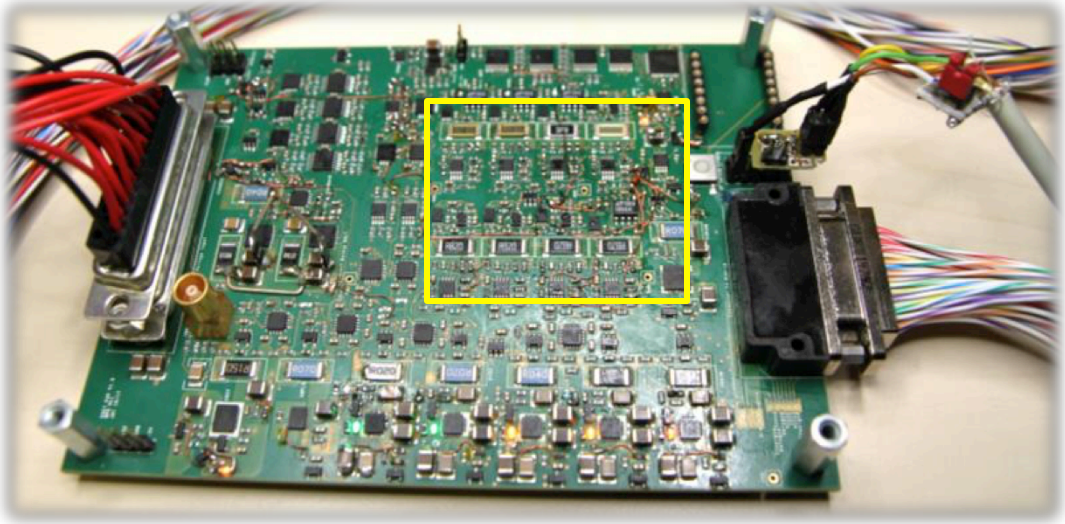
- Cleanup of current MPM
- **Test w/ PSP and detector prototype required**
- Detector power supplies from PSP need to be transferred to MPM
- Implementation of "decoupled" HK deatures

Decisions to be made:

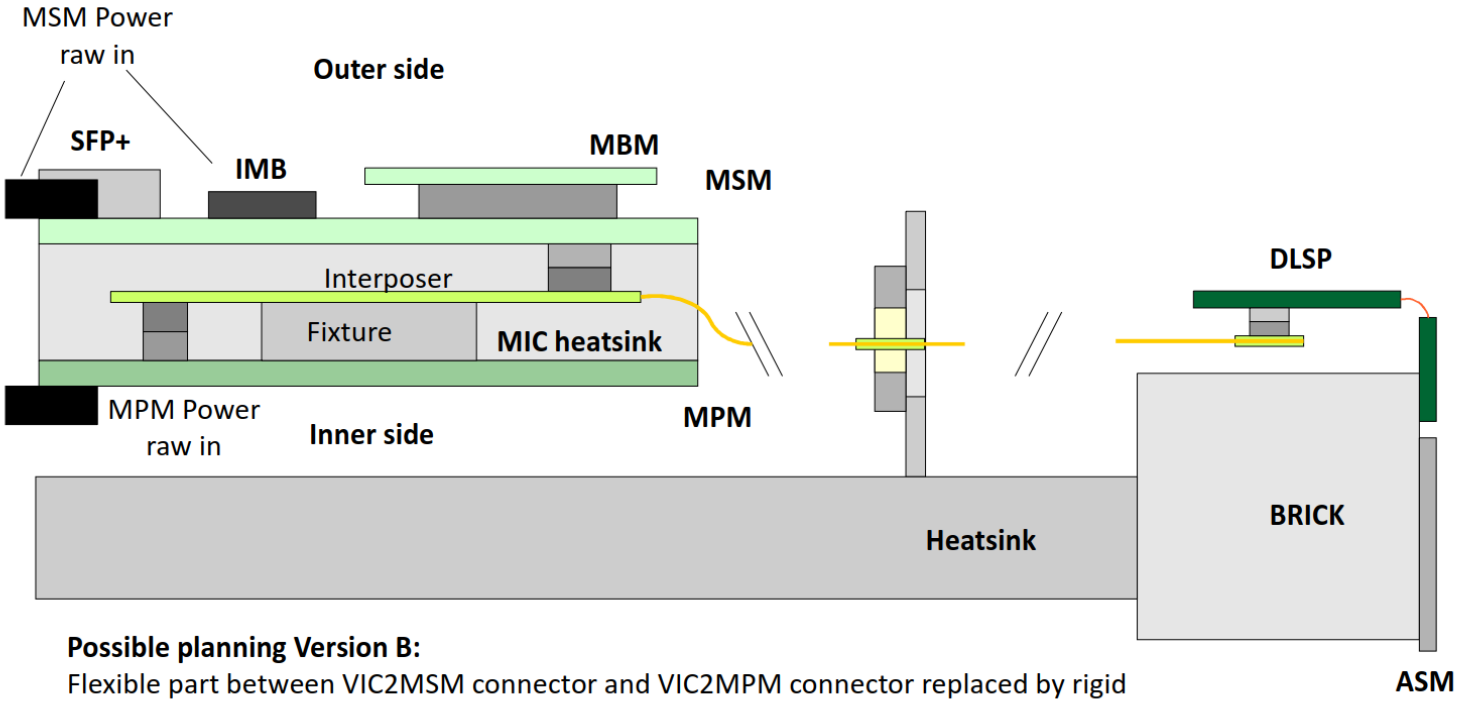
- RF cages required?
- Design of source supply w/ load sharing?

In addition:

- Breakout boards for MSM and VIC
- DLSP bracket and MIC bracket
- Design to be atrten upon finalization of VIC / DLSP



MIC stackup development

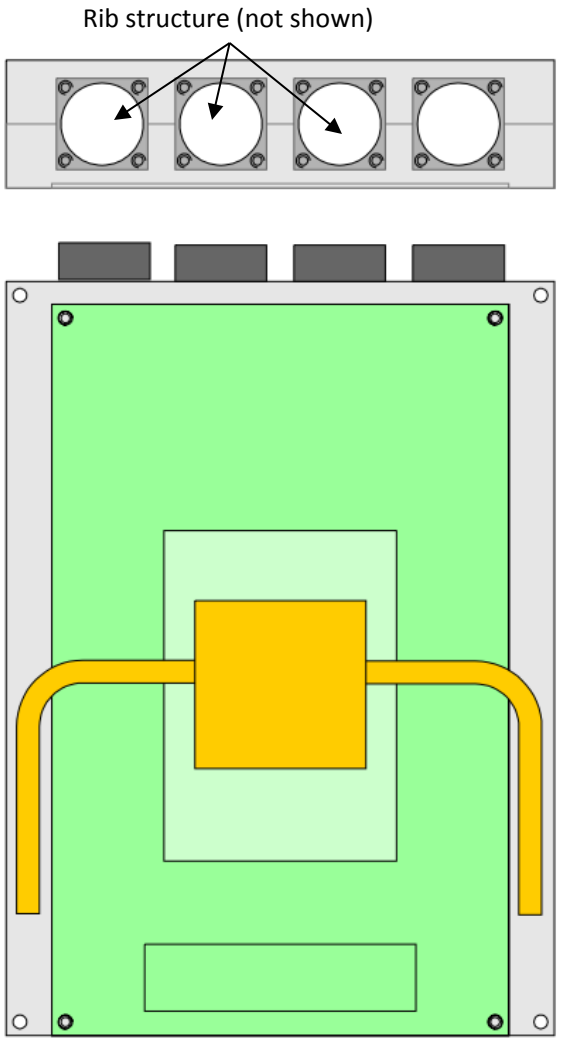


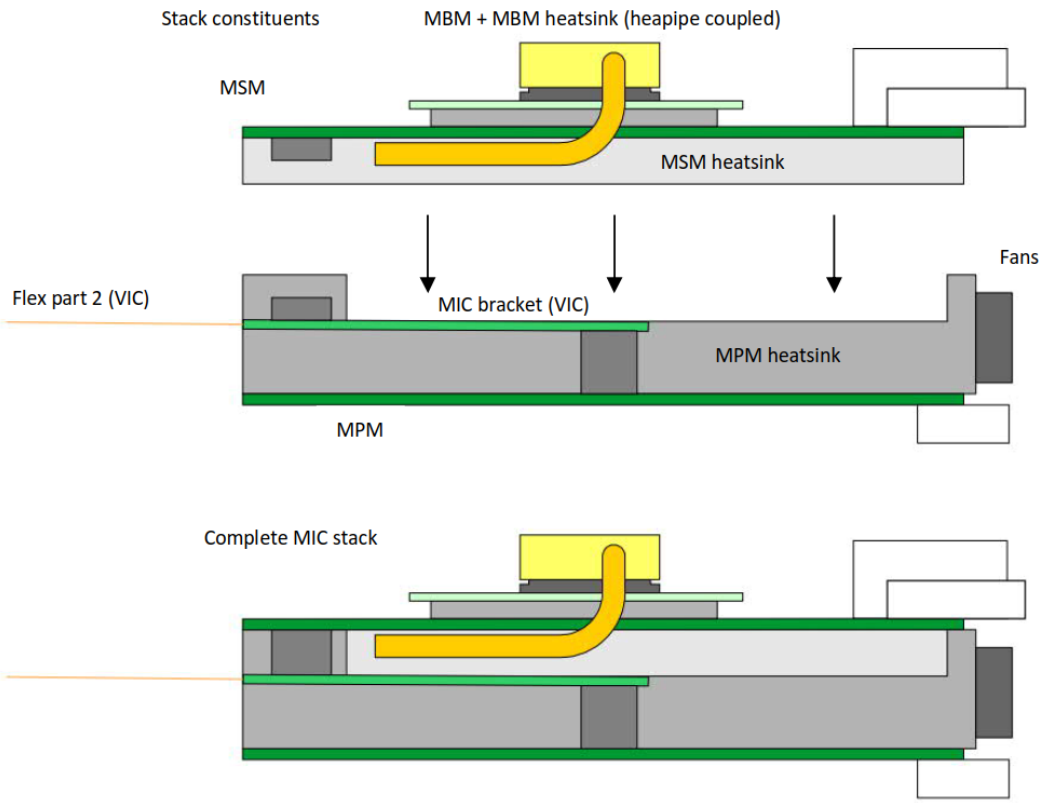
Possible planning Version B:
Flexible part between VIC2MSM connector and VIC2MPM connector replaced by rigid "Interposer" PCB

Pro:
- Advantages as for V A
- Easy to dismantle if Interposer mounted on Fixture
- More compact and robust

Con:
- 2 different power connectors
- possibly more difficult assembly

MIC stackup development





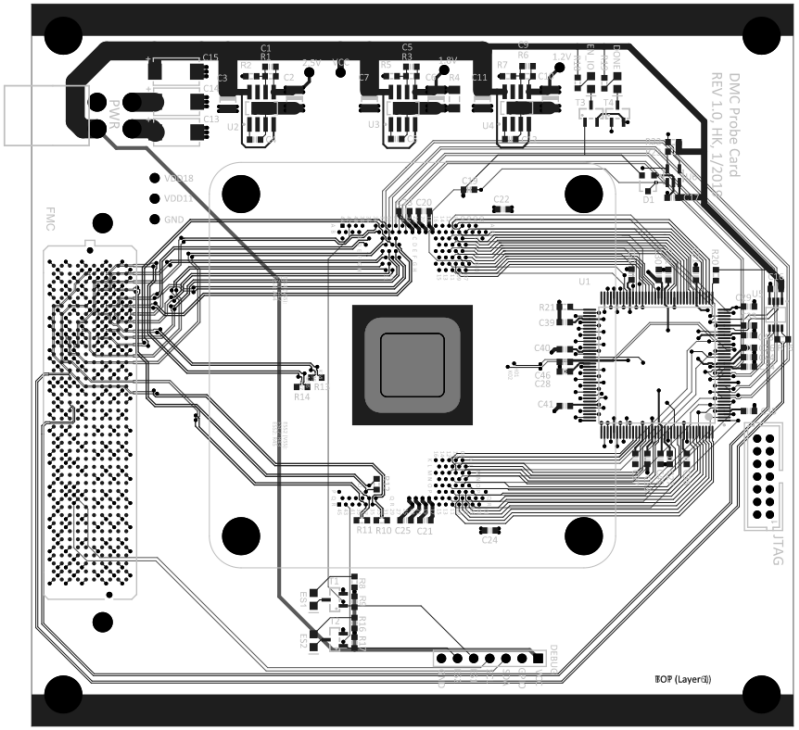
in addition:

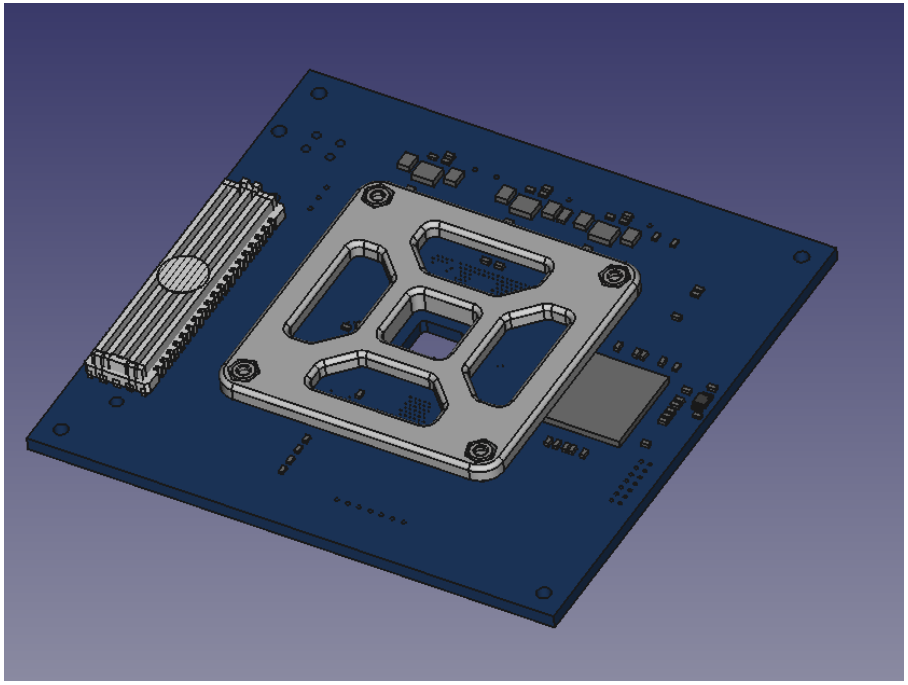
- Developoment of mechanical interface / thermal management adapter for MIC stack (MSM + MBM + MPM)

DMC probecard

Status:

- In production
- Population also arranged
- Simpler "Dummy probecard" for probecard firmware development based on actual is currently being designed

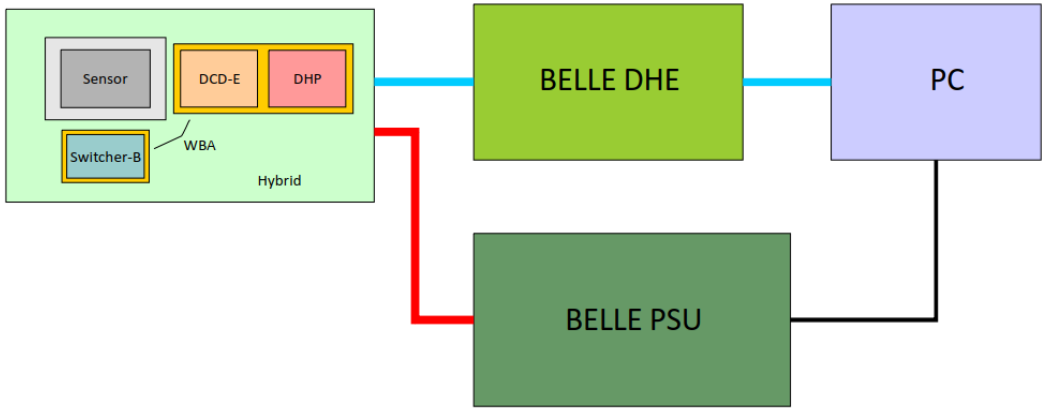


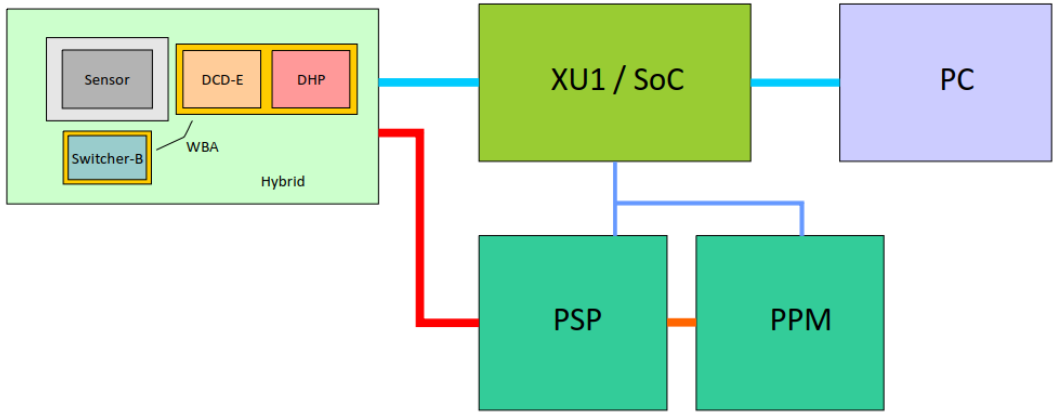


Test configurations

Status:

- DAQ chain: see talk by M. Polovykh
- PS system: See below
- HYbrids available
- Next step: Firmware merger
    - PSP & PPM control
    - DAQ firmware
- Qualification test

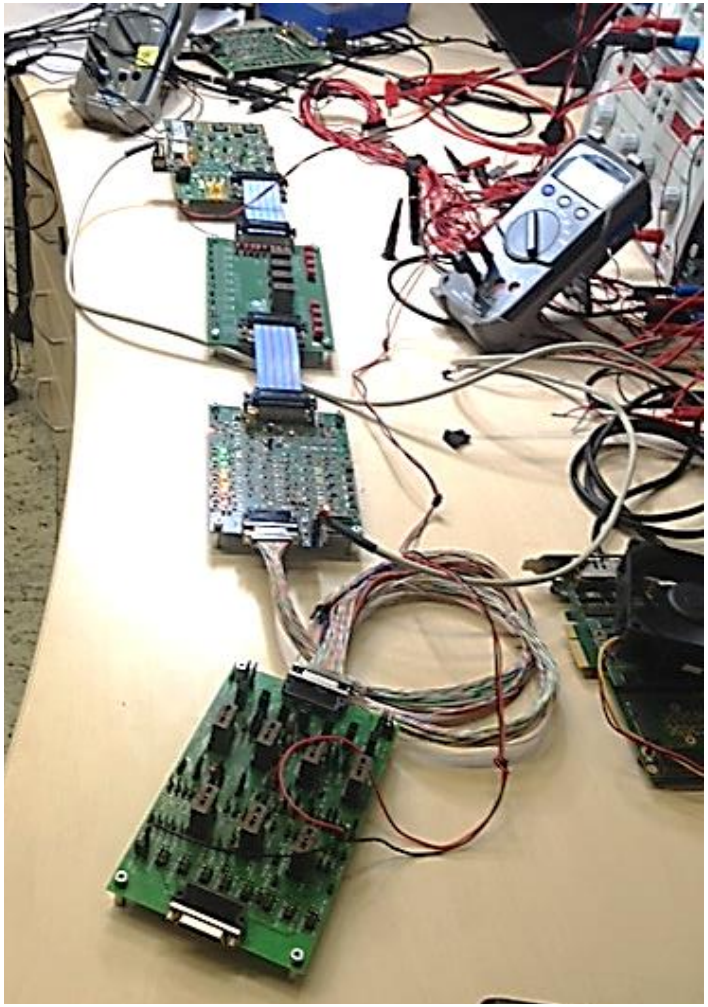


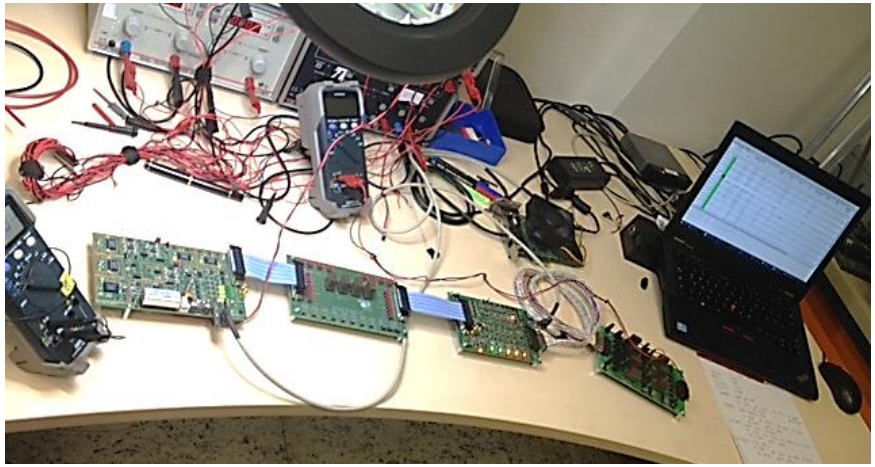


Power supply system development

Status:

- PSP & PPM successfully operated as combo
- Second specimen populated
- Calibration finalized
- Test can start as soon as firmware is ready





Timeline

MSM:

- Available end 3/19

VIC:

- Available end 4/19

DSLP:

- Available end 5/19

MPM:

- Design start after VIC finalization
- 2-3 weeks of layout
- 4 weeks of production
- 4 weeks of population
- Check component availability!
- Available 6/19

In parallel:

- Testing and qualification of delivered components
- Software and firmware development

Important milestone:

- Operation of Hybrid / DUT with PSP / PPM combo

Summary & Outlook

Status:

- Late, but on track
- Most important milestone is prototype
- Components for Quadrant system in production
- No conceptual issues