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An Avalanche Diode Array with Bulk Integrated Quench Resistors for Single Photon Detection

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1 Polysilicon quench resistors a cost driver in a SiPM technology
2. An alternative SiPM array
3. Wafer bonding
4. Discussion
5. Next steps

Polysilicon Quench Resistor – Cost driver and Obstacle

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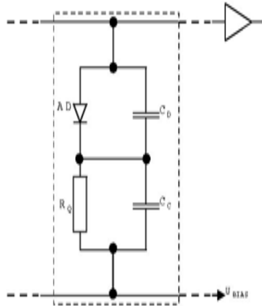


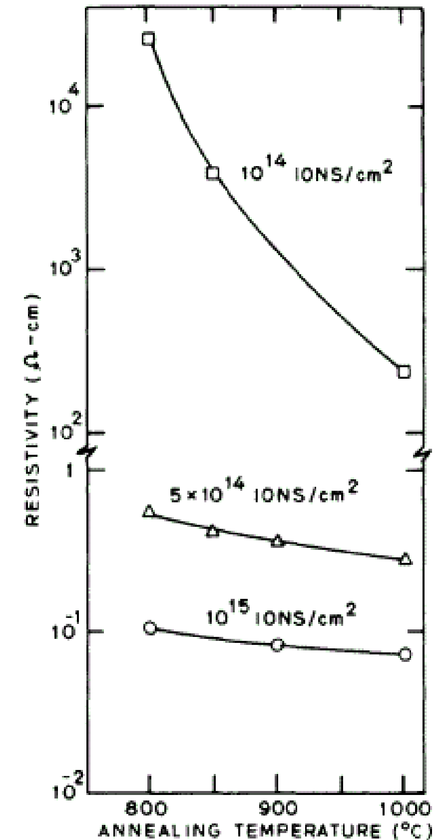
Process complexity

- CVD deposition
- Photolithography, etching
- insulation
- over bias voltage drops across the insulator
- beneath the resistor

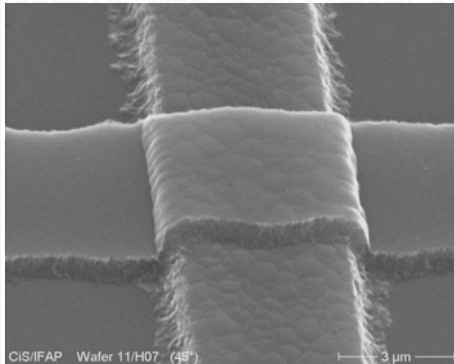
Critical resistance range

influenced by:
grain size, dopant segragation
in grain boundaries, carrier trapping,
barrier height
-> sheet resistance depends on

Deposition conditions, implantation dose, layer thicl
annealing temperature, preconditioning (cleaning st
before deposition)



M. Mohammad et al.
'Dopant segragation in polycrystalline silicon',
J. Appl. Physics, Nov.,1980

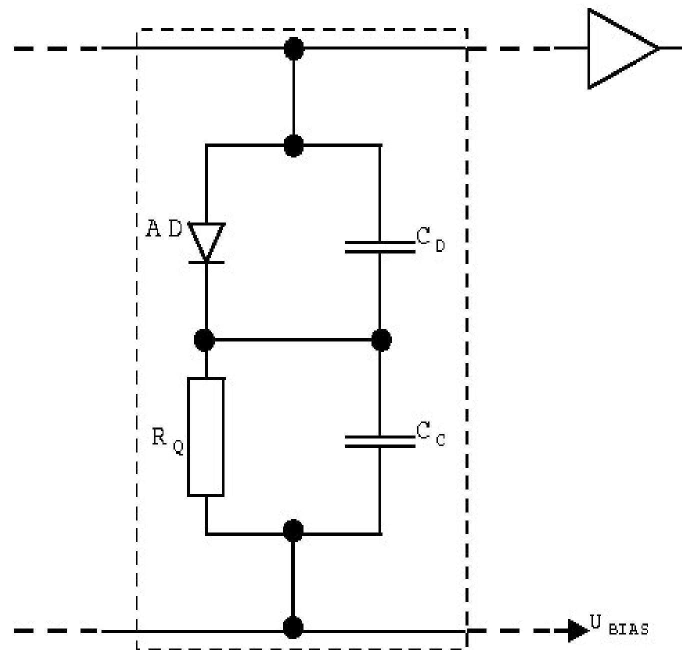


wet etching not trivial at all
not very homogeneous over the wafer

Rather unreliable process step

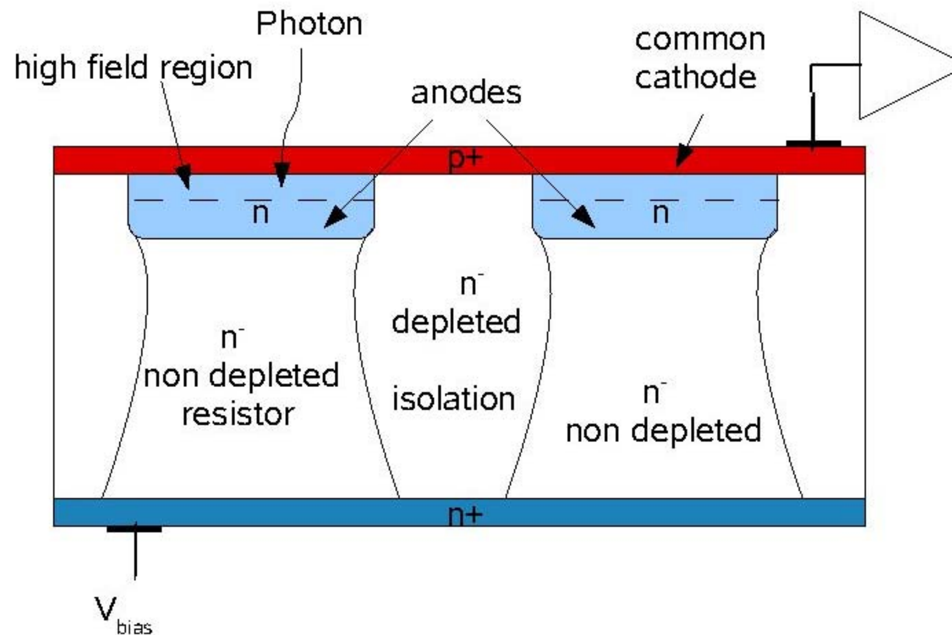
and an obstacle for light

Ingredients of a SiPM cell



Is it possible to simplify the implementation into silicon?

Why not ?

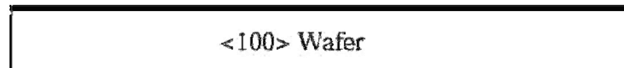


- Front side cathode and backside n+ region are common for the entire array
- Anode region becomes an internal node within silicon
- Bulk region beneath the anode acts as vertical resistor shielded by the anode from depletion
- Gap regions are depleted and isolate the individual resistors

But resistor matching does not work with a wafer of usual thickness ! ☹

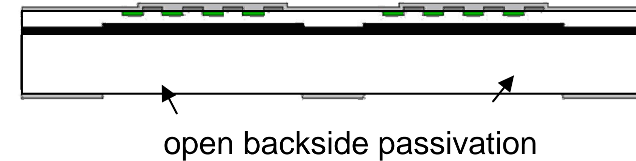
Processing thin detectors (50 μm)

a) oxidation and back side implant of top wafer

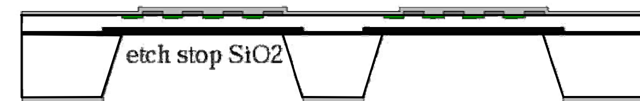


b) wafer bonding and grinding/polishing of top wafer

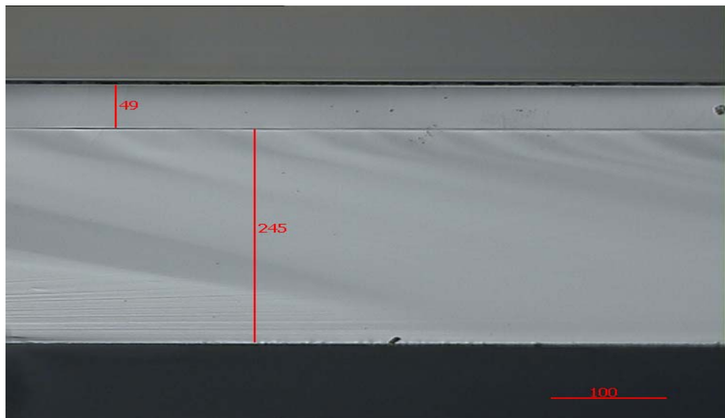
c) process ➔ passivation

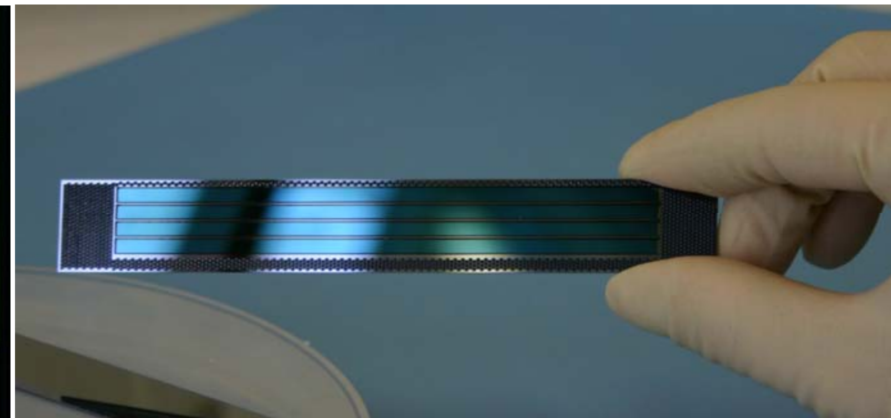


open backside passivation



d) deep etching opens "windows" in handle wafer





Thinning Technology

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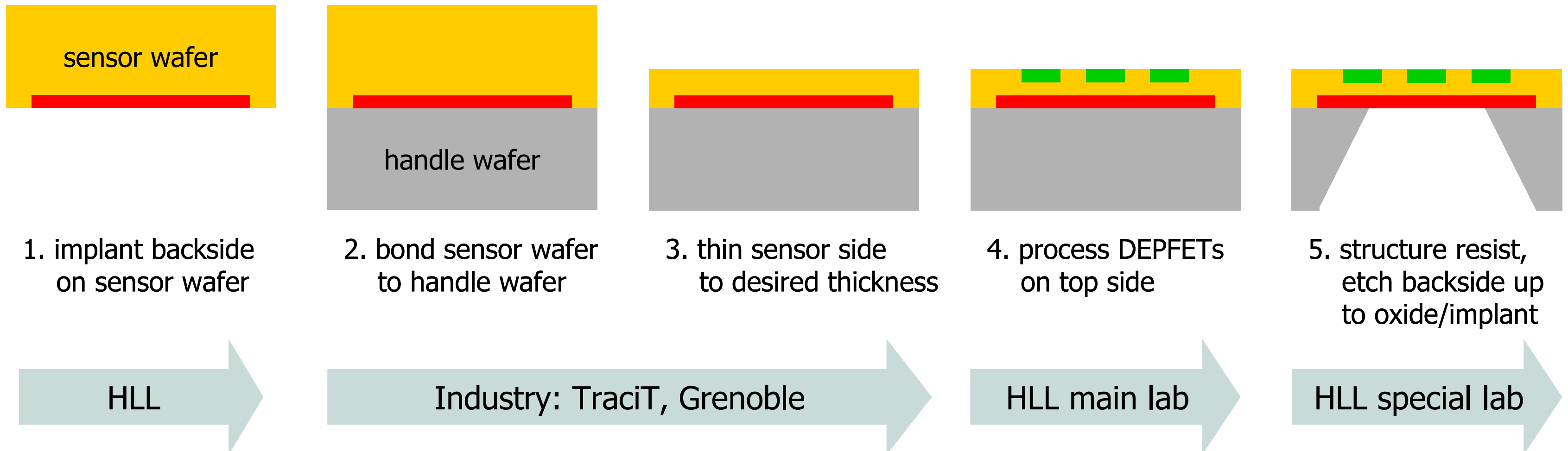
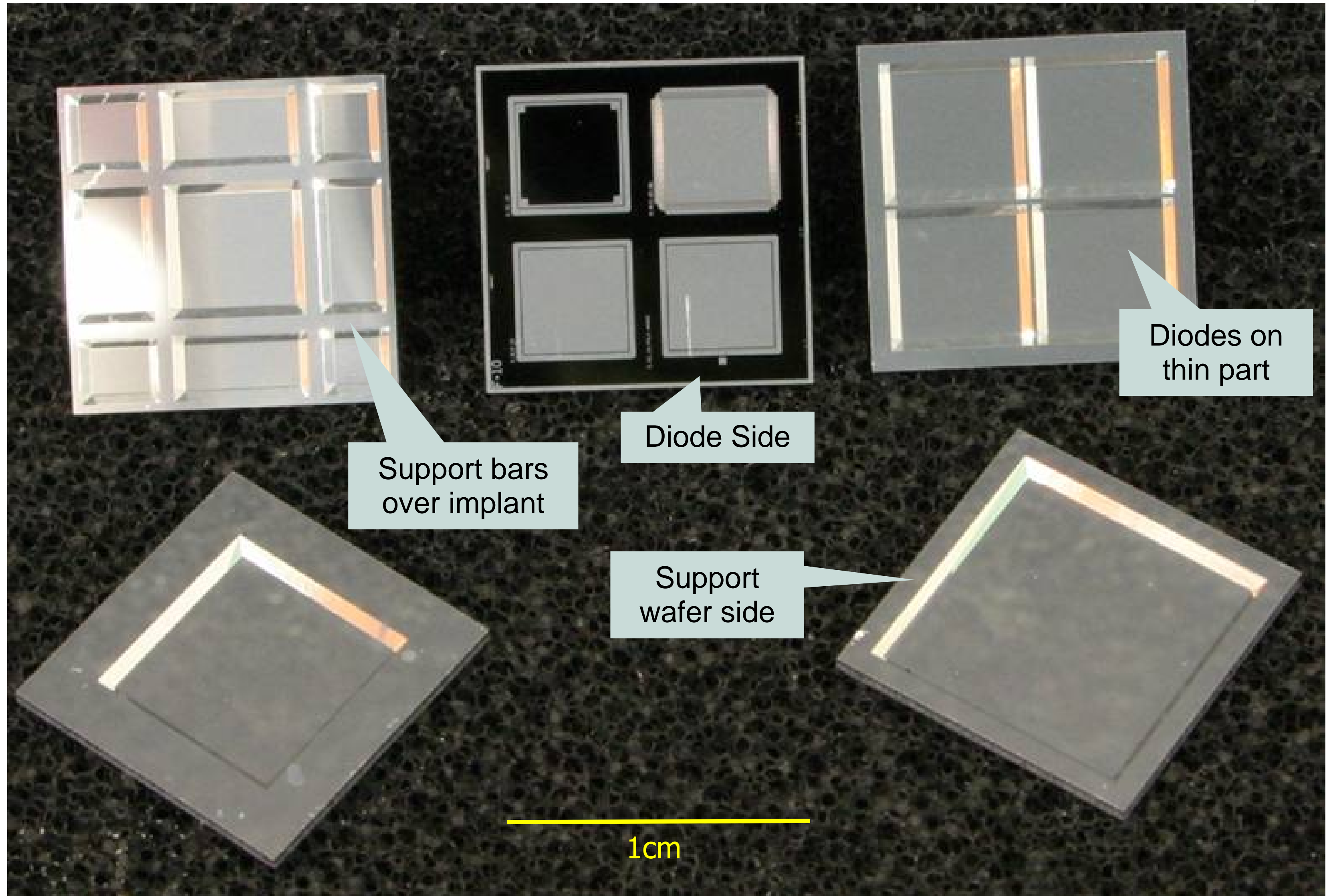


150mm Ø wafers

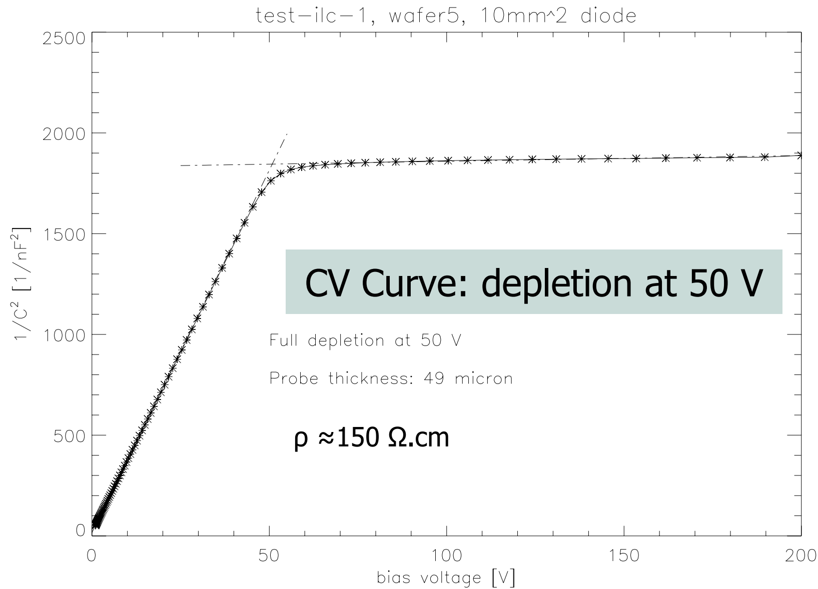
Wafer bonding and thinning in **industry**

Processing in **HLL main lab**

PiN Diodes with Different Support Sides

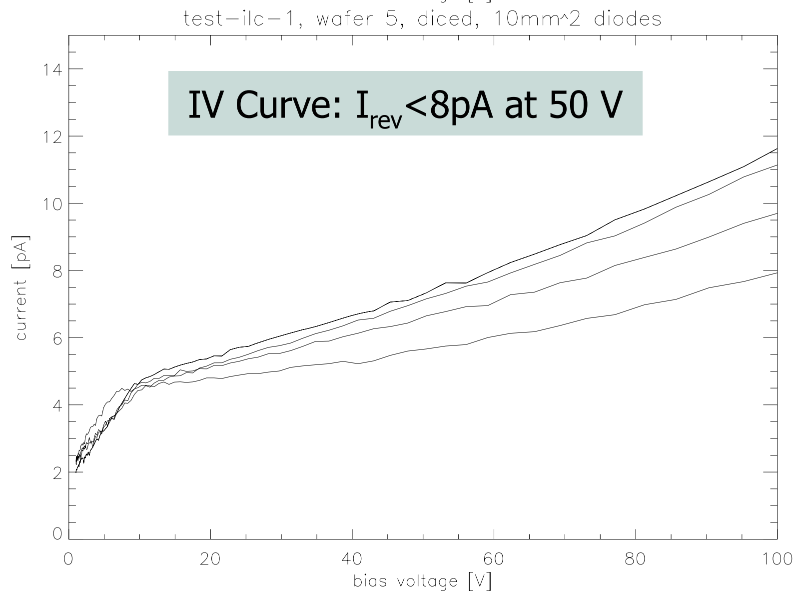


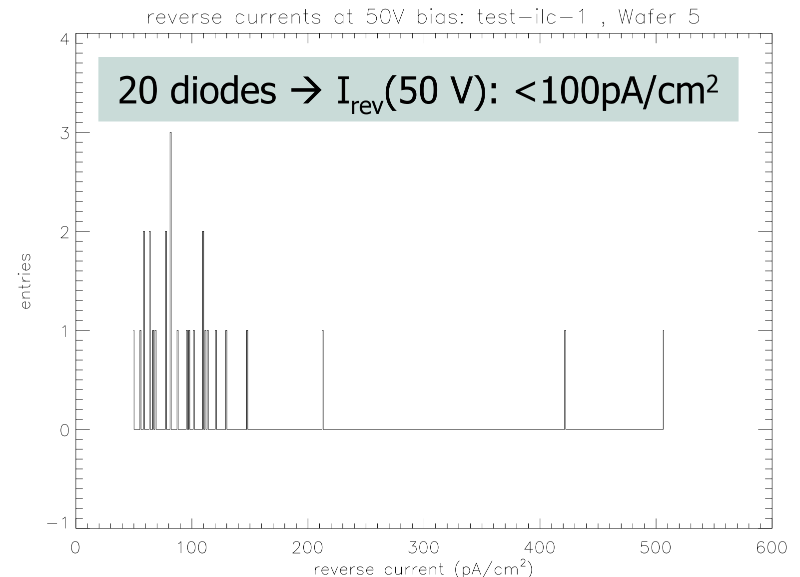
PiN Diodes on thin Silicon



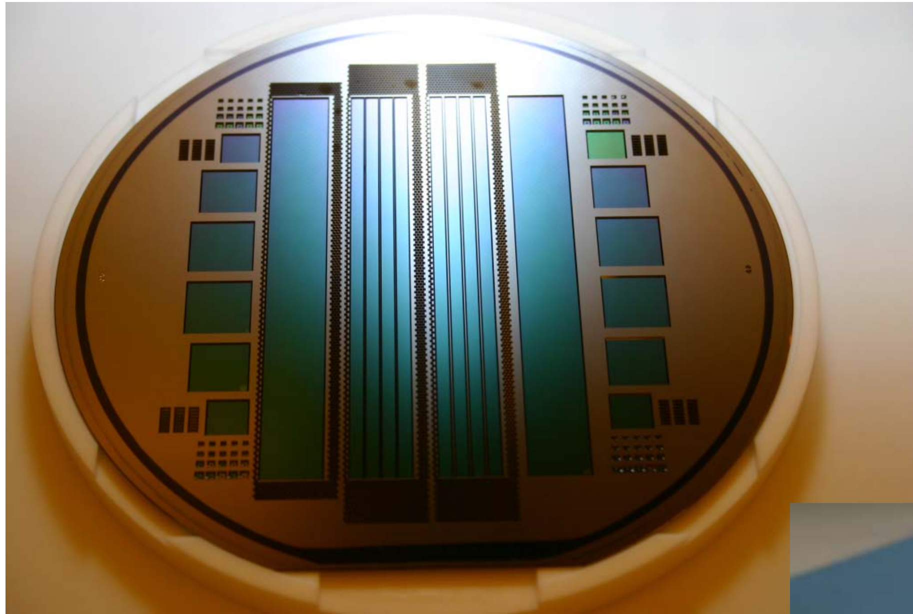
Thin diodes have **excellent** leakage currents.

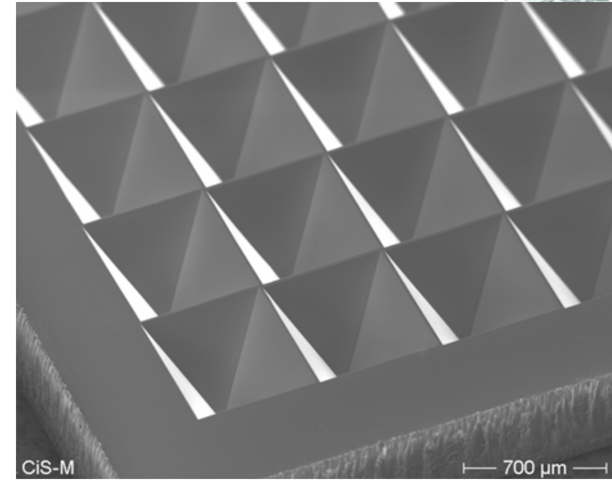
Processing of the SOI wafers and removal of handle wafer **does not degrade devices**!

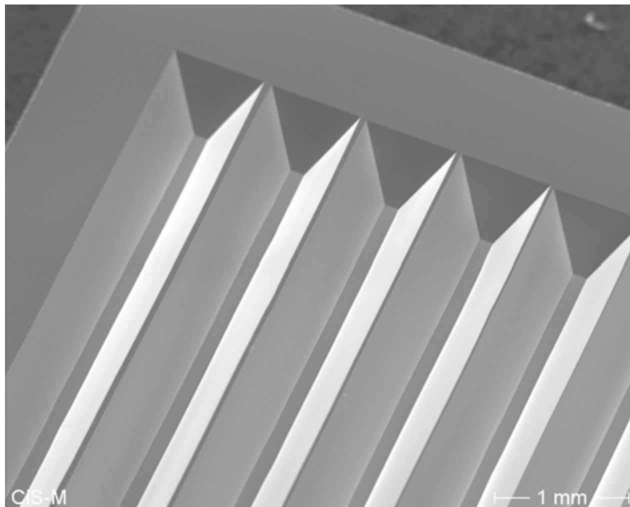


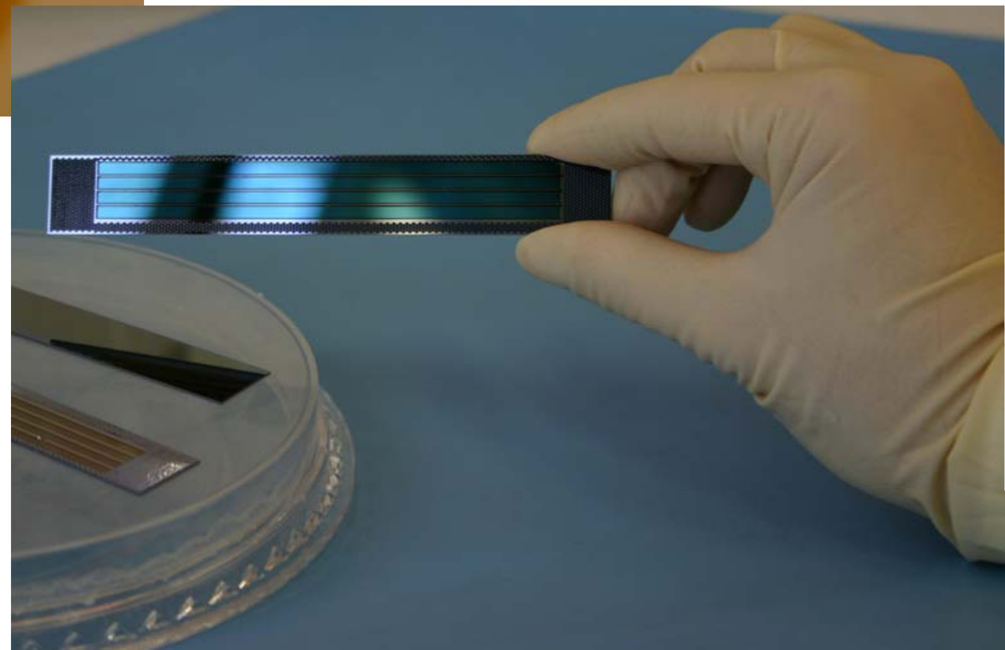


Thinning : mechanical samples









Wafer bonding technique is a well established technology.

SOITEC-TRACIT (France), ICEMOS (Ireland)

It provides the means for the quench resistor adoption !

two parameters: top wafer thickness

doping level

Much experience with processing at HLL

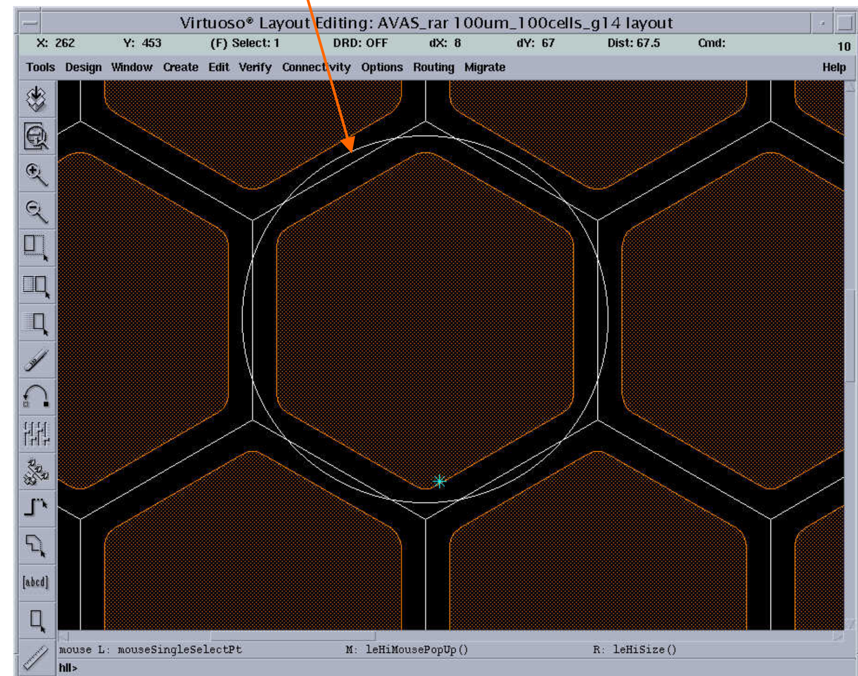
Matching of resistor requirements with bulk geometry

Actually a simple resistor problem (bulk resistivity and geometry)

- but carrier diffusion from top and bottom layer into the resistor bulk
- sideward depletion

-> device simulation necessary

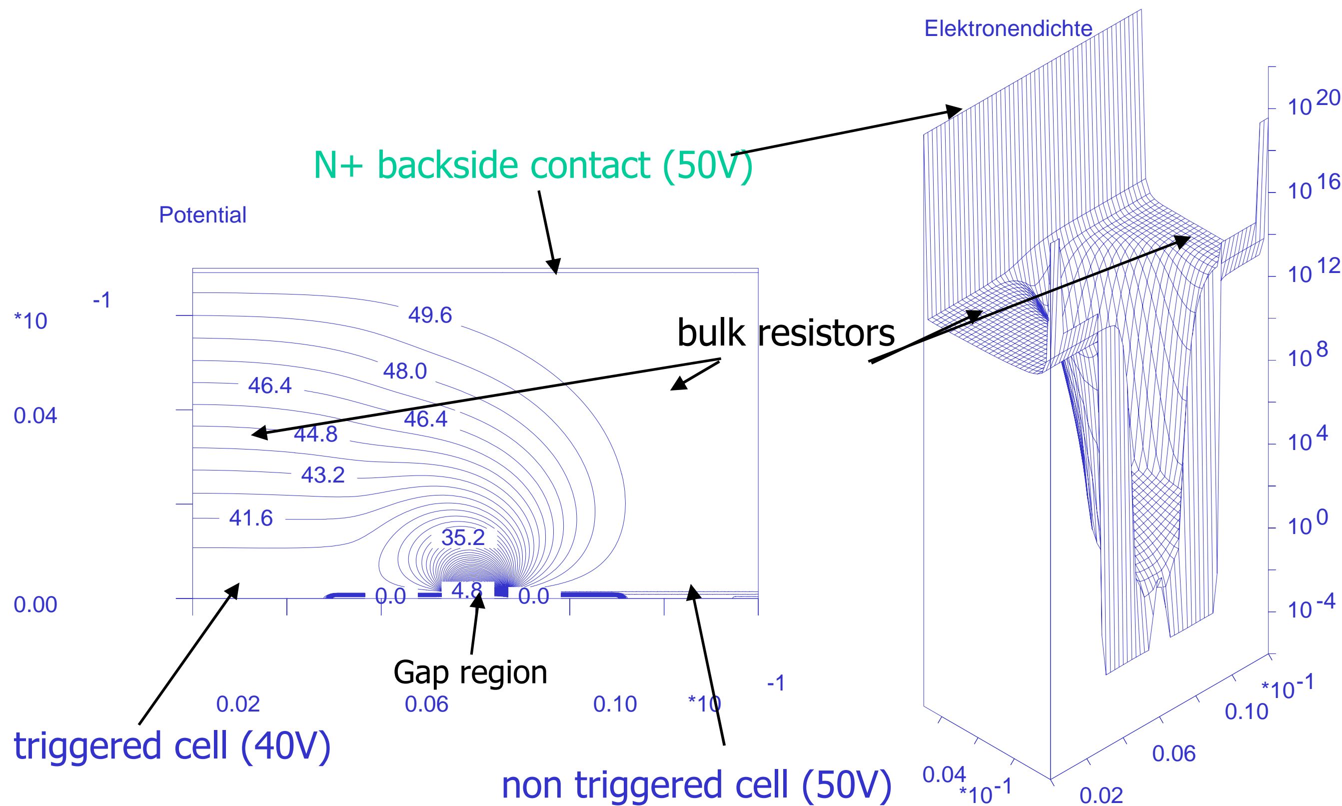
zylindrical approximation of hexagons for quasi 3d simulation



Simulation example 120μm pitch, 14 um gap, 70μm thickness

Potential

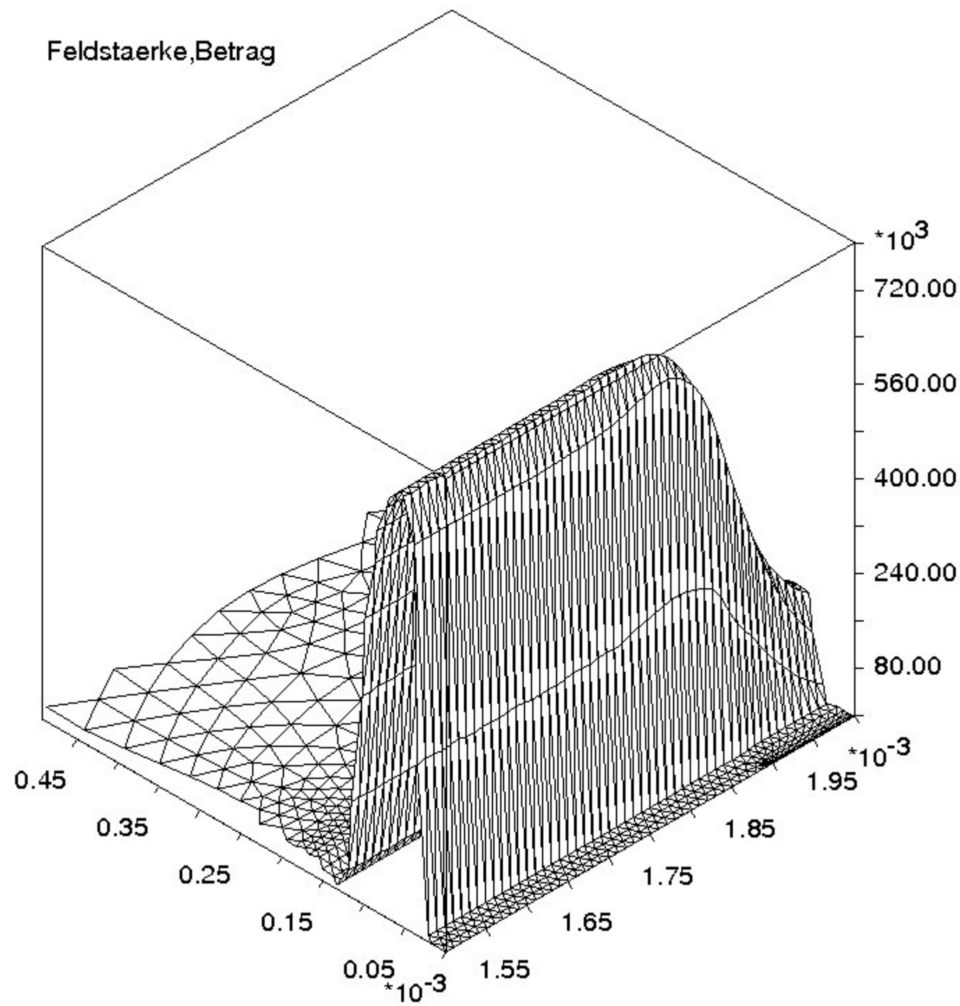
Cylindrical simulation (quasi 3D) $N_B = 3*10^{12} cm^{-2}$ (WIAS-TeSCA, ISE-TCAD DIOS)



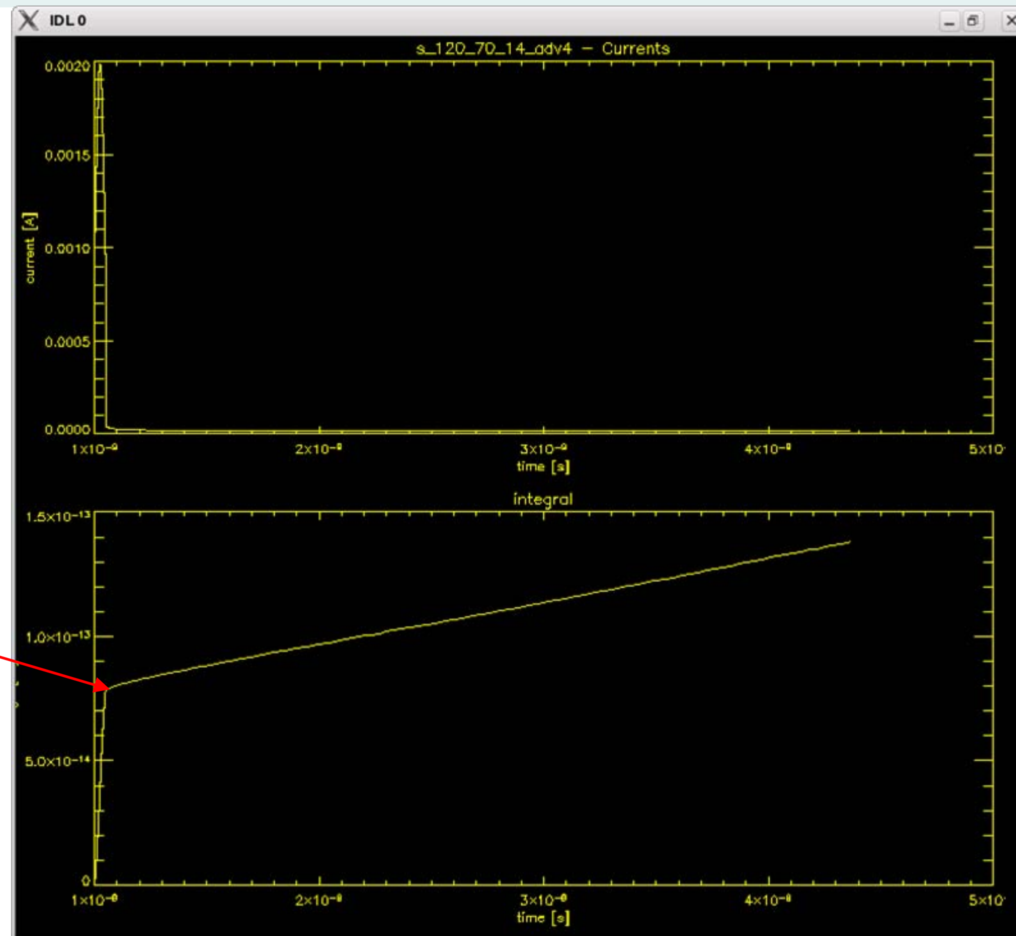
Complete separation of individual quench resistors

Every subpixel geometry needs an optimized bulk doping!

- Nice high field edge termination without guard structure



Signal height – given by (bulk) coupling capacitance



$8x10^{-14}$As

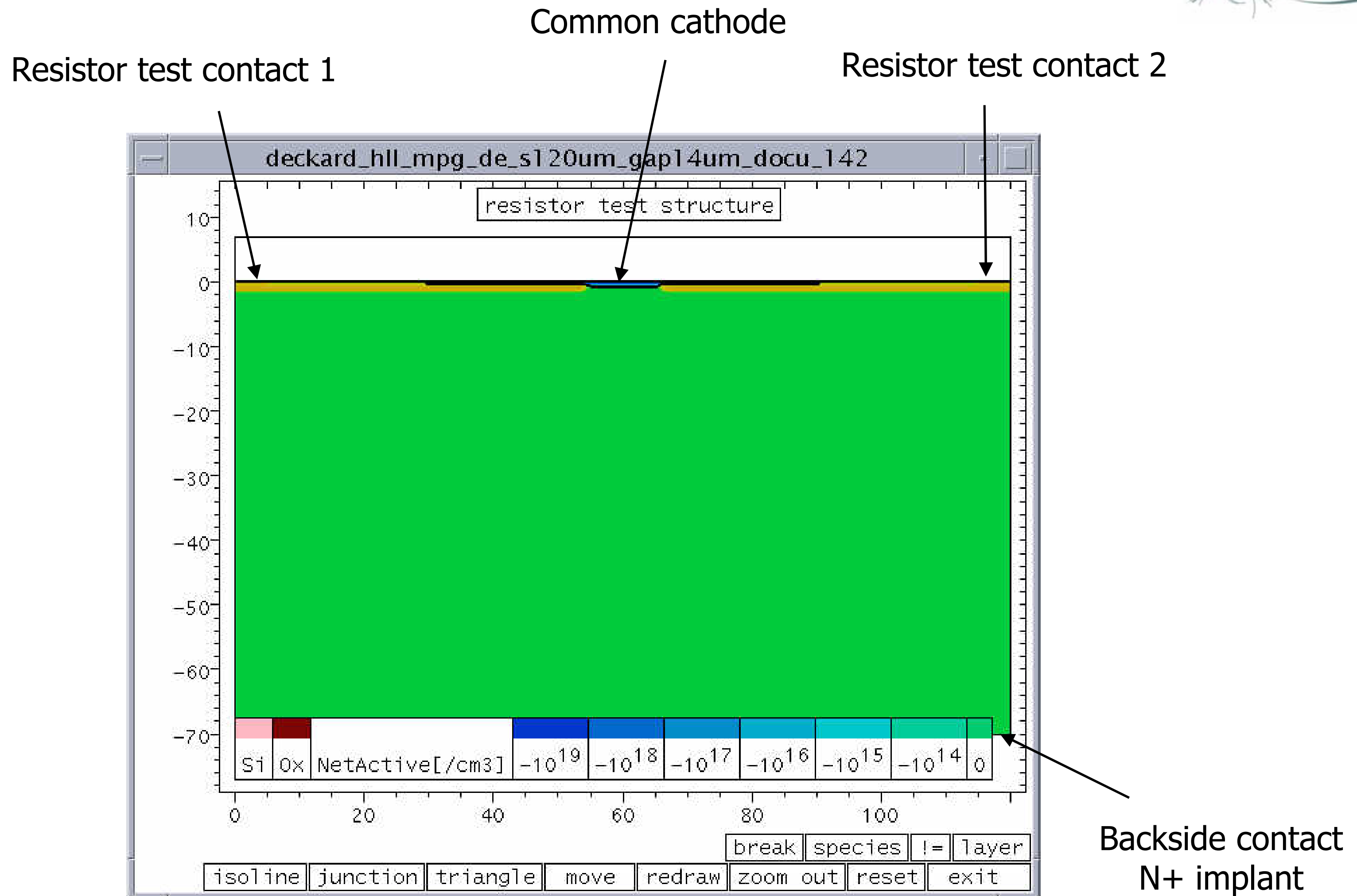
@6V overbias

C_{coupl} = 14fF

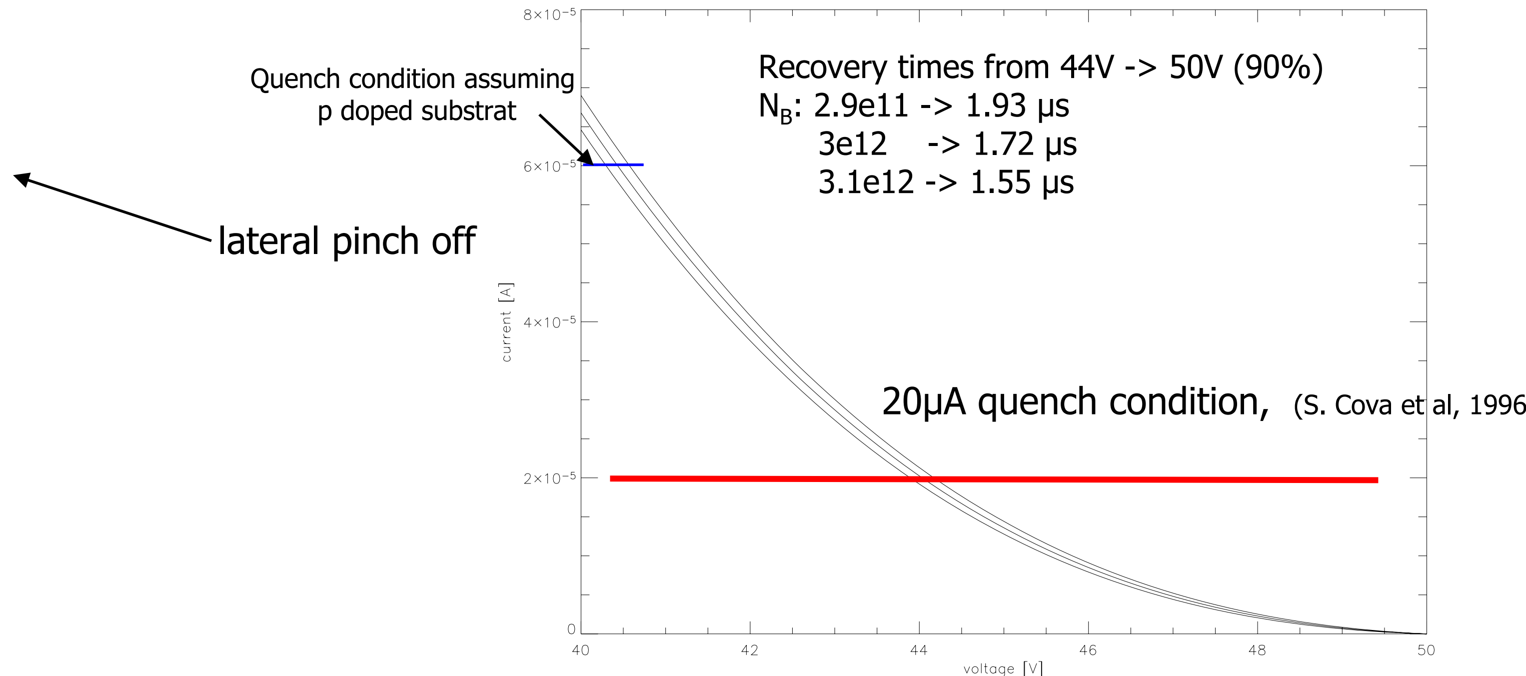
Total Matrix Capacitance

just given by the plate capacitance C' = eps /d = 1.5pF/mm² (d =70µm)

Resistor studies for device simulations



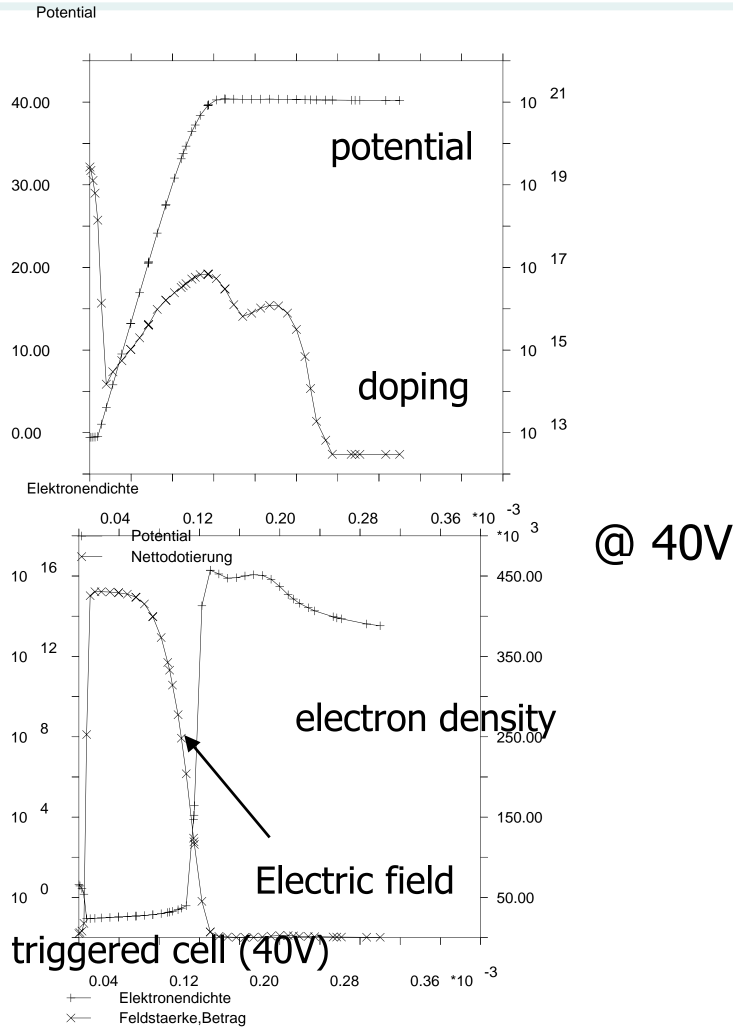
Quench condition – parasitic JFET behavior



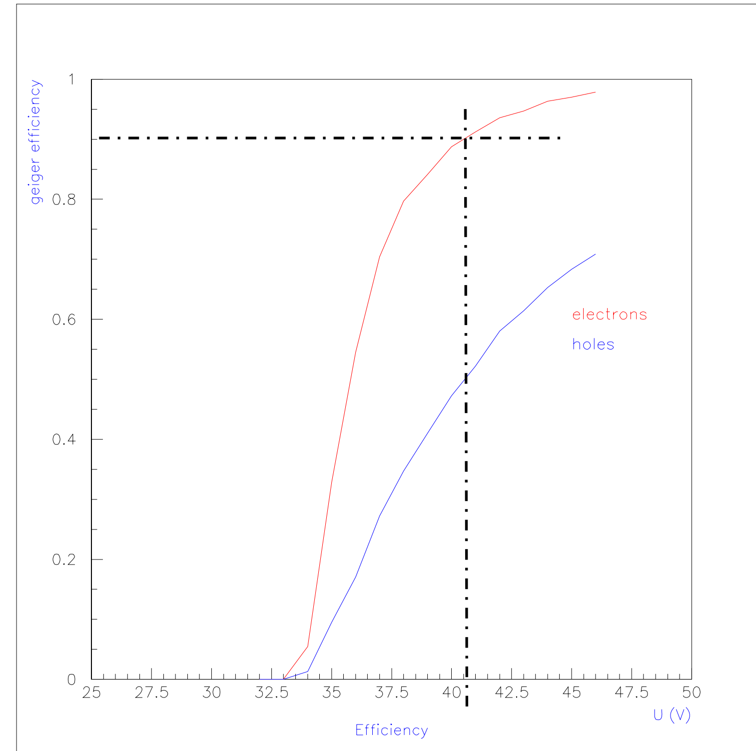
Deeper high field implantation ->diode capacitance reduction by a factor of 2 or 3 possible

But recovery times by a factor 3 - 4 longer than with an optimum adjusted polysilicon resistor

Geiger efficiency



MC - avalanche probabilty



Vbias-Vbreak = 6.5V -> 90%

PDE estimation

Hexagonal design pitch 150μm, isolation gap 20μm
geomatrical fill factor 75%

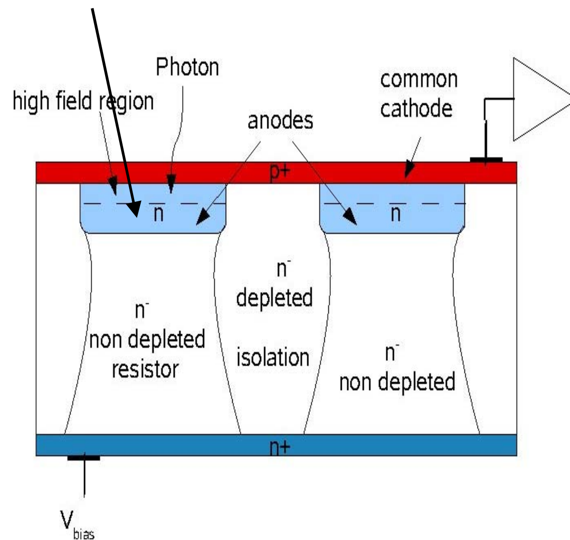
Optical entrance window: same as for backside illimunated devices: 90% @400nm
(see Jelena's talk)

Geiger efficiency : 90%

Product PDE: 61% (depends strongly on gap size)

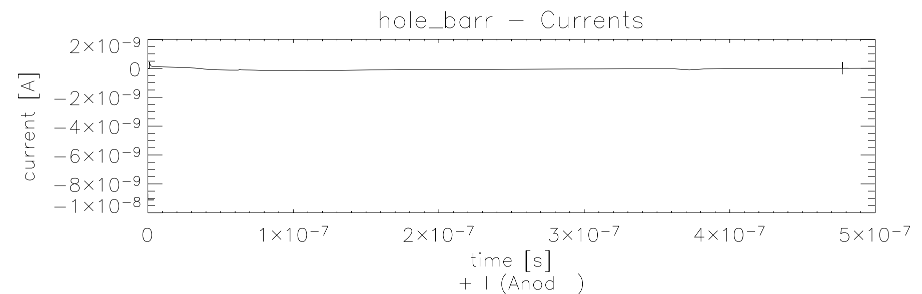
Cross talk – bulk contribution

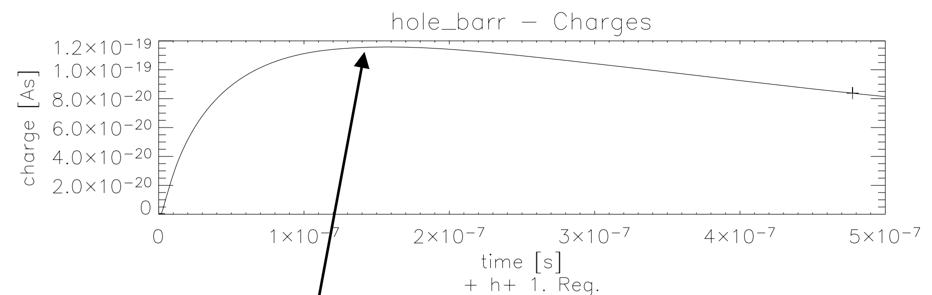
Highly doped high field region is a diffusion barrier for holes ($p\,n = n_i^2$)



device simulation

generation of 1000e/h pairs
in the bulk





Less than 1 hole in the high field region

Remarks on radiation hardness

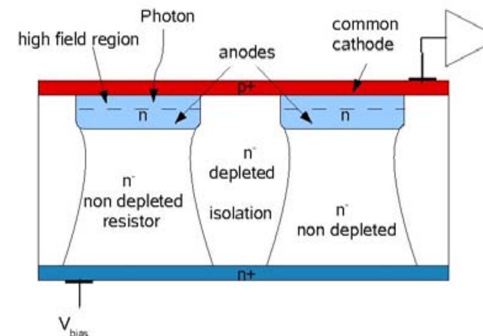
Bulk damage -> increase of darkrate, and afterpulsing
no difference to classical devices

Surface damage at Si/SiO2 interface
can become significantly already in the krad range
- fixed positive oxide charge generation
  -> flatband voltage shift, higher fields, edge breakdown
- generation of interface states (breaking of hydrogen bonds)
  -> increased leakage current, amphoteric traps

Avoid depleted interfaces
Free carriers (high doping densitys) neutralize radiation induced oxide charges, and occupies interface states preventing them from SRH generation

Ideal situation:
Highly doped surface within the array
no edges -> no lateral high field regions

(At the edge of the matrice is space enough for guard structures)



Pros and Cons

Advantages:

- no need of polysilicon (process complexity, minimum feature size, reliable resistance, obstacle for light, insulator breakdown problem)
- free entrance window for light, no metal necessary within the array
  -> easy antireflective coating
- coarse lihographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk?
- hopefully good radiation hardness

Drawbacks:

- required depth for vertical resistors does not match wafer thickness
  wafer bonding is necessary
- changes of subpixel size requires other material
- vertical 'resistor' is a JFET -> parabolic IV -> longer recovery times

Next steps

Prototyping at MPI-HLL

Proof of principle

Ordered: 50 SOI wafer (150mm), 70μm top wafer thickness, n-type, 1.8kOhmcm+/-70Ohmcm at ICEMOS (Ireland), 400€/wafer

Check reliability of specified wafer resistances

Suitable for a subpixel size of about 125μm

Minimum gap size? Optical crosstalk studies

Processing:

Currently mask design

6 mask steps (potential for reduction)

Optimized UV entrance window

Processing until early 2008

If successful: technology transfer to an industrial partner

Summary

A silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk is proposed.

Wafer bonding technique provides the required flexibility for quench resistor adjustment

replaces polysilicon and epitaxy

Geometrical fill factor is given by the need of cross talk suppression only

Very simple process, relaxed lithography requirements

Pros and Cons see above

Prototyping at HLL:

SOI Wafer ordered

Design is ongoing.

UV-sensitive samples available early next year.

Material specs

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Product analysis

Resistivity [average ± std. dev] (Ohm-cm)	1879,2 ± 65,96
Thickness [average ± std. dev] (µm)	352,7 ± 1,43
TTV [average ± std. dev] (µm)	3,1 ± 0,57
Bow [average ± std. dev] (µm)	1,3 ± 1,78
Warp [average ± std. dev] (µm)	19,4 ± 4,93

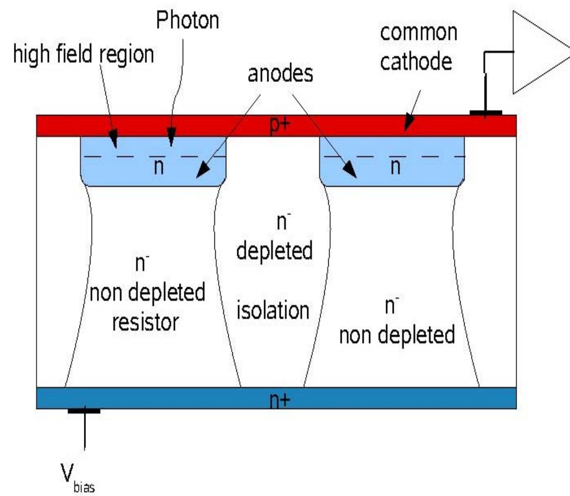
Certification

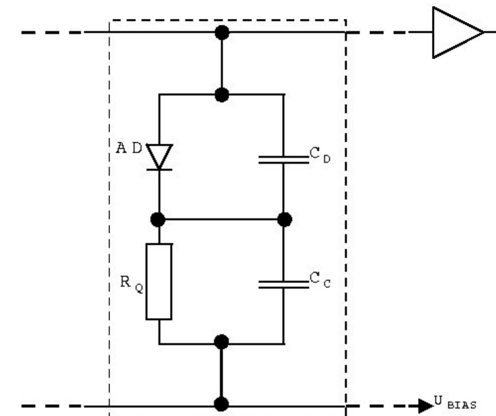
It is hereby certified that the product resistivity conform to the specification based on actual measurements following an analysis performed according to ISO 3951 standard.

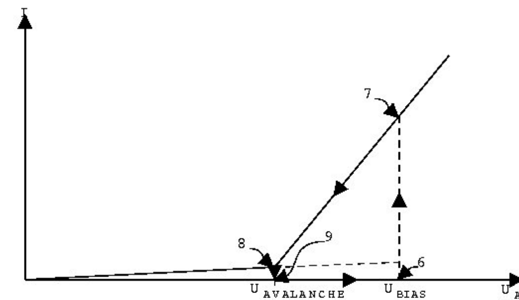
Additional product properties are in conformance with the specification according to the general process control and/or final inspection.

Resistivity is measured on four wafers measured according to a modified ASTM F-81 sampling plan C by use of a four point probe; once in the centre, four at the half radius and 4 times at 10 mm from the edge.

Signal generation







Anode discharge after trigger
Fast signals are coupled by Cc