DCD Chip for Belle II

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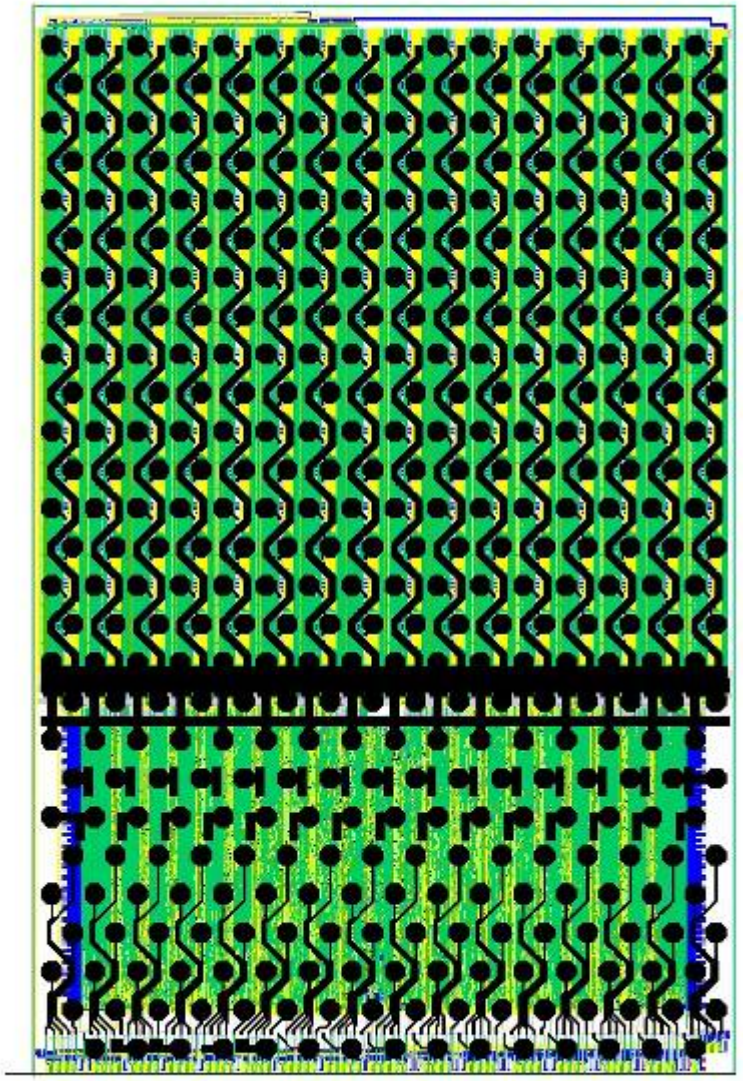
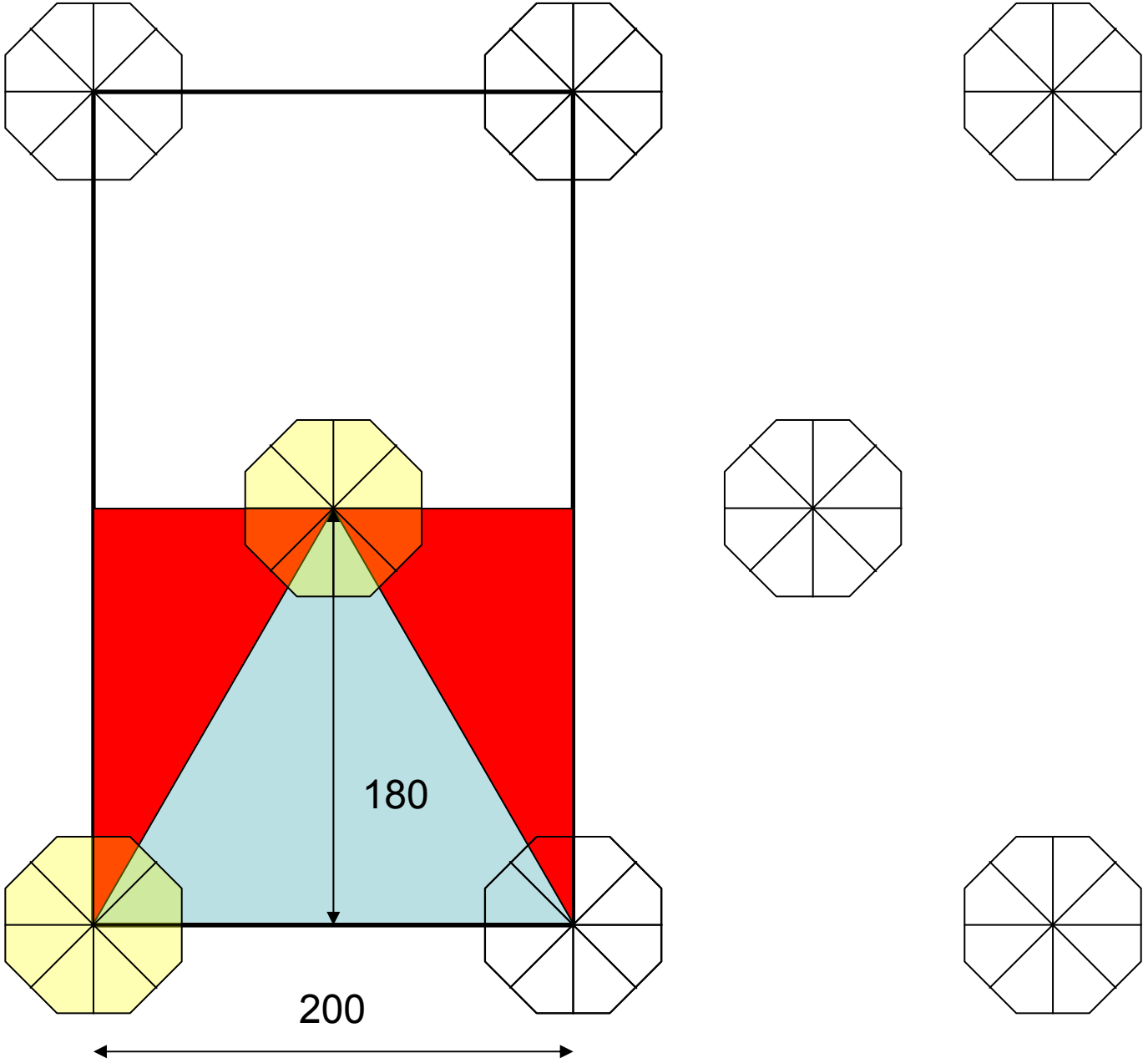
Geometry

- Size: 3240X4969 um
- 256 analog inputs
- 64 digital outputs
- 32 digital inputs for offset compensation
- 5 JTAG pads for slow control
- 3 fast sequencer signals – clk, reset and strobe
- 2 digital monitor outputs
- Analog monitor and injection
- 4 power voltages and 2 grounds
- Totaling: 416 bumps
- Supply current:
  - Analog: 300-500 mA
  - Digital: 300 mA
- Designed sampling period: ~92 ns (350 MHz)
- Simulated 30n-60 nA
- 8-bit precision
- Lead bumps and Al redistribution layer used



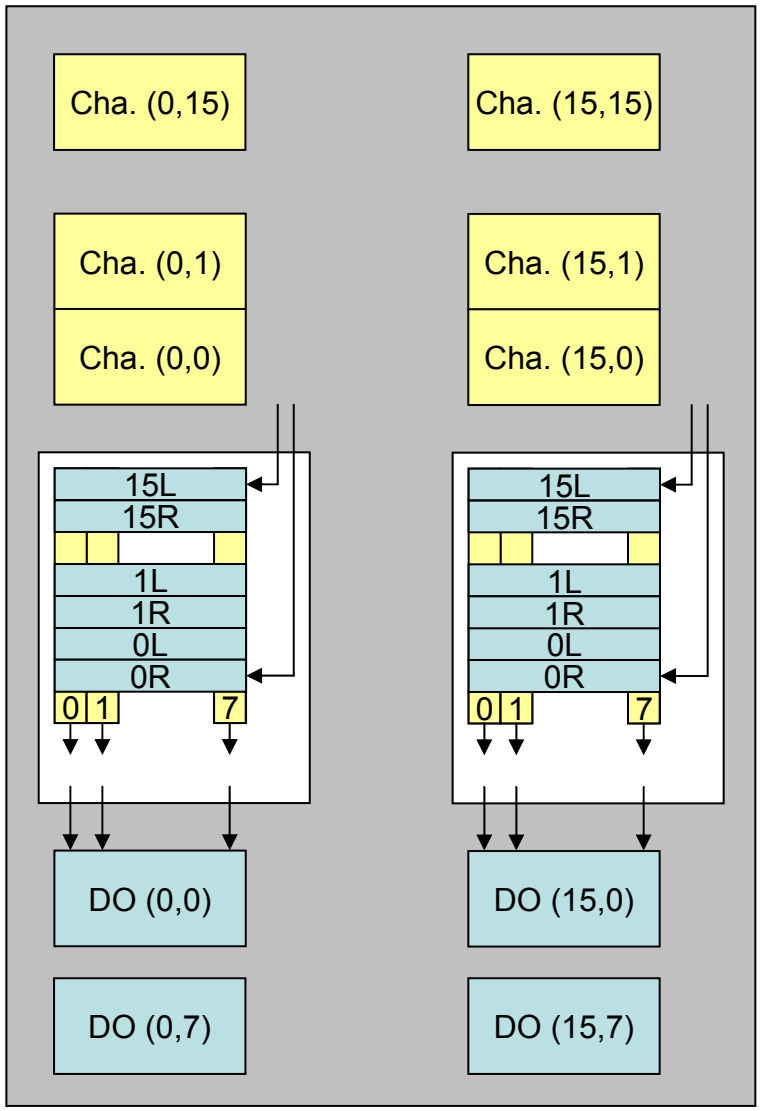
Pad Geometry



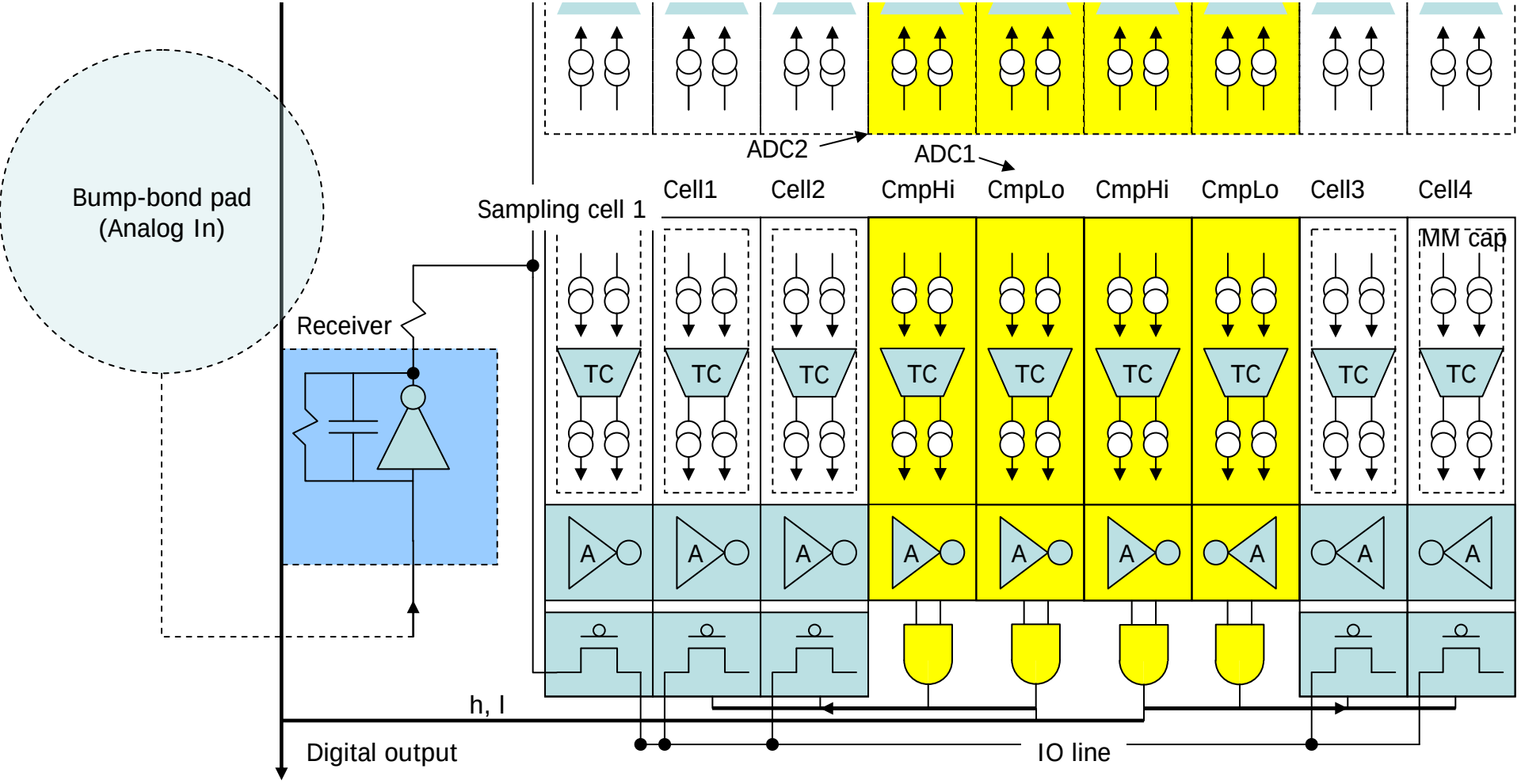
Features

- Trans-impedance amplifier with variable gain and shaping time
- 8-bit ADC
- 2-bit DAC for offset compensation
- Digital derandomizer provides parallel digital output
- Large decoupling capacitors on the chip
- Single ended digital output for 400 MBit transfer with 200 Ohm in chip termination and 1 mA bias current = 200 mV swing

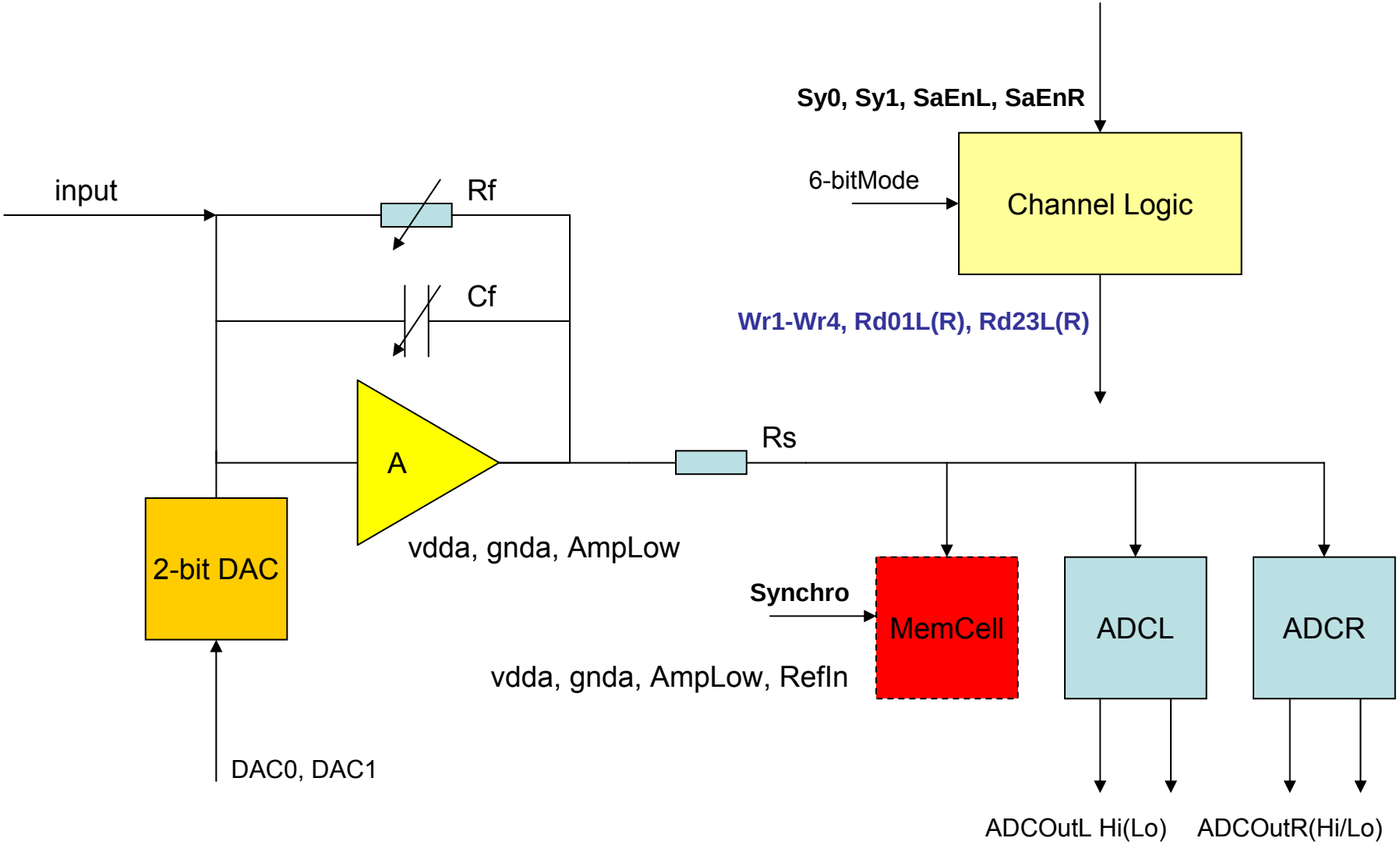
Chip architecture



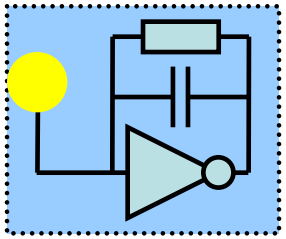
Analog Channel

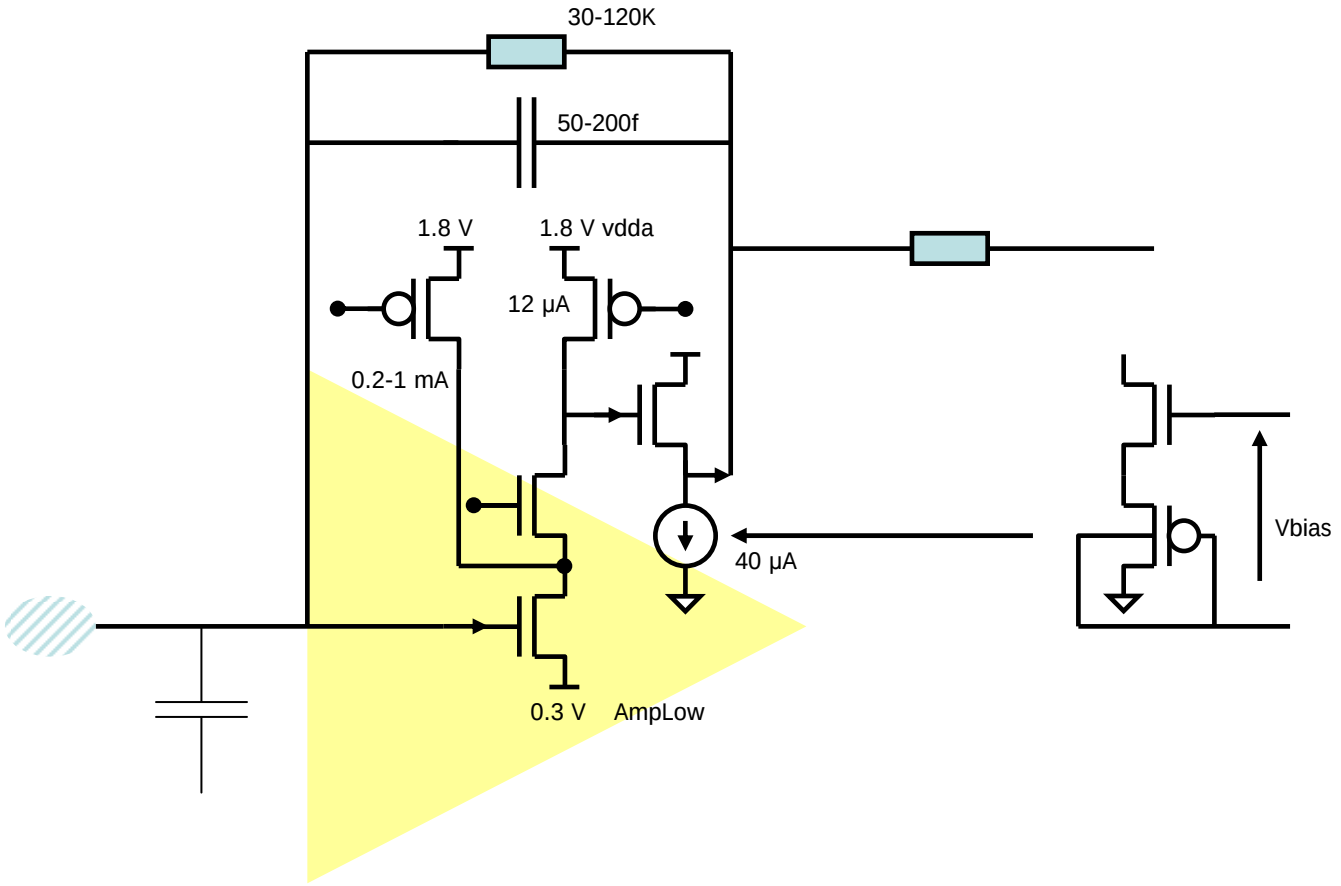


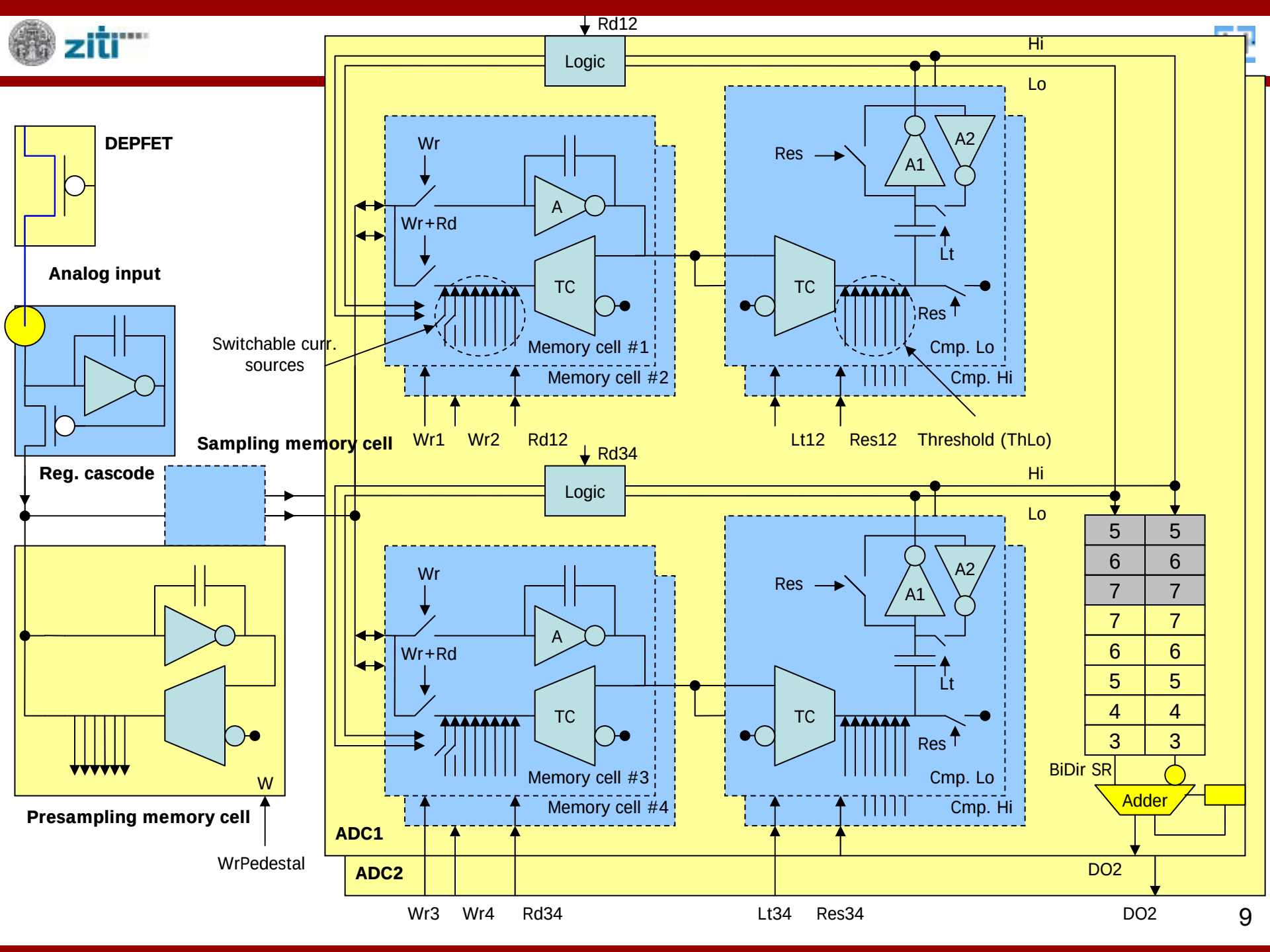
Analog Channel



Trans-impedance amplifier



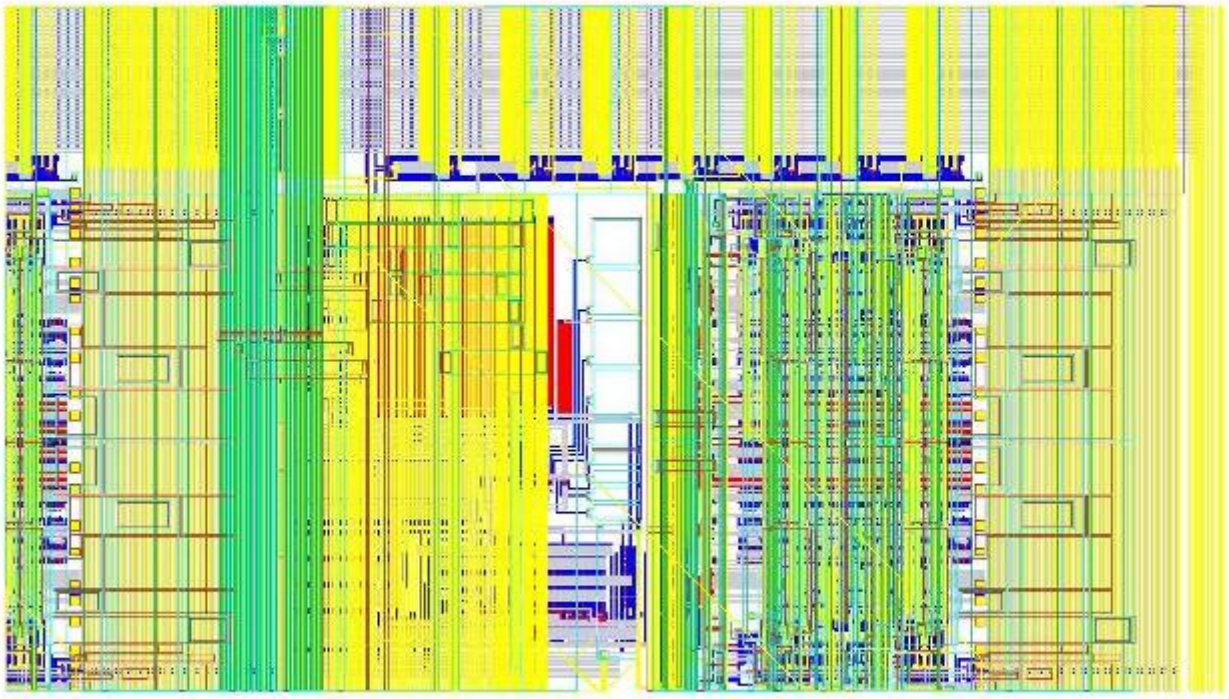



DEPFET
Analog input
Reg. cascode
Sampling memory cell
Presampling memory cell
W
WrPedestal
Switchable curr. sources
Rd12
Logic
Hi
Lo
Wr
Wr+Rd
A
TC
Memory cell #1
Memory cell #2
Res
A1
A2
Lt
Cmp. Lo
Cmp. Hi
Wr1
Wr2
Rd12
Lt12
Res12
Threshold (ThLo)
Rd34
Memory cell #3
Memory cell #4
ADC1
ADC2
BiDir SR
Adder
DO2
Wr3
Wr4
Rd34
Lt34
Res34

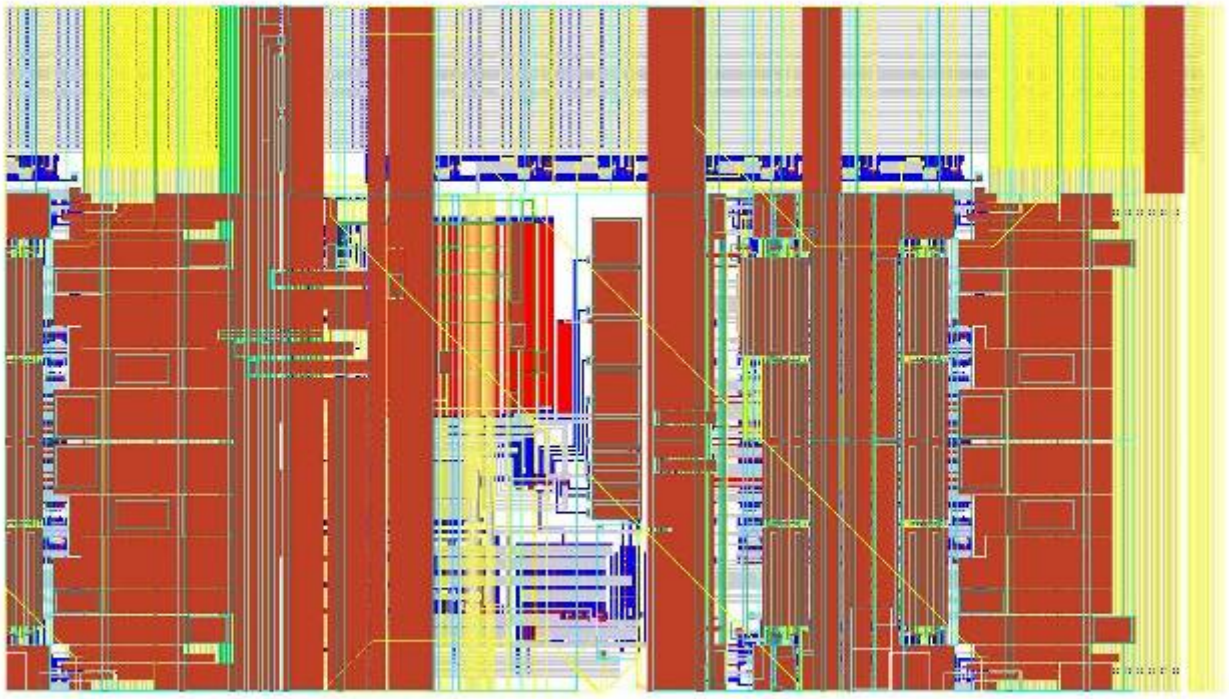
Layout

- Very big effort for power distribution and shielding
- 136 000 gates in digital block
- Very few control pads
- Synthesized digital block

Layout - analog channel



Layout



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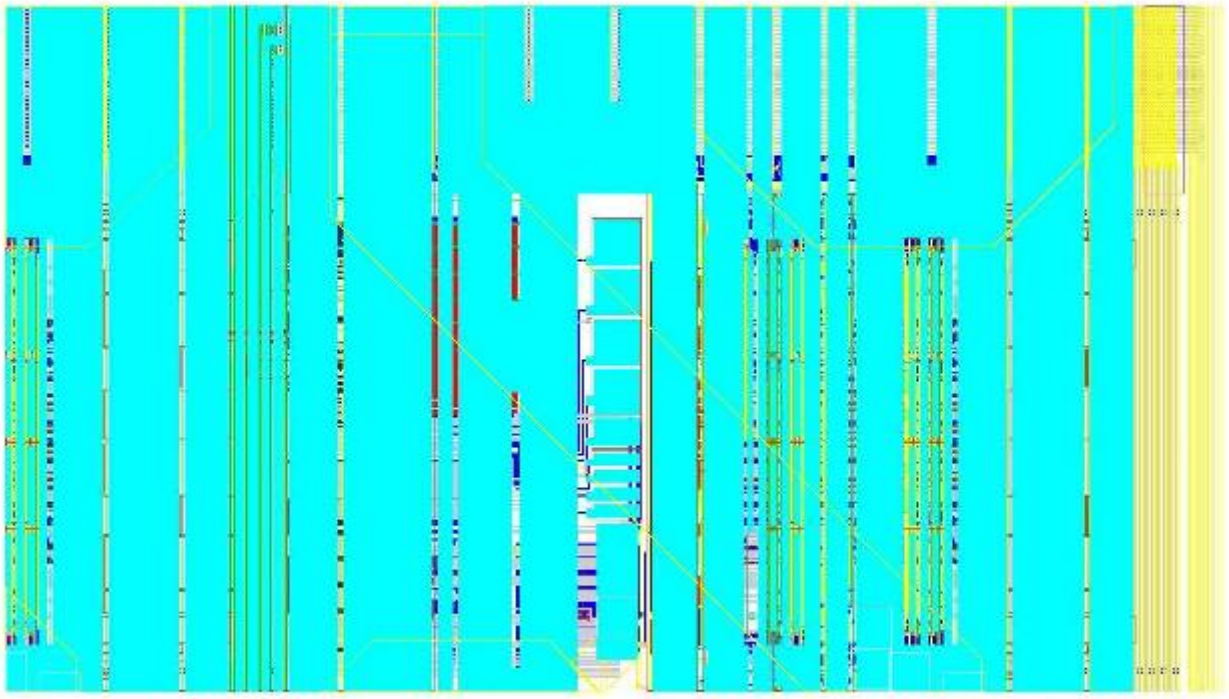

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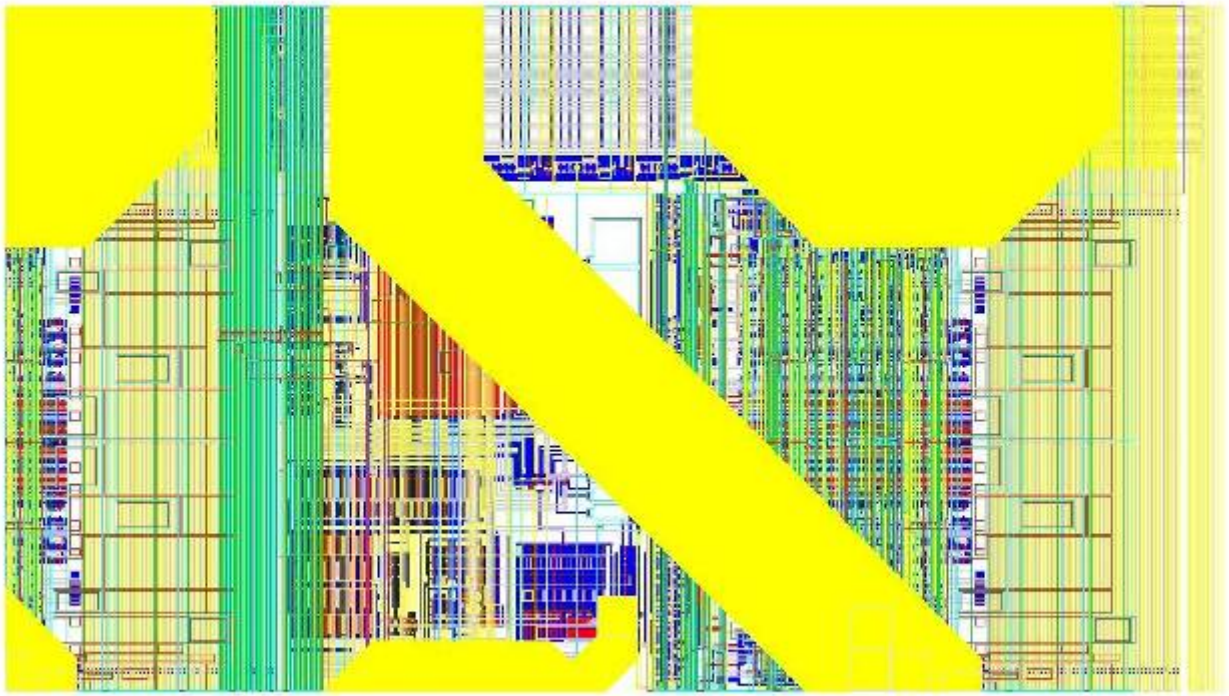

Layout digital block