Minutes (action items)

PXD6 matrix metalization

Two metal layers, no UBM

- pixel ordering important for on-chip data reduction ("hit pairing" on DHP to reduce bandwidth requirements), current implementation expects to process the four simultaneously sampled rows to be within one continuous block, no hit pairing for **ILC type** pixels/matrix
- provide support on the PXD6 large matrices for DHP 1.0 (half size chip, 32 inputs), different options discussed:
  1. split wafer run for different metal masks
  2. common landing pattern for DCD_RO and DHP 1.0 (maybe too difficult)
  3. mixed layout for certain matrix variants: 3x DCD_B + 2x DCD_RO + 1X DHP 1.0
- **actions**:
  1. design DHP landing pattern, re-use input pattern from DCD_RO (BN, by end of December)
  2. send GDSII (large matrix, DCD_RO) + technology files to BN (HD)

Bump bond test adapter

Only one metalization layer available!

- DCD_B + DCD_RO
- DCD_B + DHP 1.0
- optional: DCD_B + 2x DHP 1.0, study sync. issues between multiple DHPs
- optional: DCD_B + 1x DCD_RO + 1x DHP 1.0, DCD outputs shared between DHP and RO chip (maybe not so important)
- SW_B
- SW 4 (backup)
- **actions**
  1. DCD_B + DCD_RO adapter available when DCD_B is shipped (Feb '10 ?)
  2. DHP related layouts could be deferred

Interface between DCD_B and DHP

- current DCD_B manual (rev 0) is not up to date
- control signals: bitClk, syncRst, strb (optional only for DCS mode), **no additional sequencer signals**
- verilog model available but output port ordering not equivalent to submitted chip
- DCD_B inputs: 1.8V CMOS (need full swing drive)
- **actions**
  1. update manual (HD)
  2. check pin/port ordering (HD, BN)

DHP design

only discussed briefly

- single sampling mode is baseline
- different schemes for dynamic pedestal calculation currently being studied
- effect of common mode correction (+ error due to cm over-estimation) under

investigation
- **actions**
  1. simulate different signal processing schemes (BN)
  2. check DCD_B (+ Sw_B) synchronization requirements (BN, HD)
  3. check chip edge design rules (BN)

Electronic simulations

Full simulation with DEPFET model (3 pixels) + distributed RC line + DCD_B (one channel) running (HD)!

- simulated drain current signal does not show over- and undershoots as seen by the DCD2 measurements during transitions of the clear (and gate) signals
- **actions**
  1. check influence of line inductance for gate, clear, drain and wire-bonds (HD)
  2. provide latest measurement results from DCD2 (BN)

Test system development

- discussed proposal of modular test setup
- maybe not all permutations of chips and matrices needed
- bump bonded matrix assemblies (128 x 16, 128 x [120, 160, 180]) do not really benefit from modular conncept
- make at least small wire bond matrices exchangeable
- yield of DCD_B + DCD_RO assemblies ? (replacement of mounted Si-adapter should be unproblematic)
- **actions**
  1. provide openings in the PCB stack for access of the matrix backside with laser (9 mm working distance for BN laser setup) (HD)
  2. or mount matrix support PCB upside down (HD)
  3. check availability of additional LVDS lines on IGEL board as possible upgrade of Manuels board (V4) (MPI)
  4. use SVN repository (same SVN server as for S3a/b) for common V4 system FW and app. development (BH, HD)
  5. DCD_B test (HD)
  6. DHP emulation + integration of V4 system in DAQ for TB (BN)

not covered

- flex design
- impact of common mode, SNR, pedestal dispersion (effective ADC dynamic range) etc. on DHP signal processing

-- HansKrueger - 03 Dec 2009

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