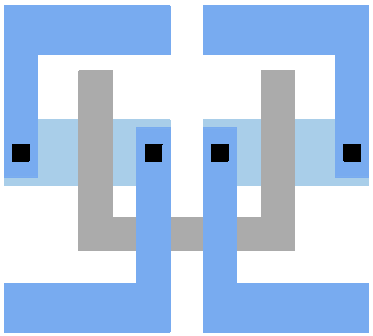
UNIVERSITÄT
HEIDELBERG

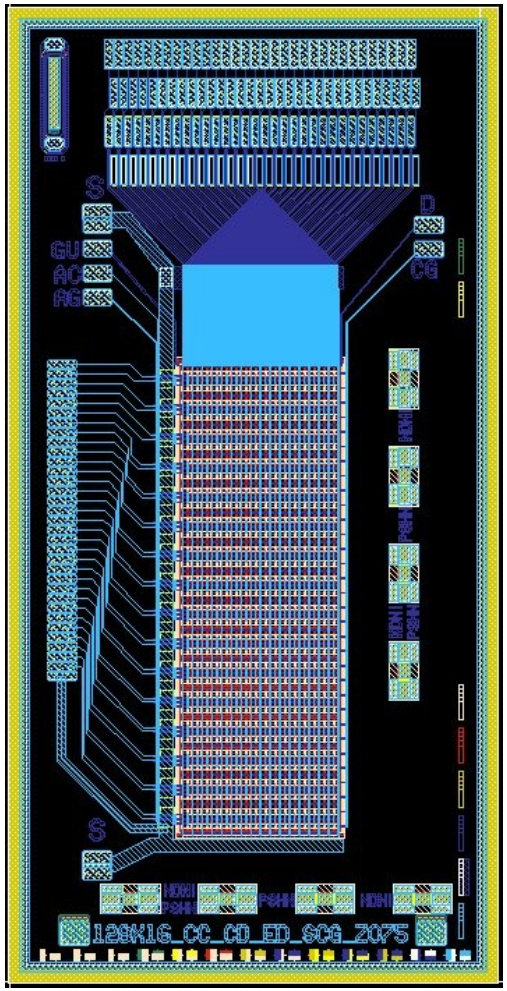
PXD6 readout and steering chip interconnect

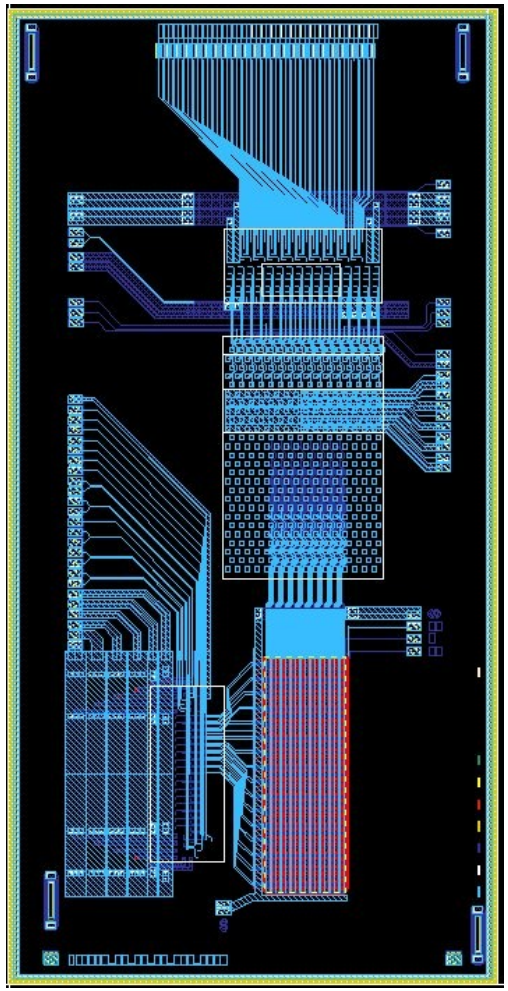


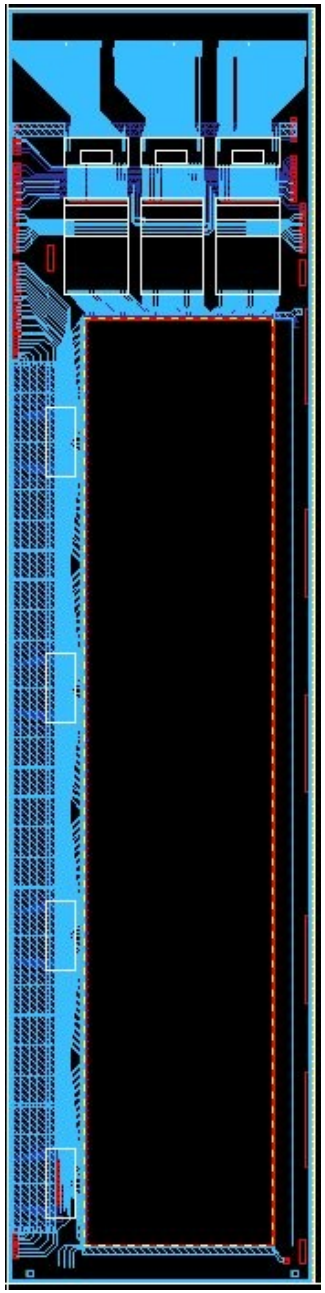
Schaltungstechnik
und Simulation

PXD6 Matrix Overview

- wirebond matrix: 128x16, 128x8
- bumpbond matrix small: 128x16
- bumbond matrix large: 768x120, 768x160, 768x180





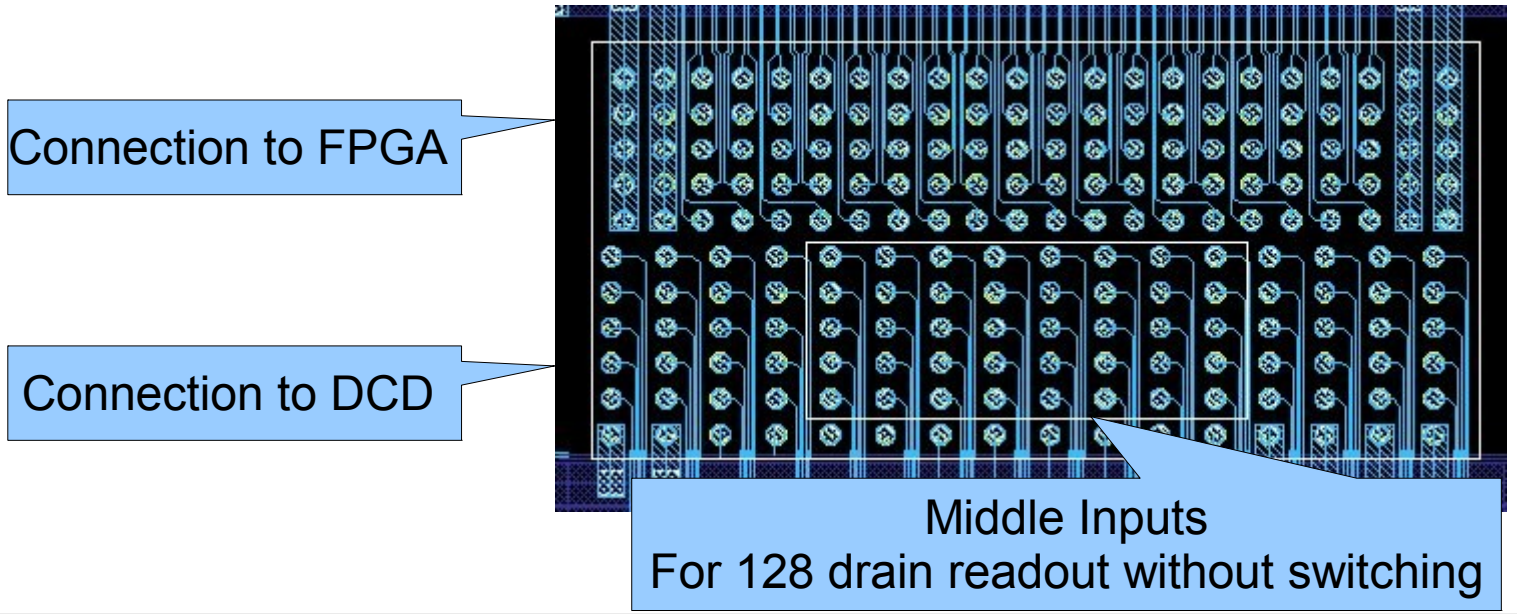


PXD6 Readout

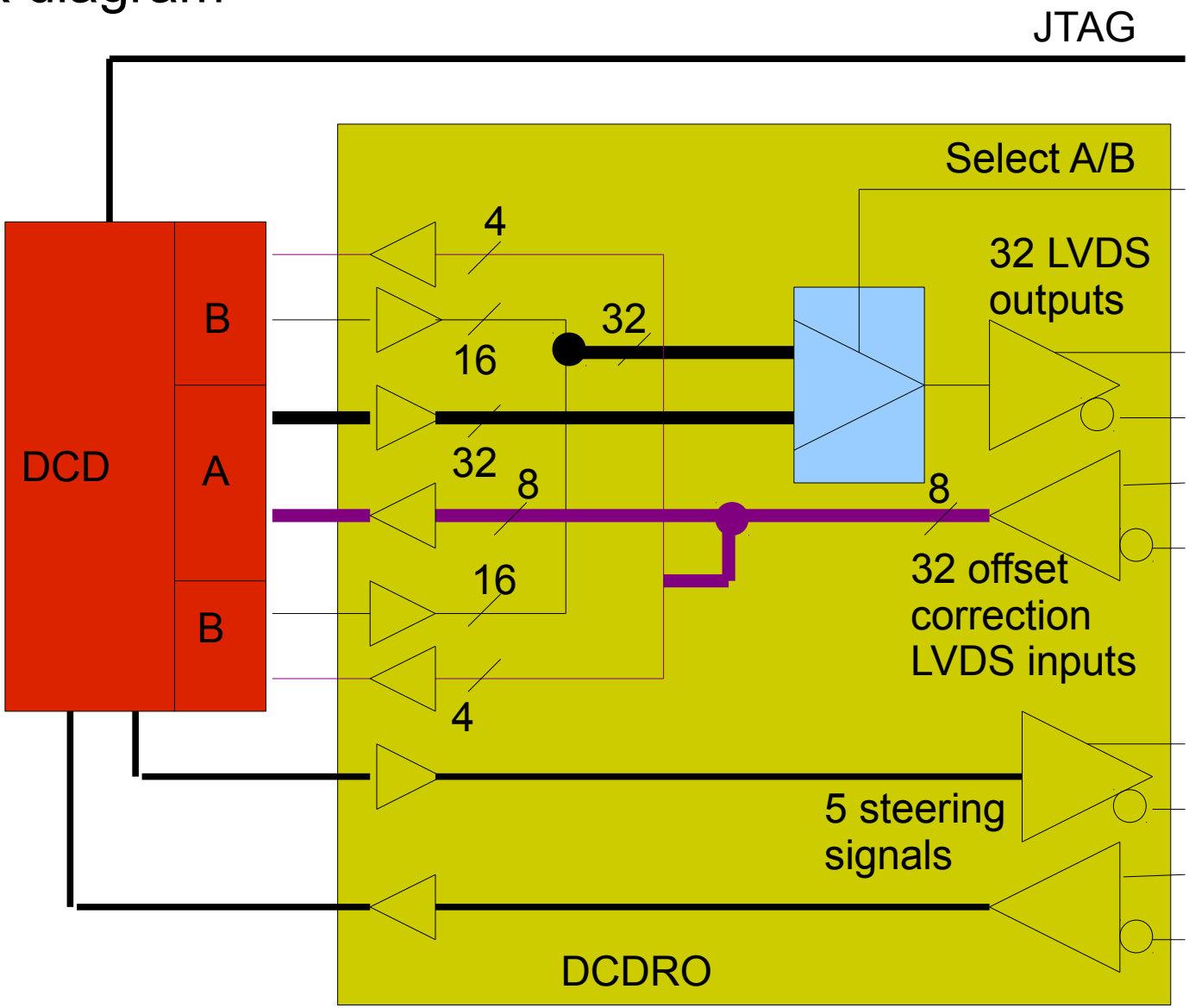
- Bumpbond matrices
  - chip are flipped onto the matrix
  - matrix is wirebonded to hybrid PCB
- wirebond matrices
  - all chips have bump bonds only
  - need adaptor to connect bumpbond chips with wirebond matrix
  - chips flipped onto adaptor
  - adaptor wirebonded to matrix and to hybrid PCB
- operating DCD without DHP
  - DCD cannot drive long lines to FPGA
  - converter chip needed

DCDRO Converter Chip

- DCD Outputs cannot drive long lines
  - need converter chip if DCD operated without DHP
  - convert to LVDS, integrates (slow) multiplexer to access all DCD outputs
- 1x2 miniASIC (1525µm x 3280µm)
  - fits DCD width → all DCD I/Os connected (if flipped onto matrix)
  - chipsize cannot contain LVDS pairs for all DCD I/Os → multiplexer needed
- multiplex between 4 middle and 4 outer DCD slices
  - matrix with 128 drains can be read out without switching

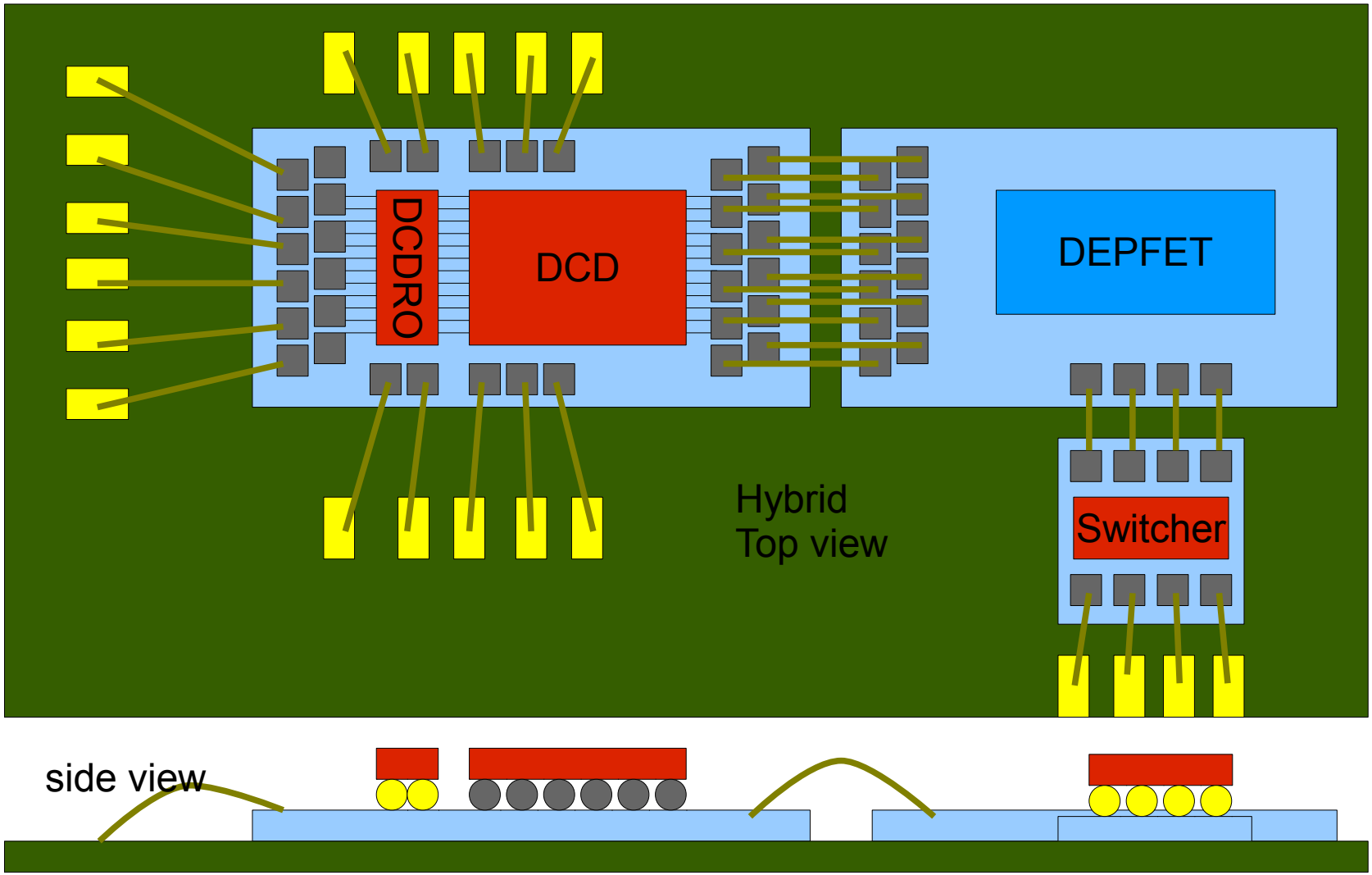


- Block diagram

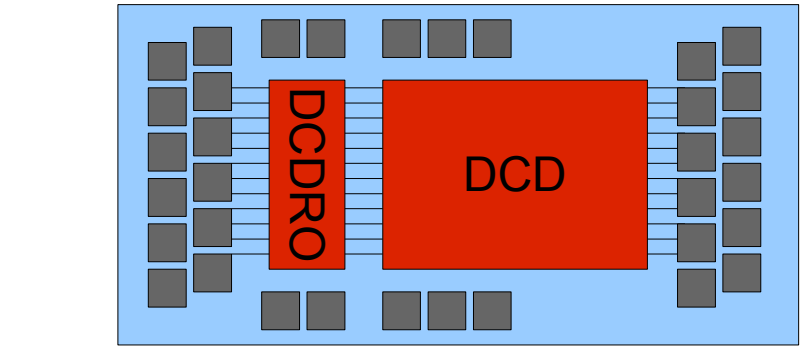


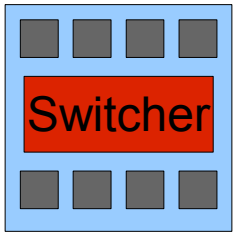
Wirebond Adaptor

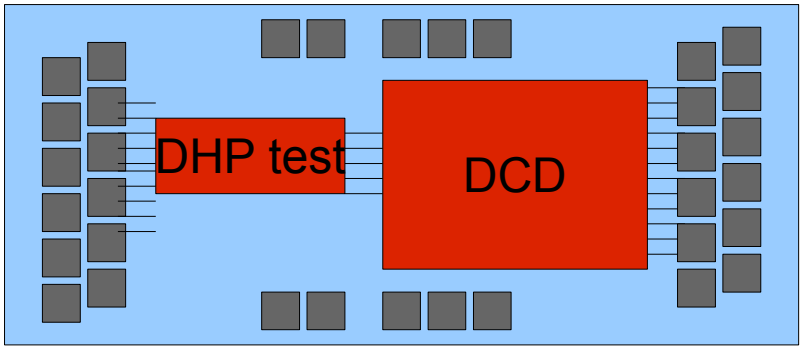
- DCD-B with DCDRO converter chip on one adaptor
- Switcher-B on another adaptor



- suggested types





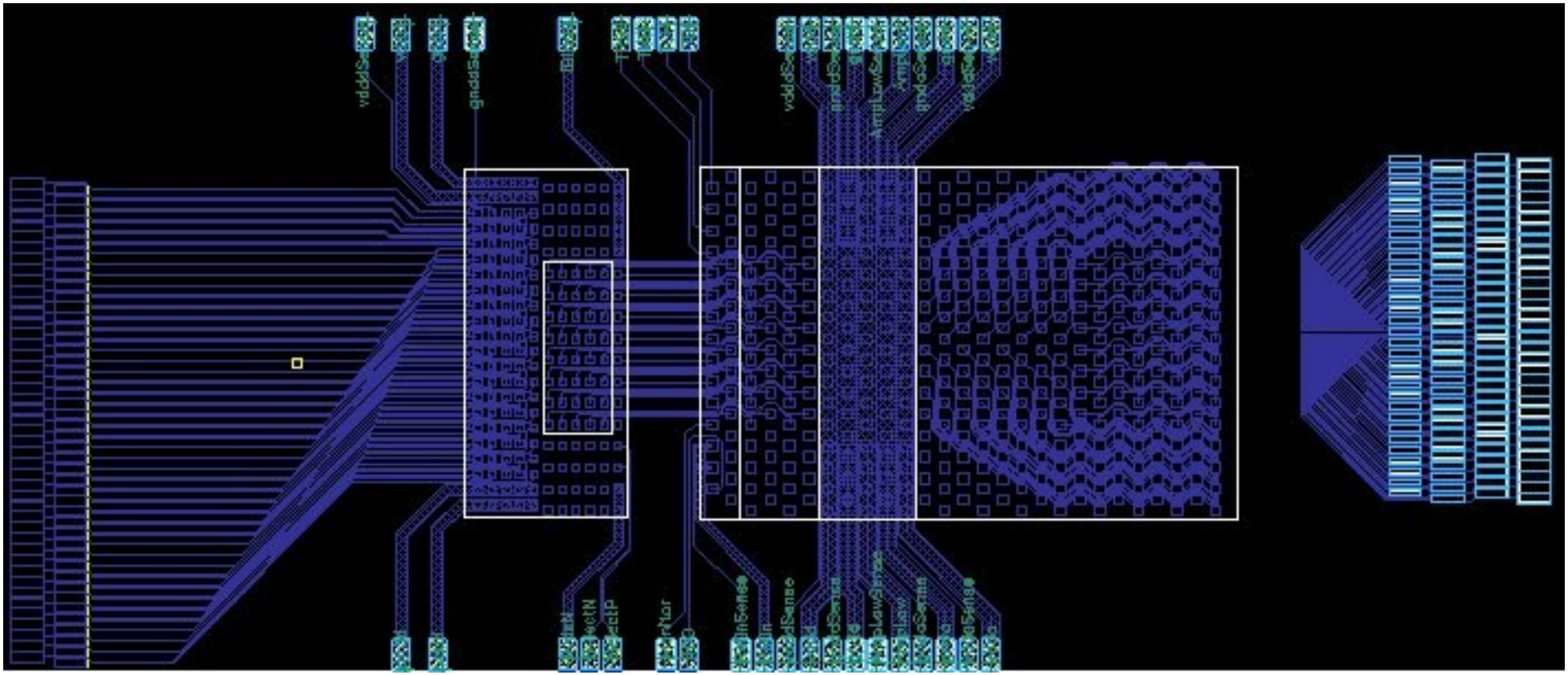


more?

Wirebondadapter facts

- Wirebondadaptor will be silicon with one metal layer
  - produced at HLL
  - metalized wafers at HLL available
    - need only masks, etching, dicing
  - can be processed out-of-order
  - ~5 weeks production time
- DCD-B + DCDRO
  - 128 drains connected different than on 2-layer matrices
  - only middle DCD slices connected
- DCD-B + DHP/2
  - design DHP/2 footprint with respect to 1 layer accessibility of pads
  - or need 2 metal layers on adaptor
    - longer processing time
    - needs to be sheduled

DCD-B + DCDRO Wirebondadapter



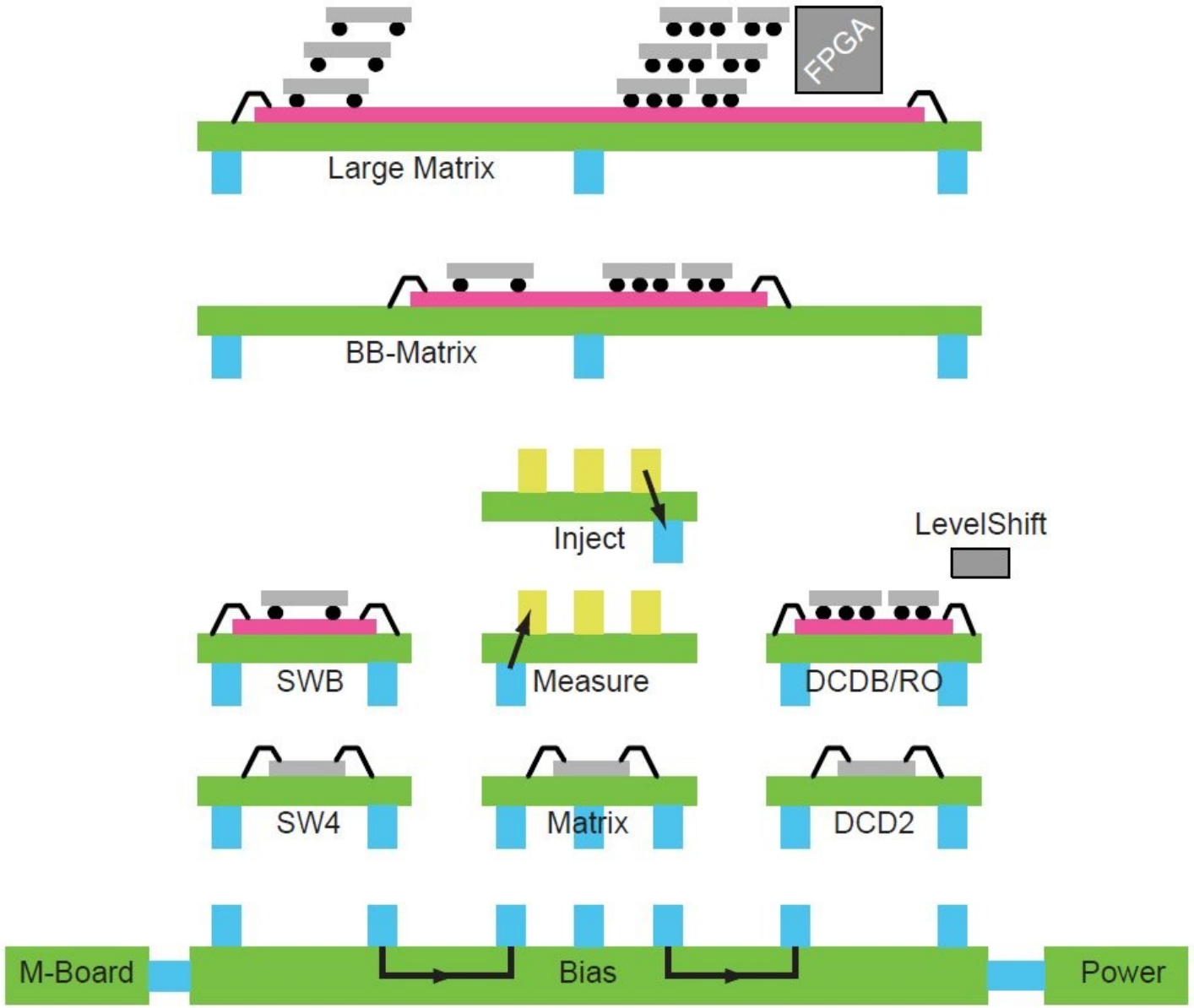
Large Matrix Design

- DHP/2 footprint instead of DCDRO?
  - different metal masks → one for DCDRO-only design, one for DHP/2
- DHP footprint
  - fix footprint soon
  - different metal masks

Hybrid Types

- different matrix ↔ chip combinations need different hybrids
  - different supplies, control lines, pad positions
- combinations:
  - wirebond matrix with wirebond adaptor
    - DCD-B+DCDRO; Switcher-B
    - DCD-B+DHP/2; Switcher-B
    - DCD-B+DCDRO; Switcher4
    - DCD-B+DHP/2; Switcher4
  - bumpbond matrix with 128 drains → 1DCD
    - DCD-B+DCDRO; Switcher-B
  - bumpbond matrix with 768 drains → 3 DCDs
    - DCD-B+DCDRO; Switcher-B
    - DCD-B+DHP; Switcher-B
      - need to define footprint until end of year
- which combinations are needed??
- tried to keep order of signals. only positions differ

Modular Hybrid

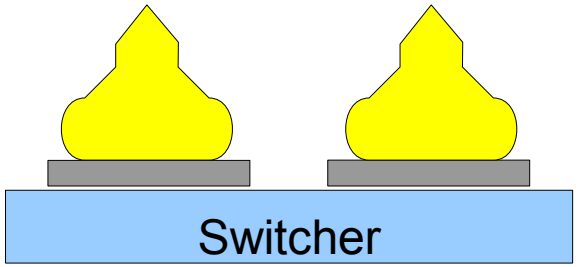


PXD6 Bump Bonding Summary

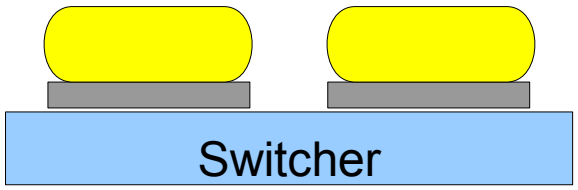
- rely on solder bumping → broken chips can be desoldered
- Al-pads not wettable by solder
- different bumping technologies for multi project wafer runs
  - DCD-B: commercial solderbumping by chip manufacturer
  - DHP: commercial solderbumping by chip manufacturer
  - Switcher: no commercial bumping available by manufacturer
    - we don't receive wafers → no commercial processing for solder bumping
    - have to place solder bumps on our own
  - DCDRO: commercial solderbumping not feasable due to pitch restrictions
    - use gold stud bonding with or without solder balls
  - PXD6: no commercial bumping or under bump metallization
    - have to place gold studs
    - final PXD has copper layer

Single Chip Solder Bumping

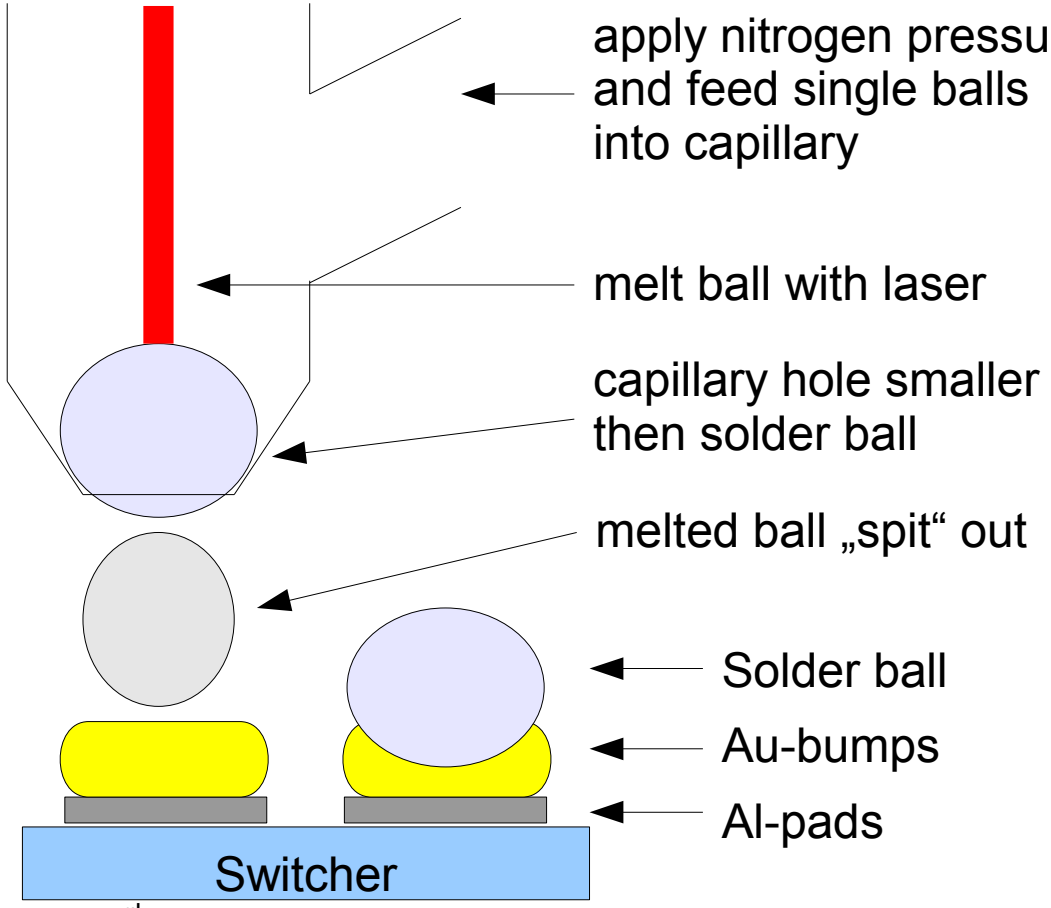
- use coined gold studs as an under bump metallization
- place solder bumps ontop using PacTec solder jetting technology
  - 60µm minimum ball size available
  - SnAgCu solder
  - Pb-free



1st : place goldstud



2rd : coin gold studs



3rd : jet solder balls