HEC HV - LV Interlock System

Teresa Barillari MPI Meeting 28 Jan. 2005

- Introduction
- JCOP and ELMB Framework and New HEC Panels
- HV - LV Interlock System

Introduction

- Work is going on to rebuild the final HEC LV Control System in PVSS to comply the JCOP and ELMB Framework
- A first version of this software will be used at the cold test in February 2005
  - The main idea is to rebuild all the main PVSS panels used during the HEC-EMEC-FCAL test-beam in 2004 into the new HEC LV Control System
- Work is also going on to build a final HEC HV - LV Interlock System
  - We want to avoid that any of the PSBs in the cryostat get damaged. To minimaze this risk is required that the HV channels stay off if the LV channels are off.

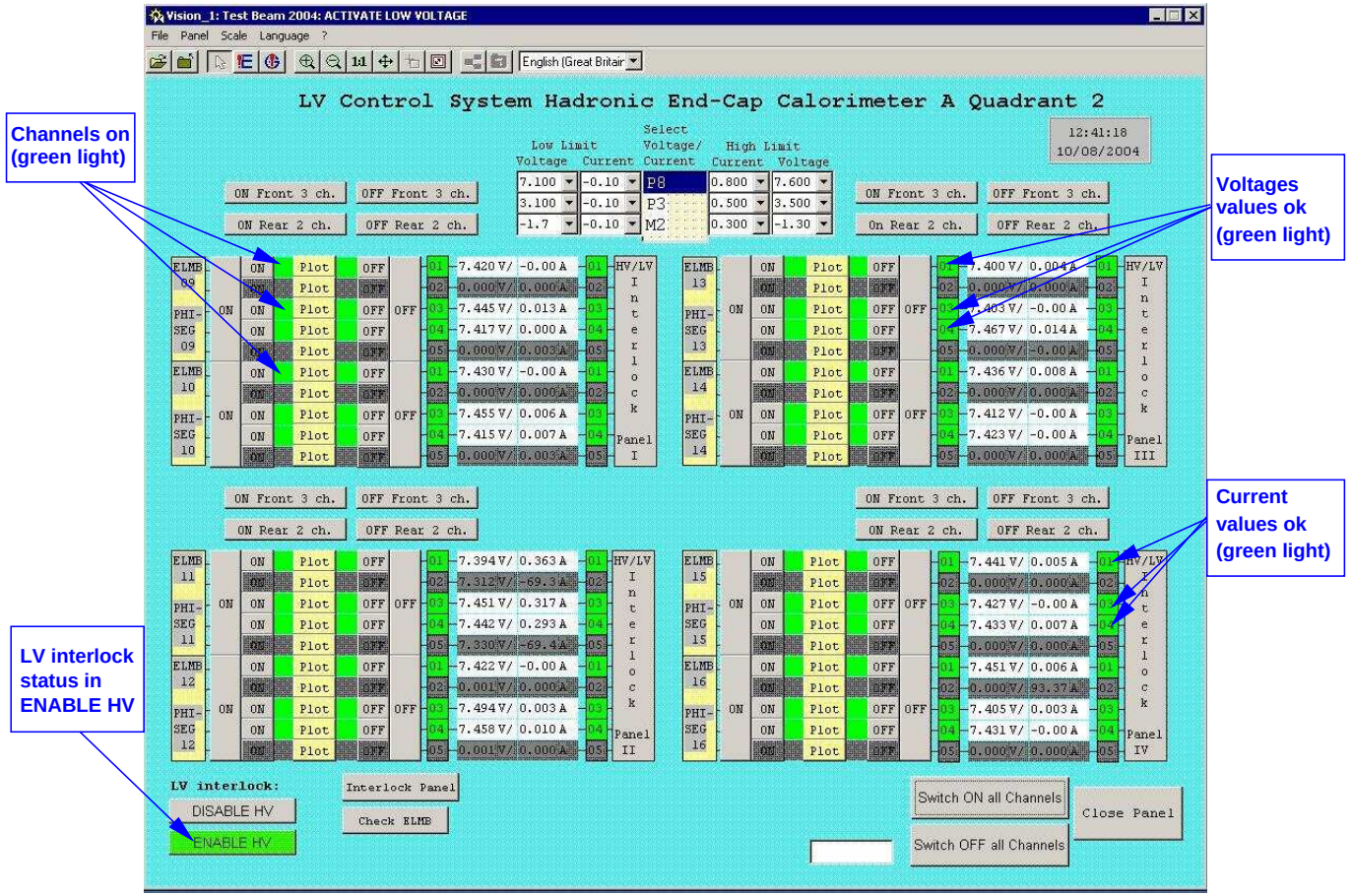
HEC LV Control System

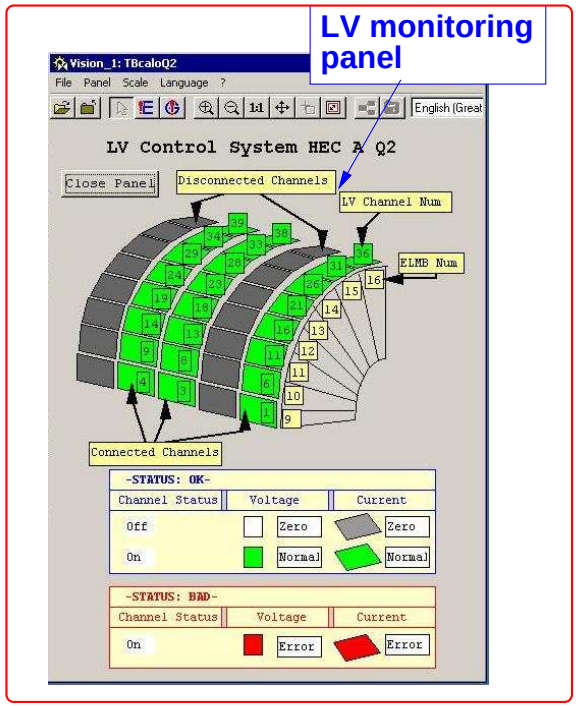
For the HEC LV Control System in PVSS we will need:

- A total of 64 + 8 ELMBs (for temperature measurements)
- A total of 8 CANBus Lines and 2 Kvaser cards
  - CANBus Port 0: ELMB_1 . . . ELMB_8 + ELMBMON_1 - HEC C Quad. 1
  - CANBus Port 1: ELMB_9 . . . ELMB_16 + ELMBMON_2 - HEC C Quad. 2
  - CANBus Port 2: ELMB_17 . . . ELMB_24 + ELMBMON_3 - HEC C Quad. 3
  - CANBus Port 3: ELMB_25 . . . ELMB_32 + ELMBMON_4 - HEC C Quad. 4
  - CANBus Port 4: ELMB_33 . . . ELMB_40 + ELMBMON_5 - HEC A Quad. 1
  - CANBus Port 5: ELMB_40 . . . ELMB_48 + ELMBMON_6 - HEC A Quad. 2
  - CANBus Port 6: ELMB_49 . . . ELMB_56 + ELMBMON_7 - HEC A Quad. 3
  - CANBus Port 7: ELMB_57 . . . ELMB_64 + ELMBMON_8 - HEC A Quad. 4

Main HEC LV panels

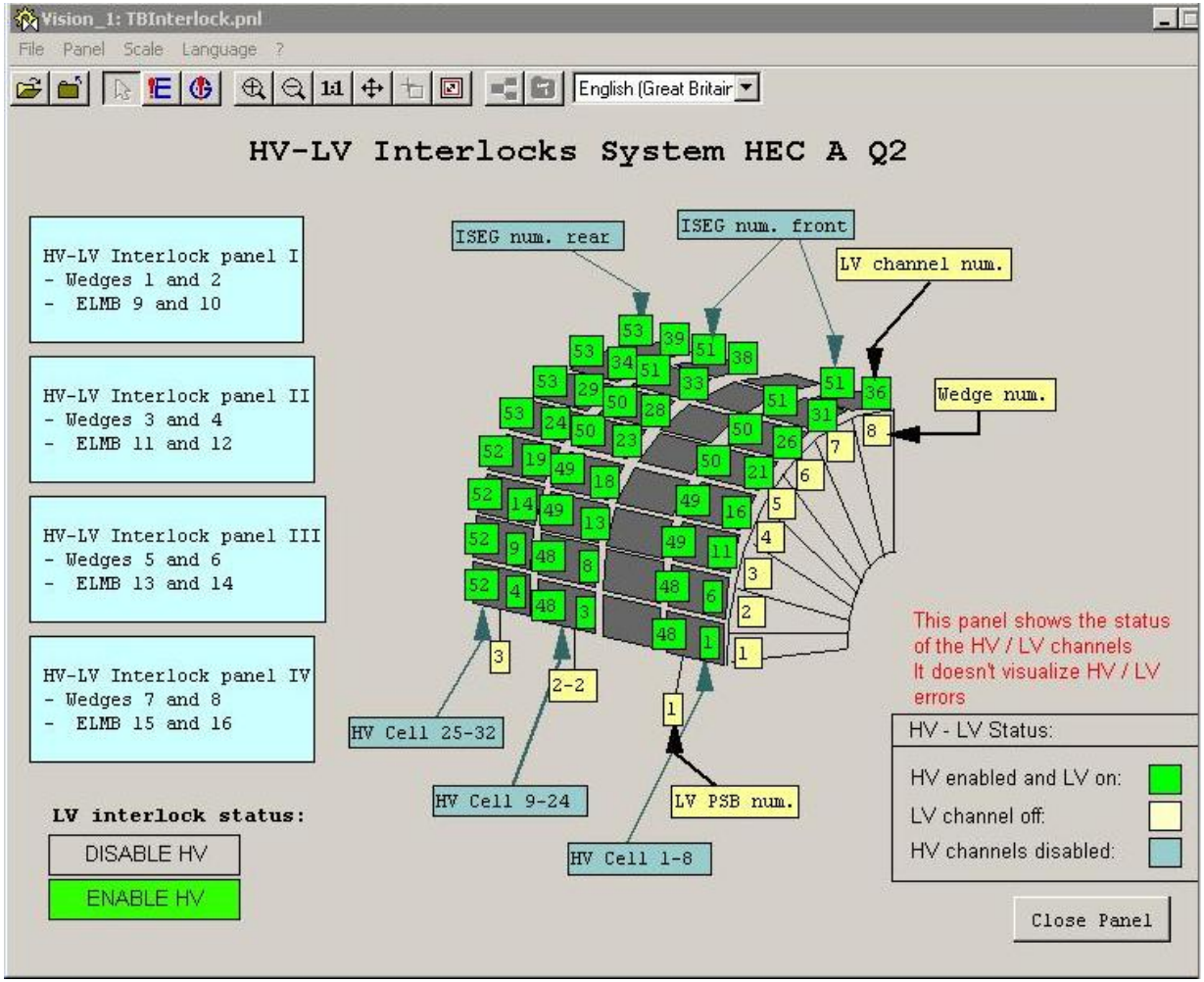
- "LV action panel" and "LV monitoring panel" used during the 2004 testbeam to be rebuild for the cold test





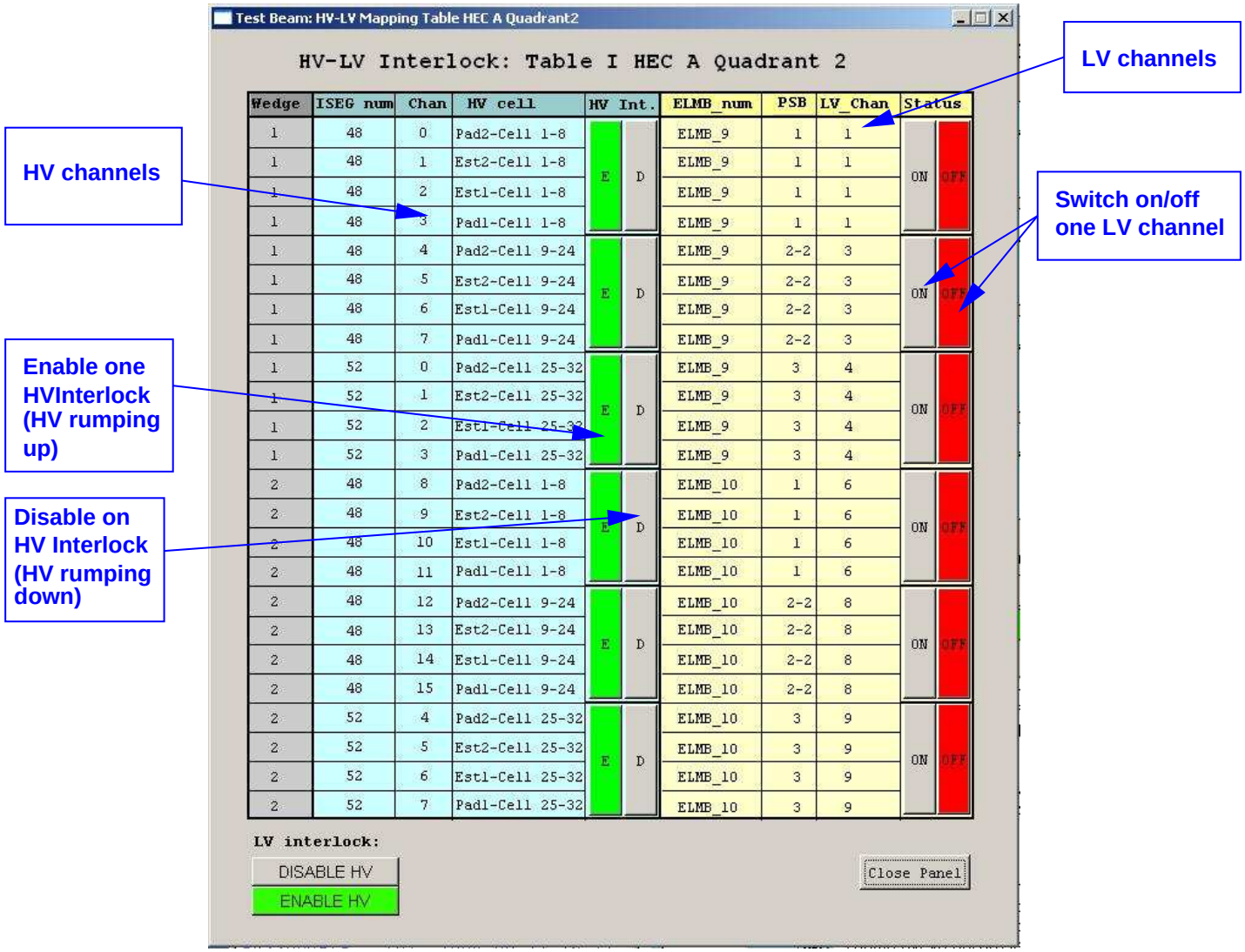
Main HV-LV Interlock panel

- The main HV-LV interlock panel monitor the status of the HV interlocks (enabled/disabled) and the LV channels (on/off)



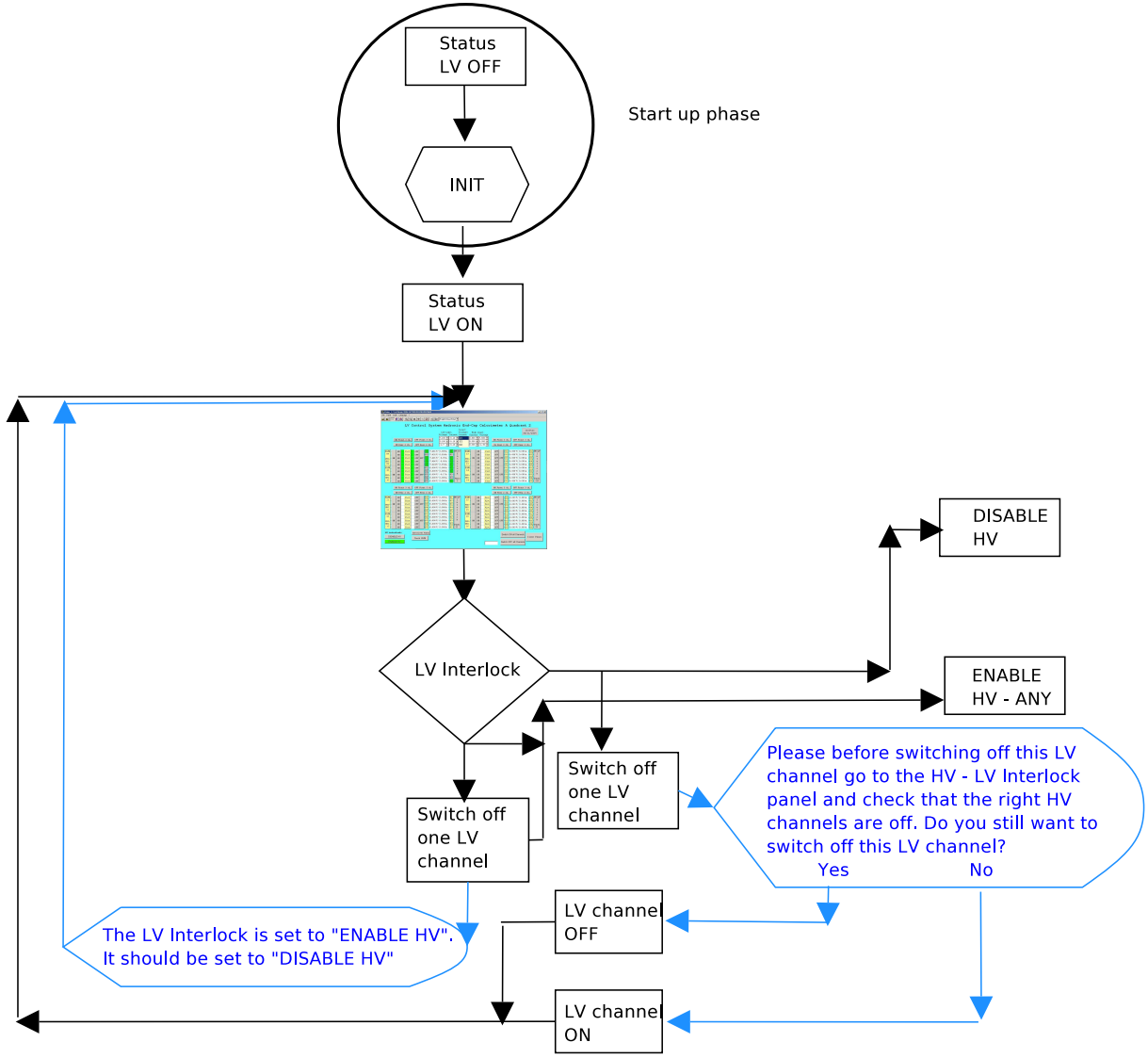
One HV-LV mapping table

- This is how a mapping table for the HV-LV interlock system looks like



Wedge	ISEG num	Chan	HV cell	HV Int.	ELMB_num	PSB	LV_Chan	Status
1	48	0	Pad2-Cell 1-8	E D	ELMB_9	1	1	ON OFF
1	48	1	Est2-Cell 1-8		ELMB_9	1	1	
1	48	2	Est1-Cell 1-8		ELMB_9	1	1	
1	48	3	Pad1-Cell 1-8		ELMB_9	1	1	
1	48	4	Pad2-Cell 9-24	E D	ELMB_9	2-2	3	ON OFF
1	48	5	Est2-Cell 9-24		ELMB_9	2-2	3	
1	48	6	Est1-Cell 9-24		ELMB_9	2-2	3	
1	48	7	Pad1-Cell 9-24		ELMB_9	2-2	3	
1	52	0	Pad2-Cell 25-32	E D	ELMB_9	3	4	ON OFF
1	52	1	Est2-Cell 25-32		ELMB_9	3	4	
1	52	2	Est1-Cell 25-32		ELMB_9	3	4	
1	52	3	Pad1-Cell 25-32		ELMB_9	3	4	
2	48	8	Pad2-Cell 1-8	E D	ELMB_10	1	6	ON OFF
2	48	9	Est2-Cell 1-8		ELMB_10	1	6	
2	48	10	Est1-Cell 1-8		ELMB_10	1	6	
2	48	11	Pad1-Cell 1-8		ELMB_10	1	6	
2	48	12	Pad2-Cell 9-24	E D	ELMB_10	2-2	8	ON OFF
2	48	13	Est2-Cell 9-24		ELMB_10	2-2	8	
2	48	14	Est1-Cell 9-24		ELMB_10	2-2	8	
2	48	15	Pad1-Cell 9-24		ELMB_10	2-2	8	
2	52	4	Pad2-Cell 25-32	E D	ELMB_10	3	9	ON OFF
2	52	5	Est2-Cell 25-32		ELMB_10	3	9	
2	52	6	Est1-Cell 25-32		ELMB_10	3	9	
2	52	7	Pad1-Cell 25-32		ELMB_10	3	9	

HV - LV Interlock logic from the LV action panel



HV - LV Interlock logic from the Interlock panel