

HEC HV - LV Interlock System

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MPI Meeting

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- ▶ Introduction
- ▶ JCOP and ELMB Framework and New HEC Panels
- ▶ HV - LV Interlock System



Introduction

- ▶ Work is going on to rebuild the final HEC LV Control System in PVSS to comply the JCOP and ELMB Framework
- ▶ A first version of this software will be used at the cold test in February 2005
 - The main idea is to rebuild all the main PVSS panels used during the HEC-EMEC-FCAL test-beam in 2004 into the new HEC LV Control System
- ▶ Work is also going on to build a final HEC HV - LV Interlock System
 - We want to avoid that any of the PSBs in the cryostat get damaged. To minimize this risk is required that the HV channels stay off if the LV channels are off.



HEC LV Control System

For the HEC LV Control System in PVSS we will need:

- ▶ A total of 64 + 8 ELMBs (for temperature measurements)
- ▶ A total of 8 CANBus Lines and 2 Kvaser cards
 - CANBus Port 0: ELMB_1 ... ELMB_8 + ELMBMON_1 - HEC C Quad. 1
 - CANBus Port 1: ELMB_9 ... ELMB_16 + ELMBMON_2 - HEC C Quad. 2
 - CANBus Port 2: ELMB_17 ... ELMB_24 + ELMBMON_3 - HEC C Quad. 3
 - CANBus Port 3: ELMB_25 ... ELMB_32 + ELMBMON_4 - HEC C Quad. 4
 - CANBus Port 4: ELMB_33 ... ELMB_40 + ELMBMON_5 - HEC A Quad. 1
 - CANBus Port 5: ELMB_40 ... ELMB_48 + ELMBMON_6 - HEC A Quad. 2
 - CANBus Port 6: ELMB_49 ... ELMB_56 + ELMBMON_7 - HEC A Quad. 3
 - CANBus Port 7: ELMB_57 ... ELMB_64 + ELMBMON_8 - HEC A Quad. 4



Main HEC LV panels

- ▶ “LV action panel” and “LV monitoring panel” used during the 2004 testbeam to be rebuild for the cold test

Channels on (green light)

LV interlock status in ENABLE HV

Voltages values ok (green light)

Current values ok (green light)

LV Control System Hadronic End-Cap Calorimeter A Quadrant 2

12:41:18
10/08/2004

Low Limit Voltage	Low Limit Current	Select	High Limit Voltage	High Limit Current
7.100	-0.10	P8	0.800	7.600
3.100	-0.10	P3	0.500	3.500
-1.7	-0.10	M2	0.300	-1.30

ELMB	PHI-SEG	ON	Plot	HV/LV	Voltage	Current
08	01	ON	Plot	OFF	7.420 V	-0.00 A
08	02	ON	Plot	OFF	0.000 V	0.000 A
08	03	ON	Plot	OFF	7.445 V	0.013 A
08	04	ON	Plot	OFF	7.417 V	0.000 A
08	05	ON	Plot	OFF	0.000 V	0.003 A
08	06	ON	Plot	OFF	7.430 V	-0.00 A
08	07	ON	Plot	OFF	0.000 V	0.000 A
08	08	ON	Plot	OFF	7.455 V	0.006 A
08	09	ON	Plot	OFF	7.415 V	0.007 A
08	10	ON	Plot	OFF	0.000 V	0.003 A

LV interlock: DISABLE HV, ENABLE HV

Switch ON all Channels, Switch OFF all Channels, Close Panel

LV monitoring panel

LV Control System HEC A Q2

Close Panel, Disconnected Channels, LV Channel Num, ELMB Num

Connected Channels

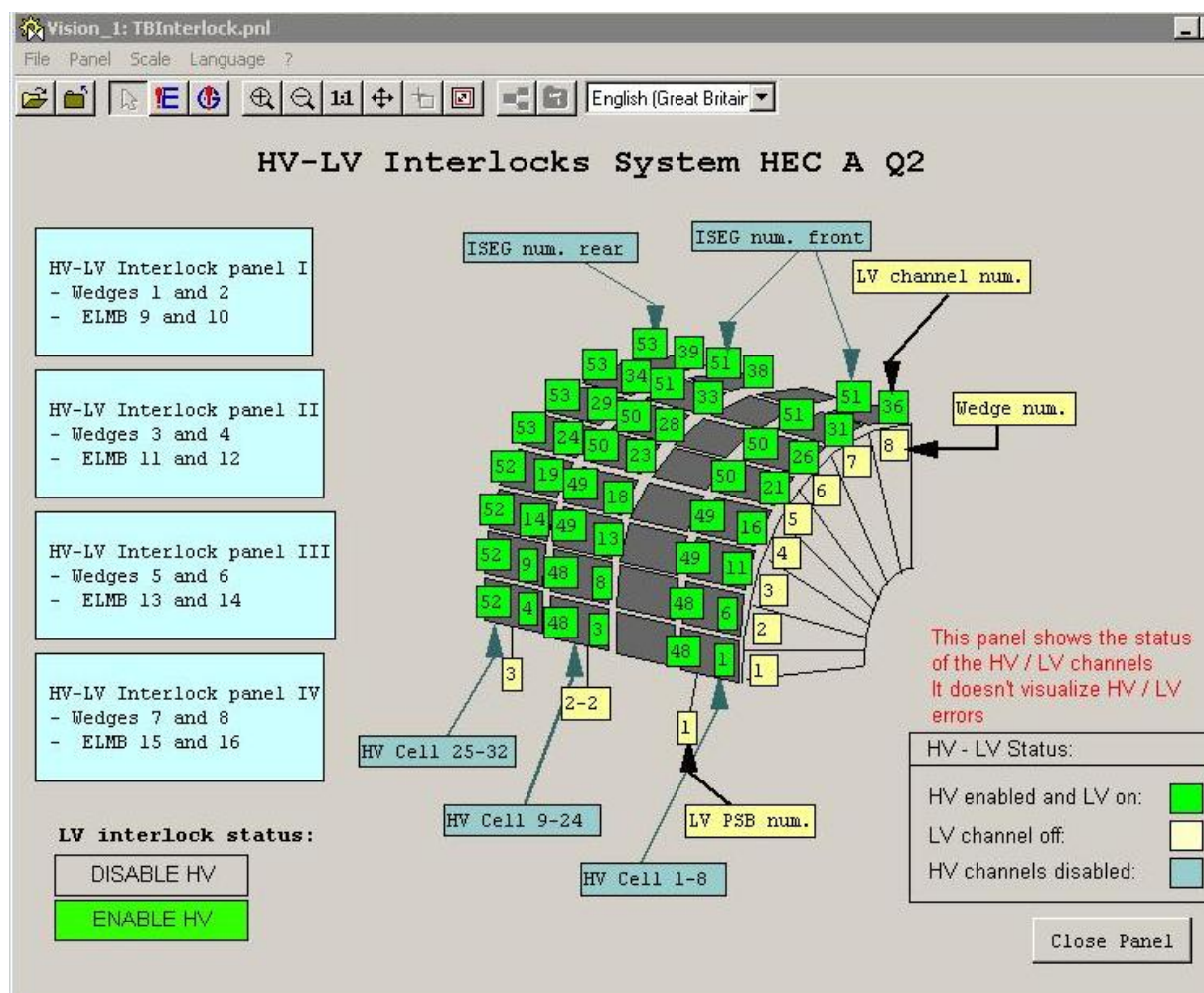
-STATUS: OK-
Channel Status: Off (Zero), On (Normal)

-STATUS: BAD-
Channel Status: On (Error)



Main HV-LV Interlock panel

- ▶ The main HV-LV interlock panel monitor the status of the HV interlocks (enabled/disabled) and the LV channels (on/off)



One HV-LV mapping table

- ▶ This is how a mapping table for the HV-LV interlock system looks like

Test Beam: HV-LV Mapping Table HEC A Quadrant 2

HV-LV Interlock: Table I HEC A Quadrant 2

Wedge	ISEG num	Chan	HV cell	HV Int.	ELMB_num	PSB	LV Chan	Status
1	48	0	Pad2-Cell 1-8	E D	ELMB_9	1	1	ON OFF
1	48	1	Est2-Cell 1-8					
1	48	2	Est1-Cell 1-8					
1	48	3	Pad1-Cell 1-8					
1	48	4	Pad2-Cell 9-24	E D	ELMB_9	2-2	3	ON OFF
1	48	5	Est2-Cell 9-24					
1	48	6	Est1-Cell 9-24					
1	48	7	Pad1-Cell 9-24					
1	52	0	Pad2-Cell 25-32	E D	ELMB_9	3	4	ON OFF
1	52	1	Est2-Cell 25-32					
1	52	2	Est1-Cell 25-32					
1	52	3	Pad1-Cell 25-32					
2	48	8	Pad2-Cell 1-8	E D	ELMB_10	1	6	ON OFF
2	48	9	Est2-Cell 1-8					
2	48	10	Est1-Cell 1-8					
2	48	11	Pad1-Cell 1-8					
2	48	12	Pad2-Cell 9-24	E D	ELMB_10	2-2	8	ON OFF
2	48	13	Est2-Cell 9-24					
2	48	14	Est1-Cell 9-24					
2	48	15	Pad1-Cell 9-24					
2	52	4	Pad2-Cell 25-32	E D	ELMB_10	3	9	ON OFF
2	52	5	Est2-Cell 25-32					
2	52	6	Est1-Cell 25-32					
2	52	7	Pad1-Cell 25-32					

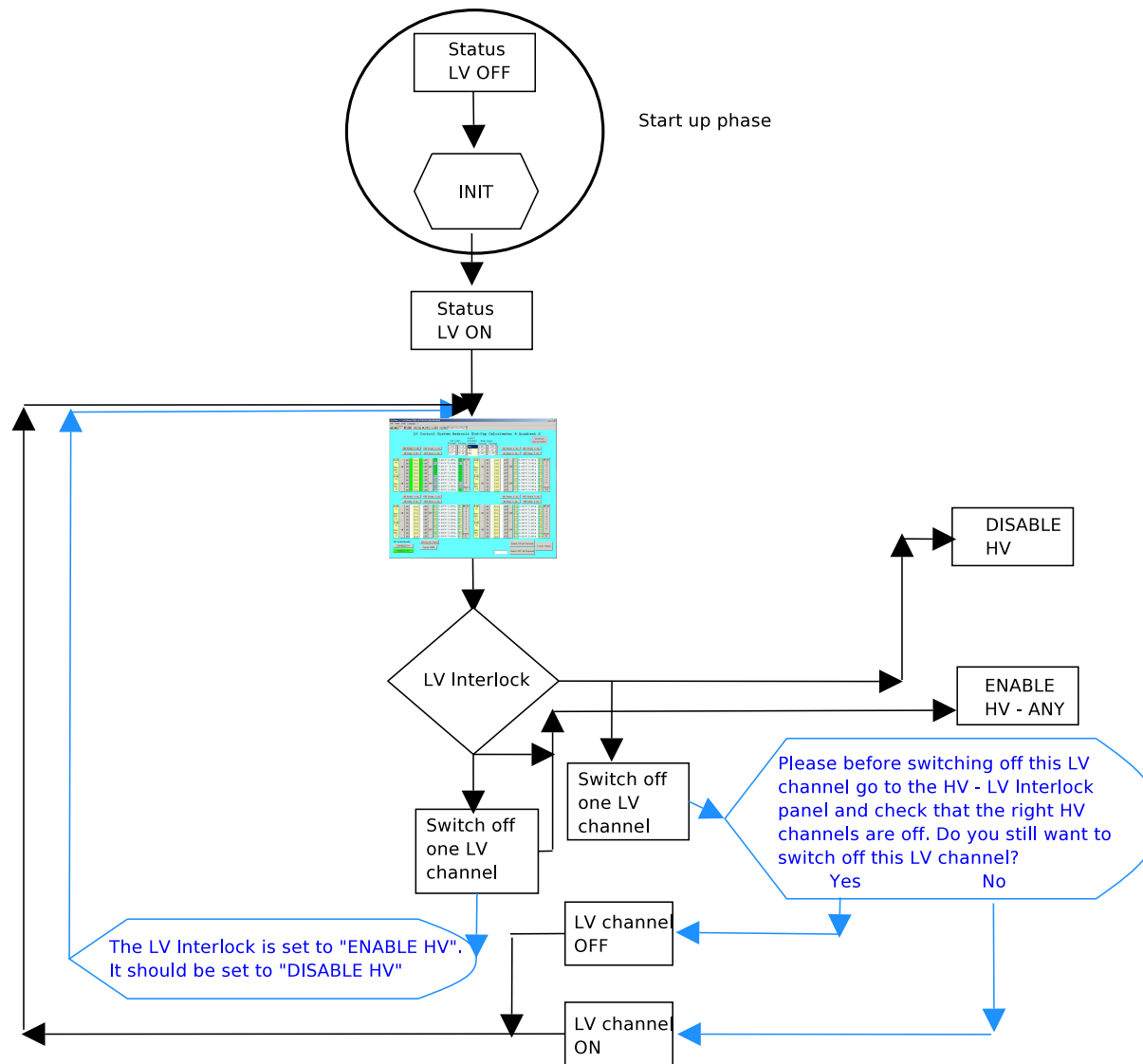
LV interlock:

Annotations:

- HV channels (points to ISEG num column)
- LV channels (points to LV Chan column)
- Switch on/off one LV channel (points to Status column)
- Enable one HV Interlock (HV rumping up) (points to HV Int. column)
- Disable on HV Interlock (HV rumping down) (points to HV Int. column)



HV - LV Interlock logic from the LV action panel



HV - LV Interlock logic from the Interlock panel

