DCD2 DEPFET matrix measurements

Belle II PXD/DEPFET Meeting

Prague 01/2010

Manuel Koch

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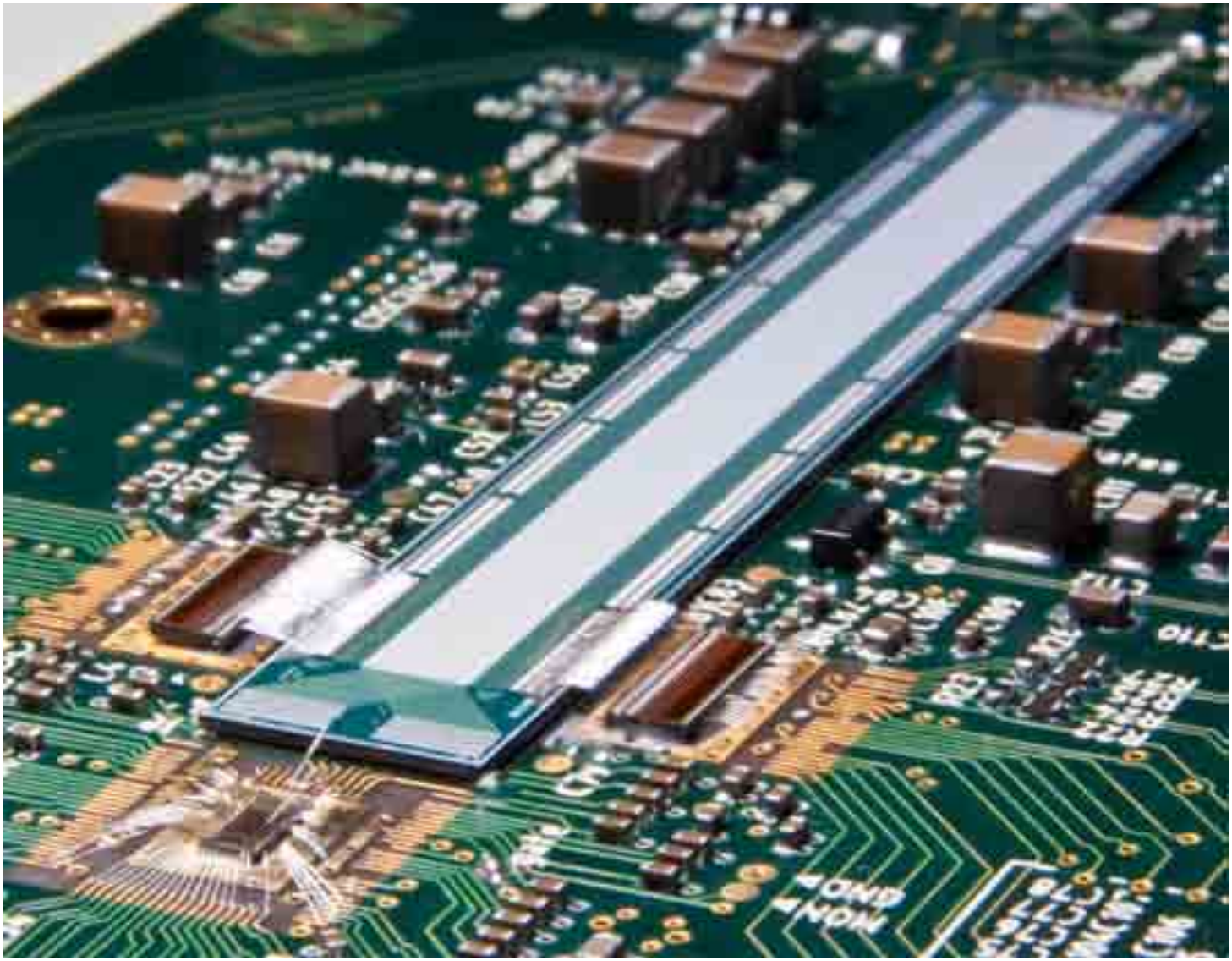
COCG SA, long



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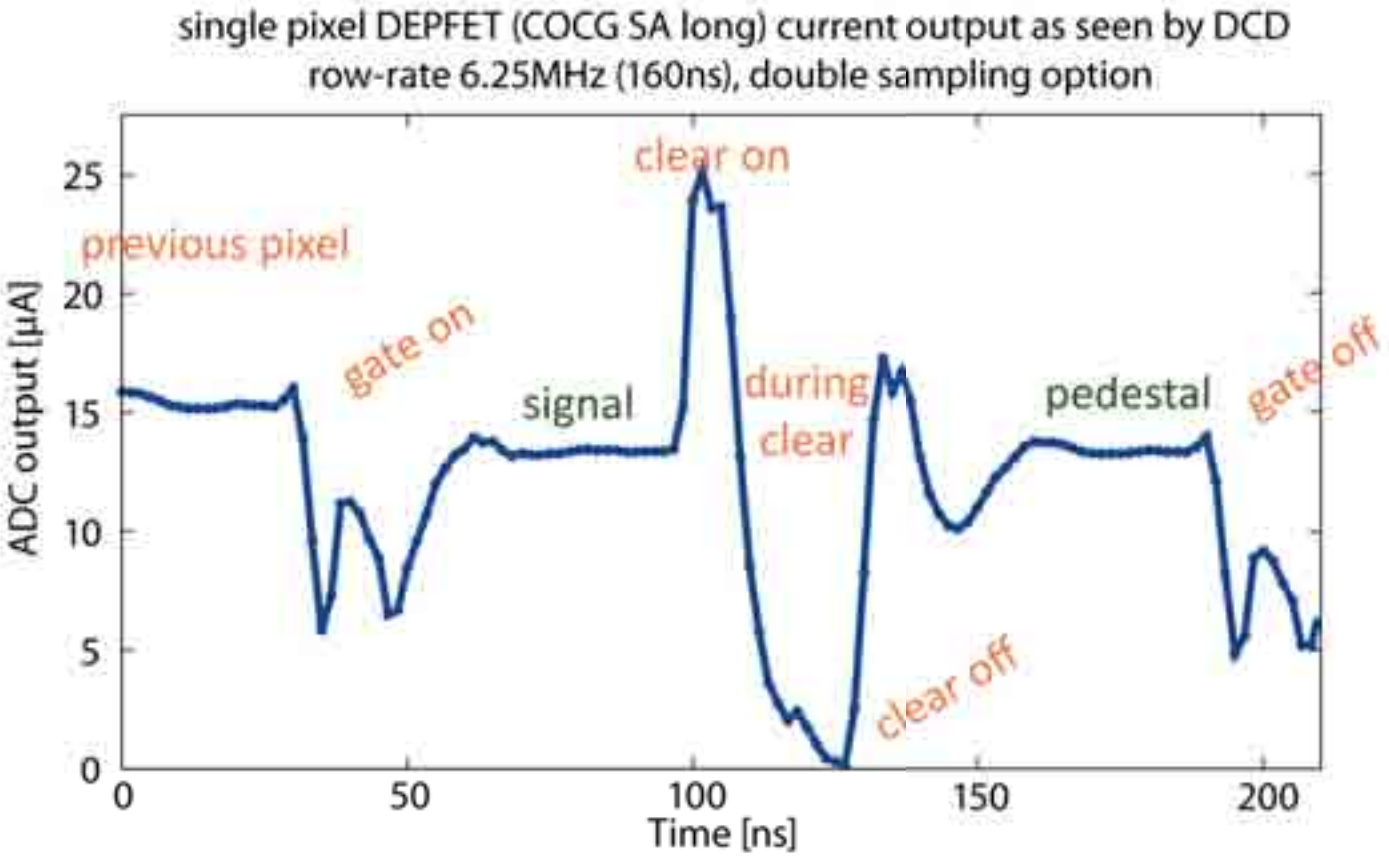
Long matrix COCG SA , slow 160ns



- Noticeable differences to small COCG LE:
  - Longer RC (as expected)
  - Double dip switching from row to row
  - Additional dip after ‘clear off’

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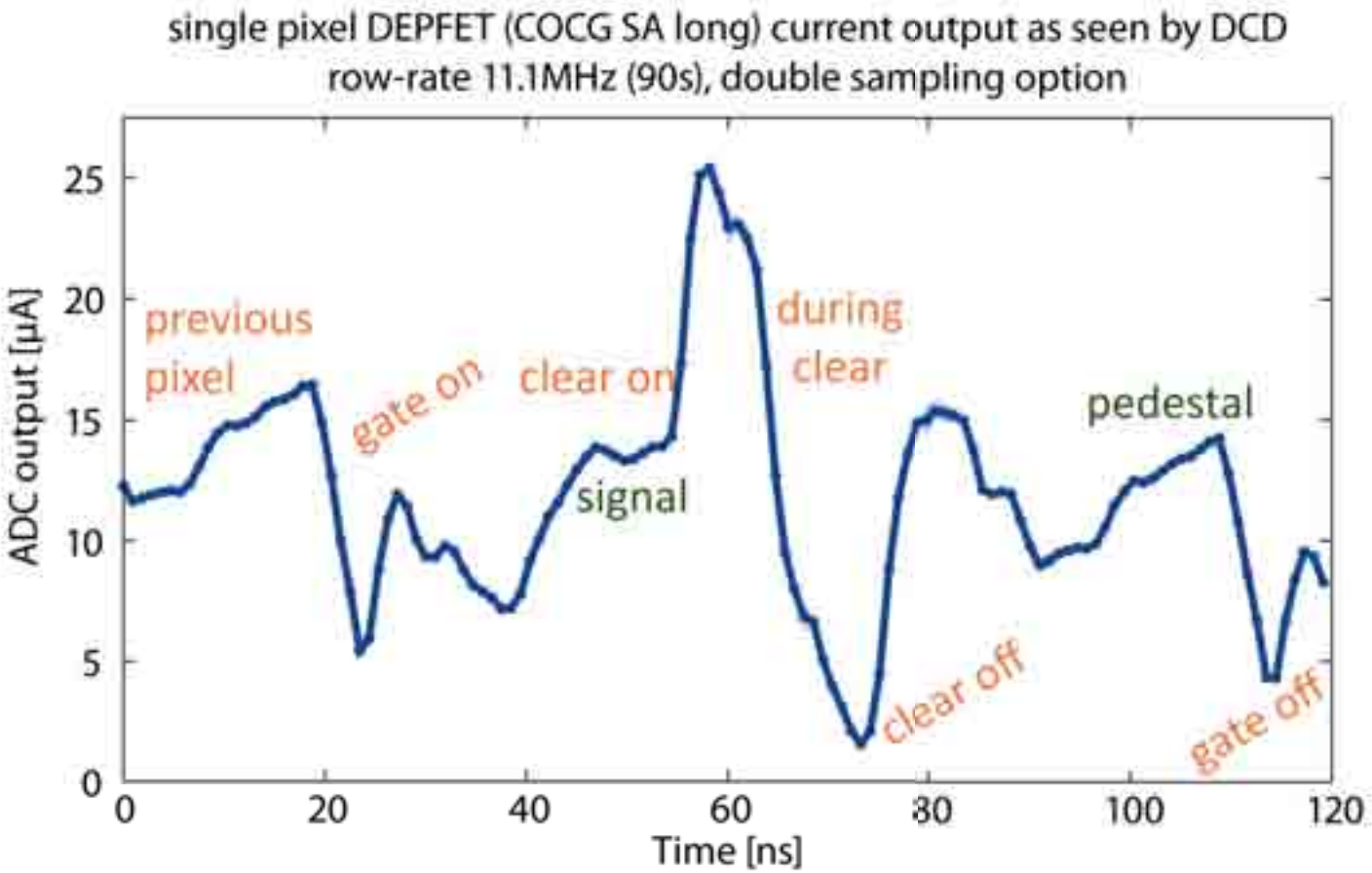
Long matrix COCG SA , fast 90ns, double sampling



- double sampling no longer possible at target speed
- However: precise gate switching and understanding of post-clear-dip might improve that picture

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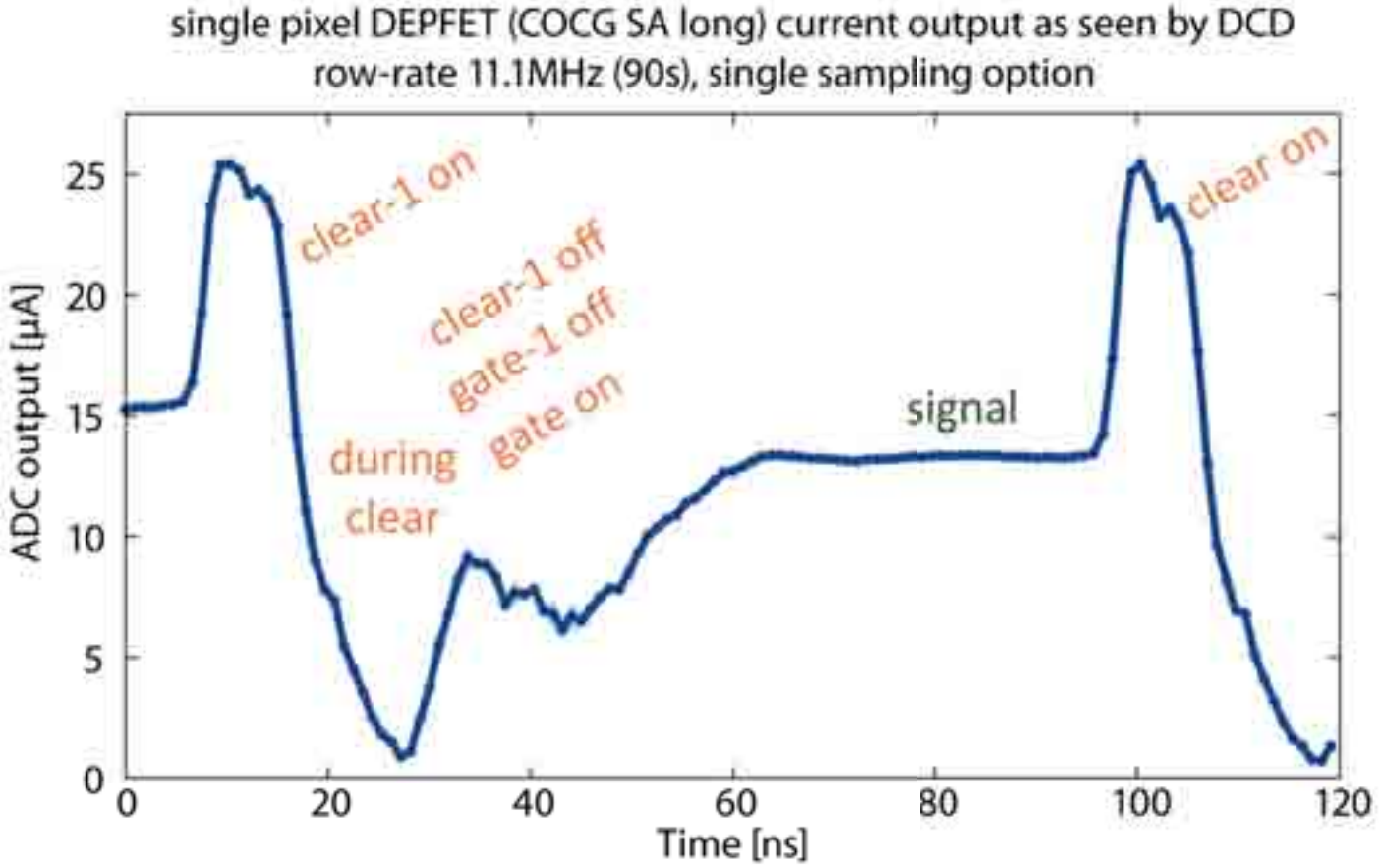
Long matrix COCG SA , fast 90ns, single sampling



- single sampling mode
- enough safety margin for settling times
- allows >20ns complete clear

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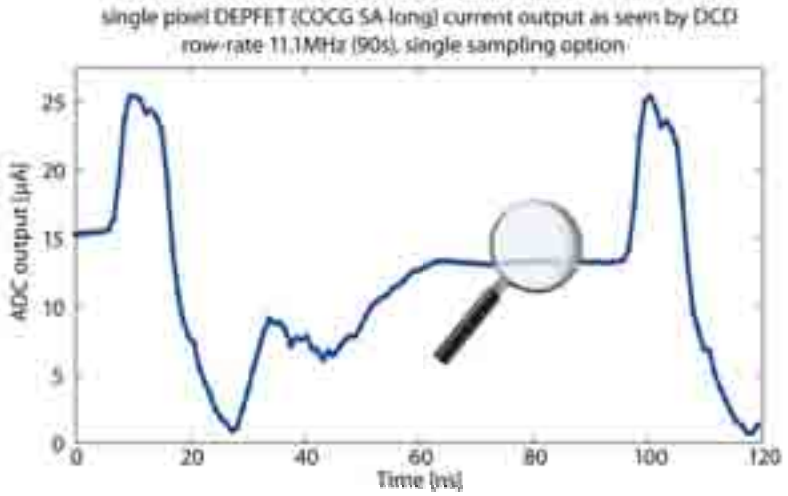
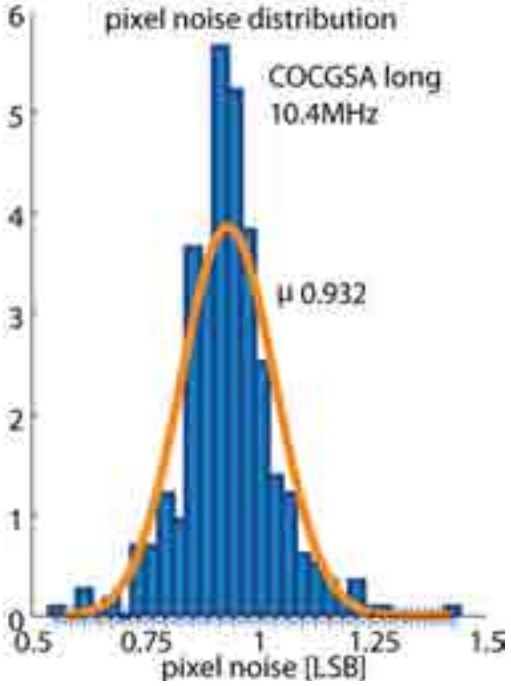
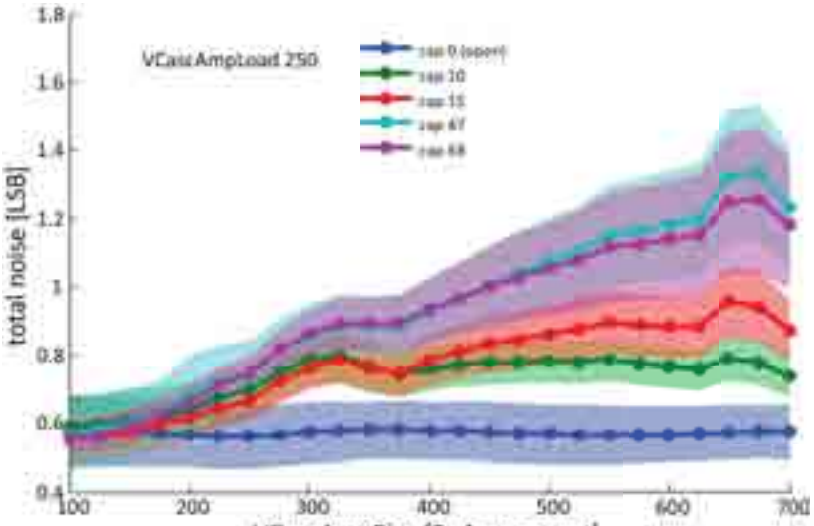
Long matrix COCG SA, pixel noise distribution





- statistics for 384 pixels
- 5000 samples each
- includes all common mode, pickup
- mean noise ~0.9LSB @10.4MHz (96ns)
- Low bias of input stage possible
- noise is lower than expected from measurements with directly bonded capacitance
  → we have RC-line



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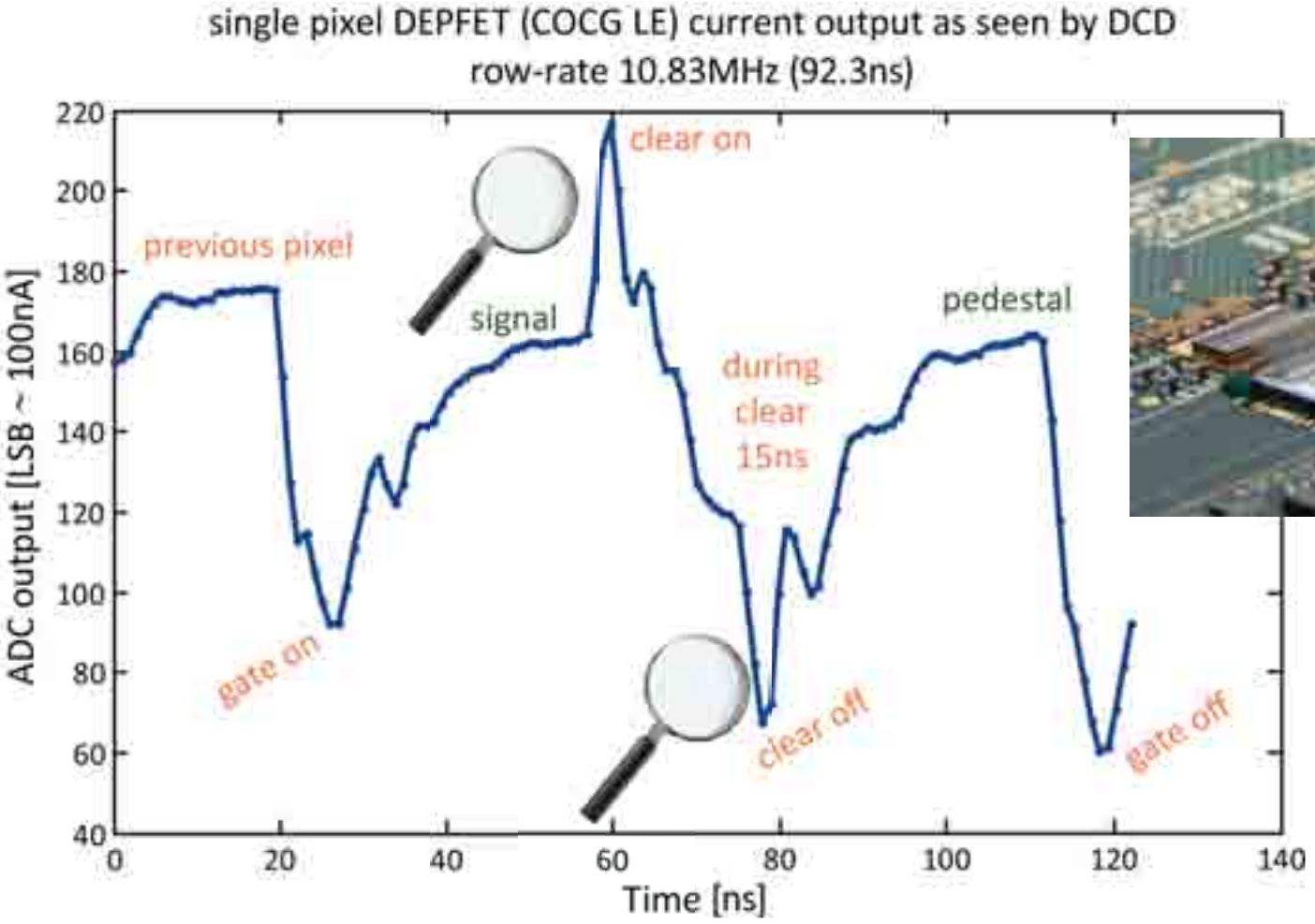
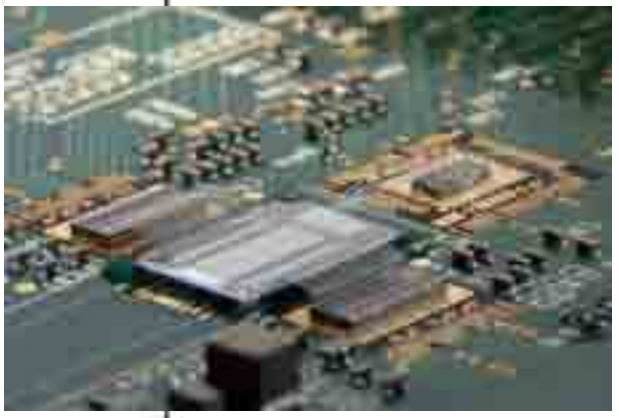
Time resolved DEPFET output current (COCG LE, small matrix)





- detailed look at spikes during clear switching
- suspect coupling capacitance between clear and drain
- → improve simulation model and understanding

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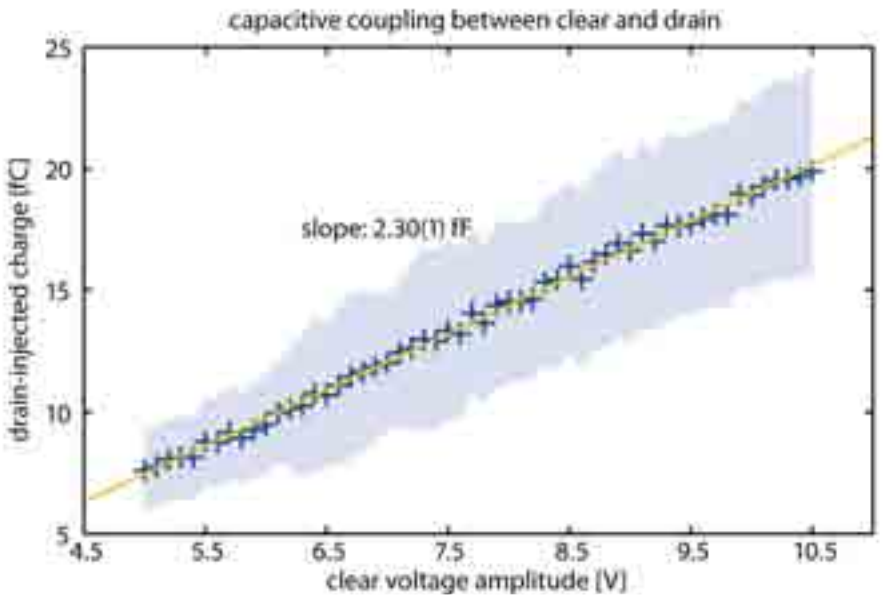
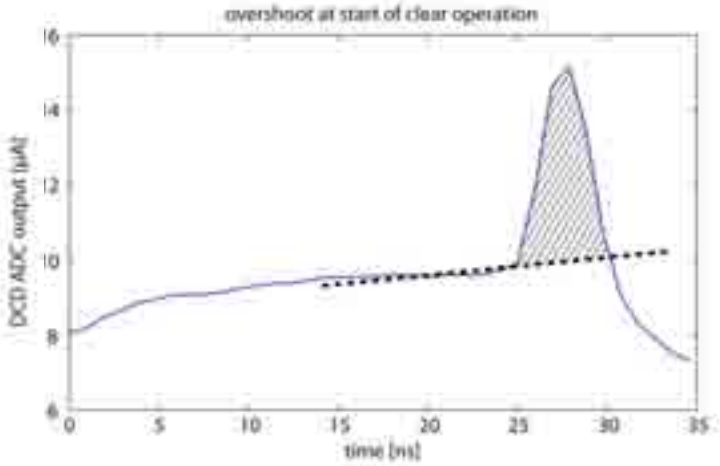
capacitive charge injection (Clear, COCG LE)

- Integrate current/time pulse shape → transferred charge
- vary clear voltage amplitude
- Clear linear relationship as result
- effect of drain capacitance is cancelled by regulated cascode
- → every charge injection is seen like a true signal
- Note: due to start of clear process the pulse is cut short; absolute values might not match





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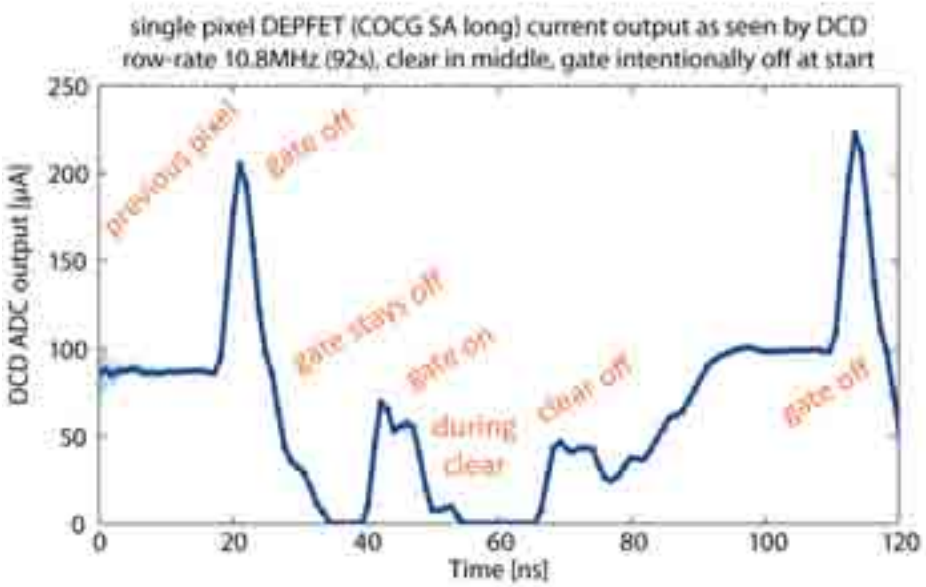
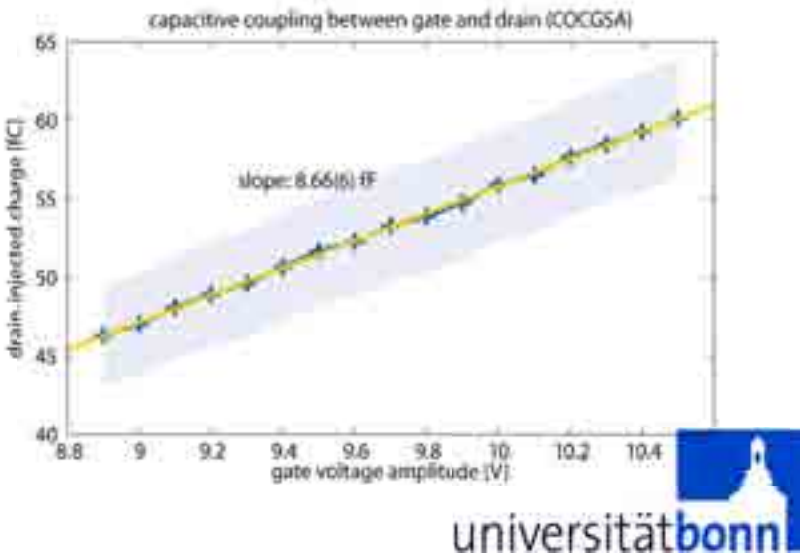
capacitive charge injection (Gate off, COCG SA long)

- Scenario: turn gate off for a short time when switching from row to row to separate problems (not a good operating mode)
- Notice capacitive charge injection spike now, measure linear relationship between charge and gate voltage amplitude
- Switching from row N-1 to row N:
  - 1.) gate N-1 off (inject +charge)
  - 2.) transistor N-1 turns off (current goes down)
  - 3.) gate N on (inject –charge)
  - 4.) transistor N turns on (current goes up)
- Charge injection should cancel each other out; unless you have a delay, or switch off row N-1 <u>after</u> you switch on row N! (as proposed for new switcher)





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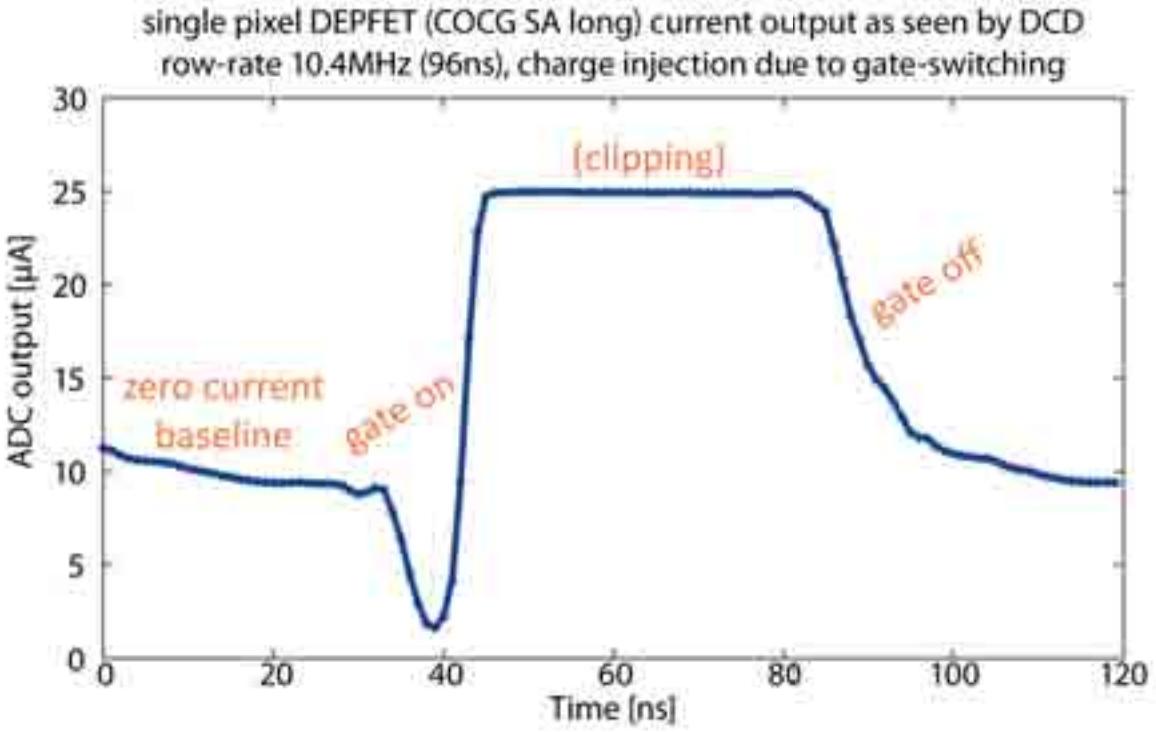
capacitive charge injection (Gate on, COCG SA long)

- injection during gate-on also exists
- difficult to observe: it is a negative spike on a zero current baseline
- bias DCD2 with extra input current
- Note: gate switching charge injection should cancel each other out as long as switching happens at the same time
  (rethink, simulate overlapped switching)



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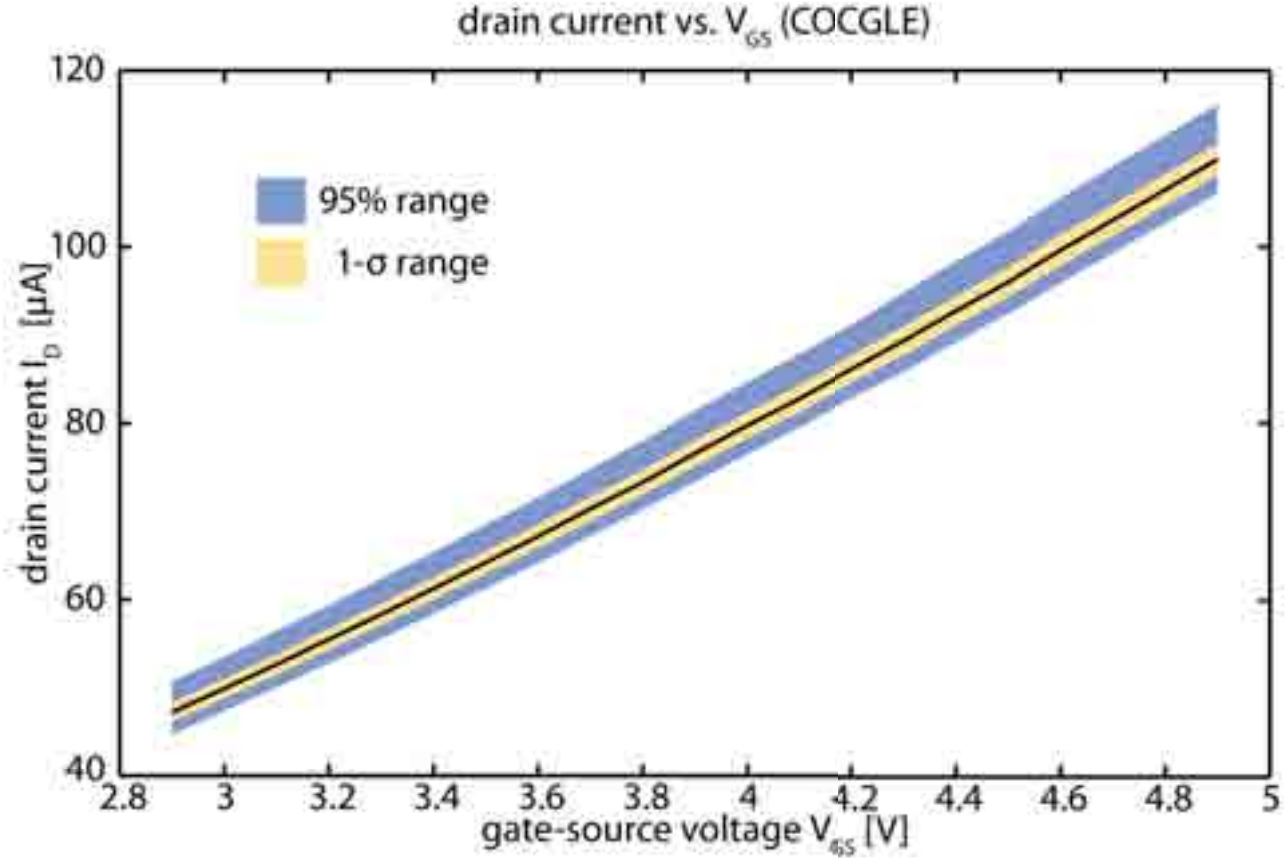
Pedestal current spread (COCG L E)



- Single sample with no input signal
- Statistics for 1200 pixels, 1k samples each
- Vary V-gate-source; piecewise calibration of DCD with Keithley24xx

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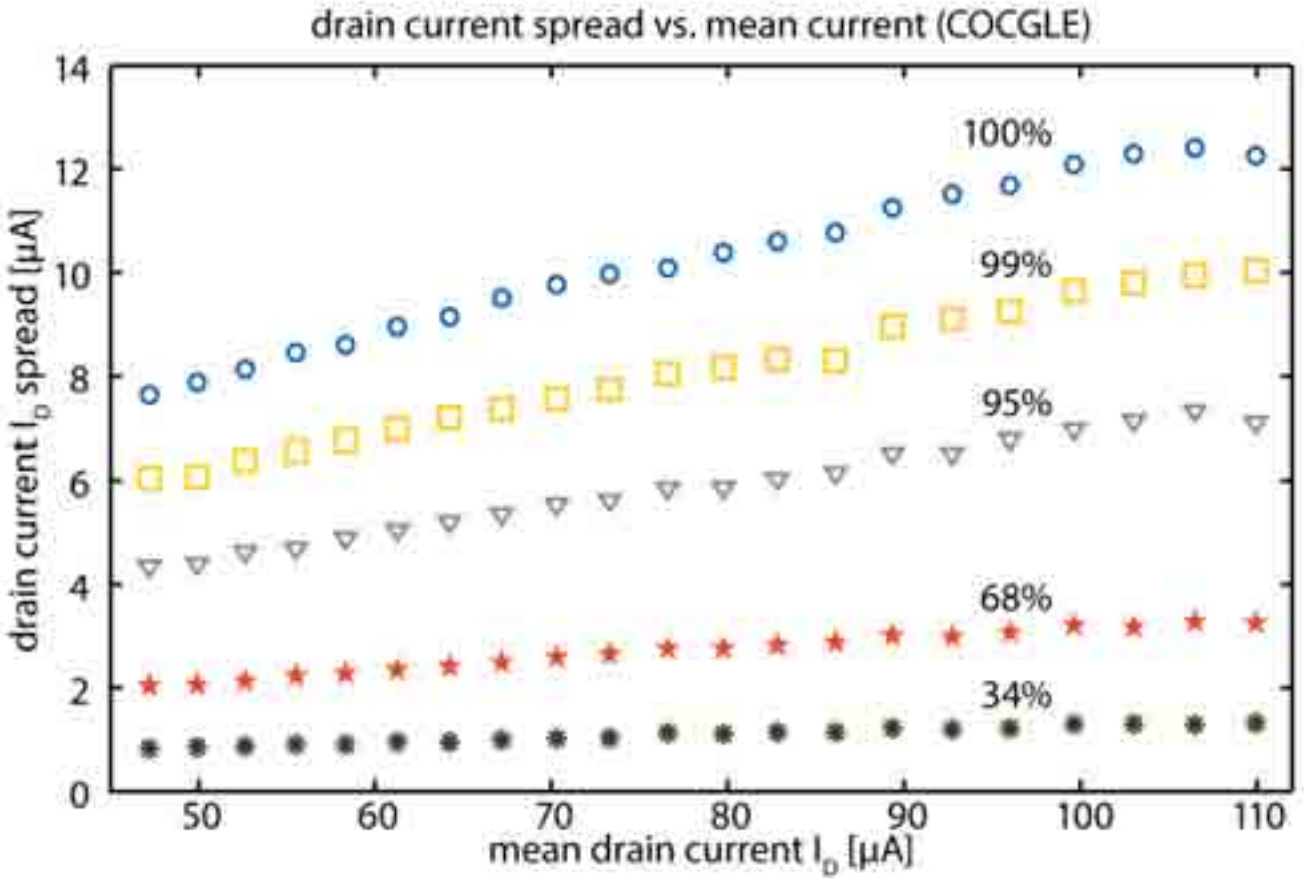
Pedestal current spread (COCG L E)



- Plotted are %-inclusion ranges with respect to mean value

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THANK YOU!

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