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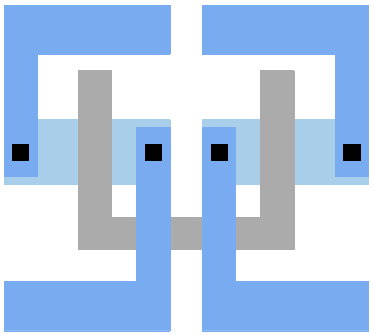
DEPFET System Simulation



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BELLE II PXD / DEPFET Meeting

Prague

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Agenda

- Motivation
- DEPFET System Simulation Environment
- Simulation Examples
- Open Issues

Motivation

Why do we need a DEPFET System Level Simulation?

The DEPFET PXD front-end electronics consist of:

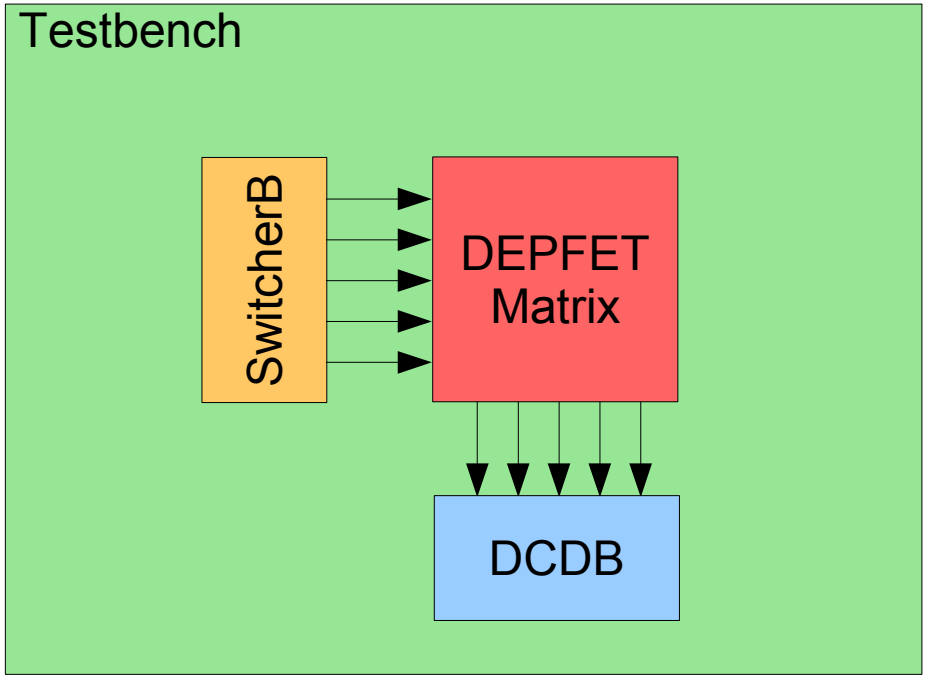
- DEPFET Matrix (HLL Munich)
- SwitcherB (Uni Heidelberg)
- DCDB (Uni Heidelberg)
- DHP (Uni Bonn)
- DHH (Uni Göttingen)

Each chip is designed and tested separately.
Do they work together?

A Simulation can give the answer!

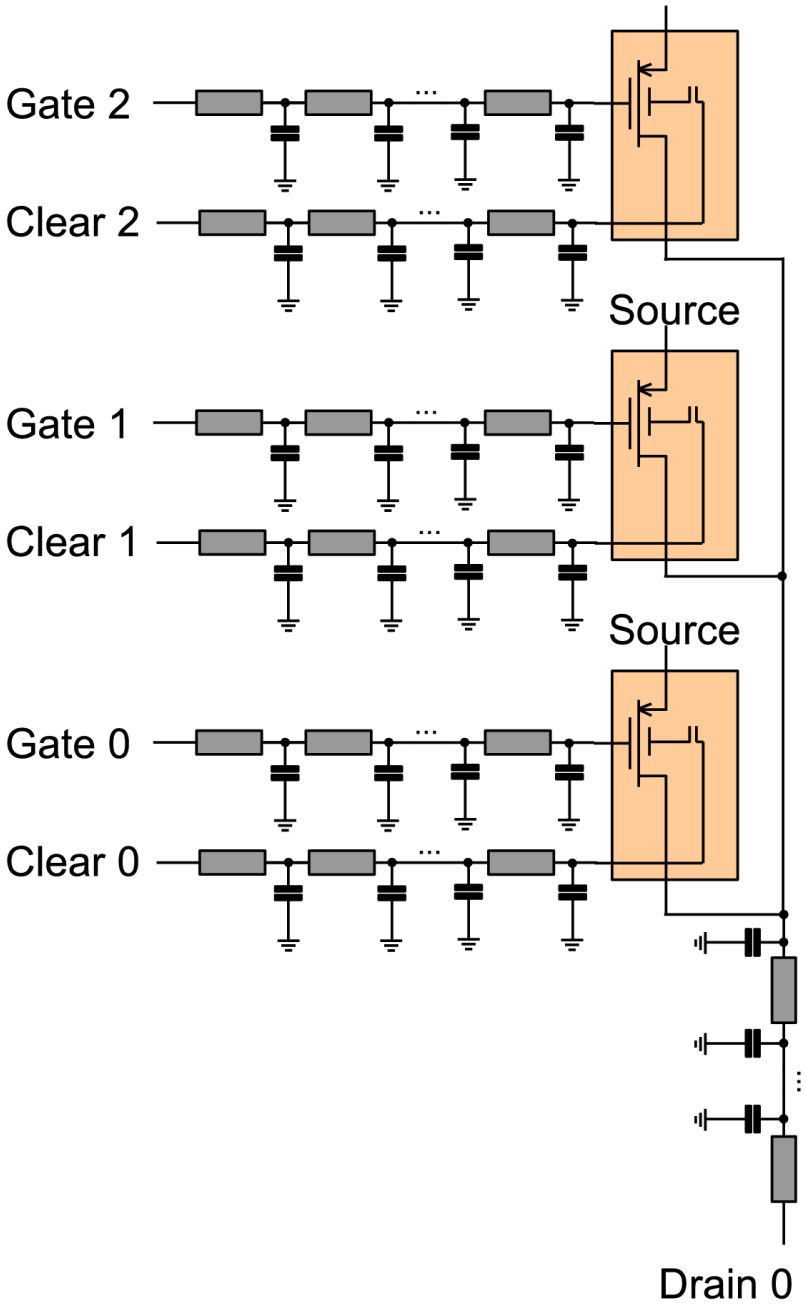
DEPFET System Simulation Environment

Simulation Environment: Overview



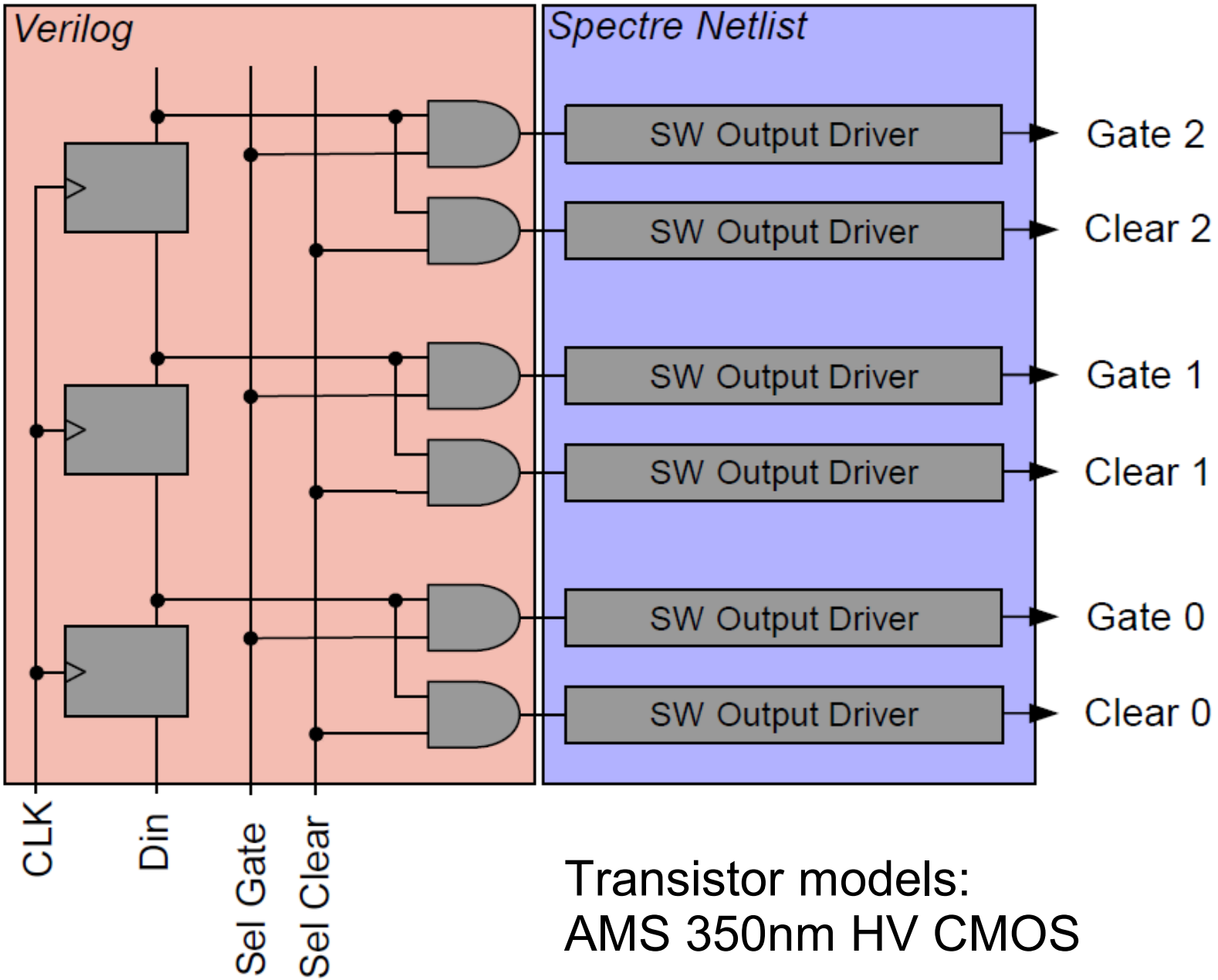
- The Simulation includes Models of the SwitcherB, the DCDB and the DEPFET Matrix.
- The Testbench stimulates the SwitcherB and the DCD
- The SwitcherB steers the DEPFET Matrix
- The DCDB reads the DEPFET Matrix

Simulation Details: The DEPFET Model



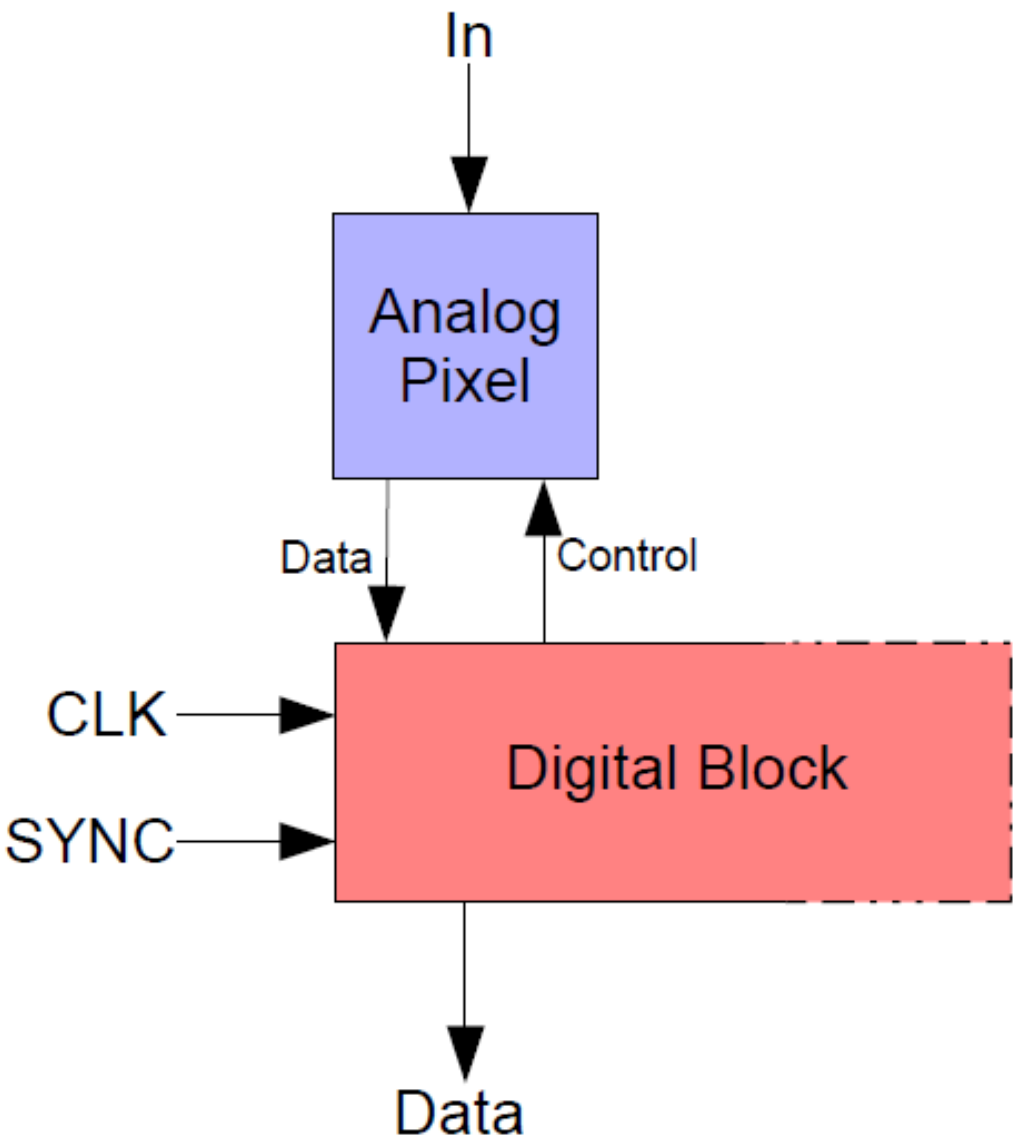
- 3 Pixel Matrix
  (3 Rows, 1 Column)
- RC lines for gate, clear and drain wires
  - Gate: ΣR 40Ω, ΣC 50pF
  - Clear: ΣR 40Ω, ΣC 50pF
  - Drain: ΣR 300Ω, ΣC 50pF
- Matrix Model: Spectre Netlist
- Transistor Model: SpectreCMI
  (Ref.: A. Wassatsch, Ringberg, May 2009)

Simulation Details: The SwitcherB Model



Transistor models:
AMS 350nm HV CMOS

Simulation Details: The DCDB Model



- Included Blocks
  - Single instance of DCDB's analog ADC pixel (Spectre Netlist)
  - Entire digital block (Verilog)
- Transistor Models: UMC CMOS 180nm

Simulation Details: Summary

- The simulation environment consists of
  - Verilog files (DCDB digital block, stimulus generator,...)
  - VerilogAMS files (Testbench,...)
  - Spectre netlist files (DCDB analog pixel, SwitcherB output driver)
  - UMC 180nm 1P6M MM/RFCMOS transistor models (DCDB analog pixel)
  - AMS 350nm HV CMOS transistor models (SwitcherB output driver)
  - HLL DEPFET model, written in SpectreCMI
- Simulation Software: Cadence Incisive Unified Simulator 9.2
  - Analog simulator: Spectre
  - Digital simulator: NCSim

→ We are exhaustivly using cutting-edge simulation technology!

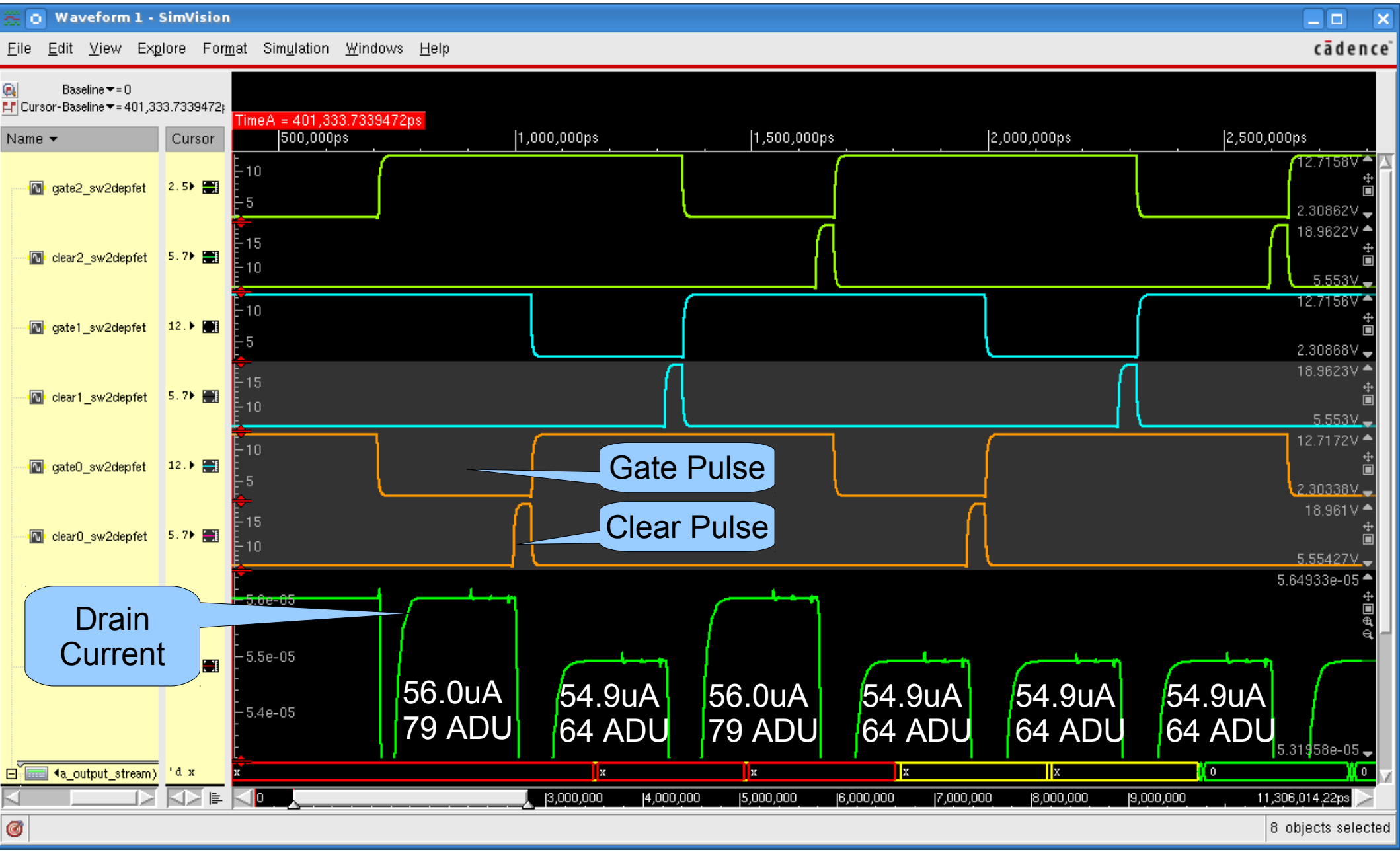
Simulation Examples

Simulation Example: Conditions

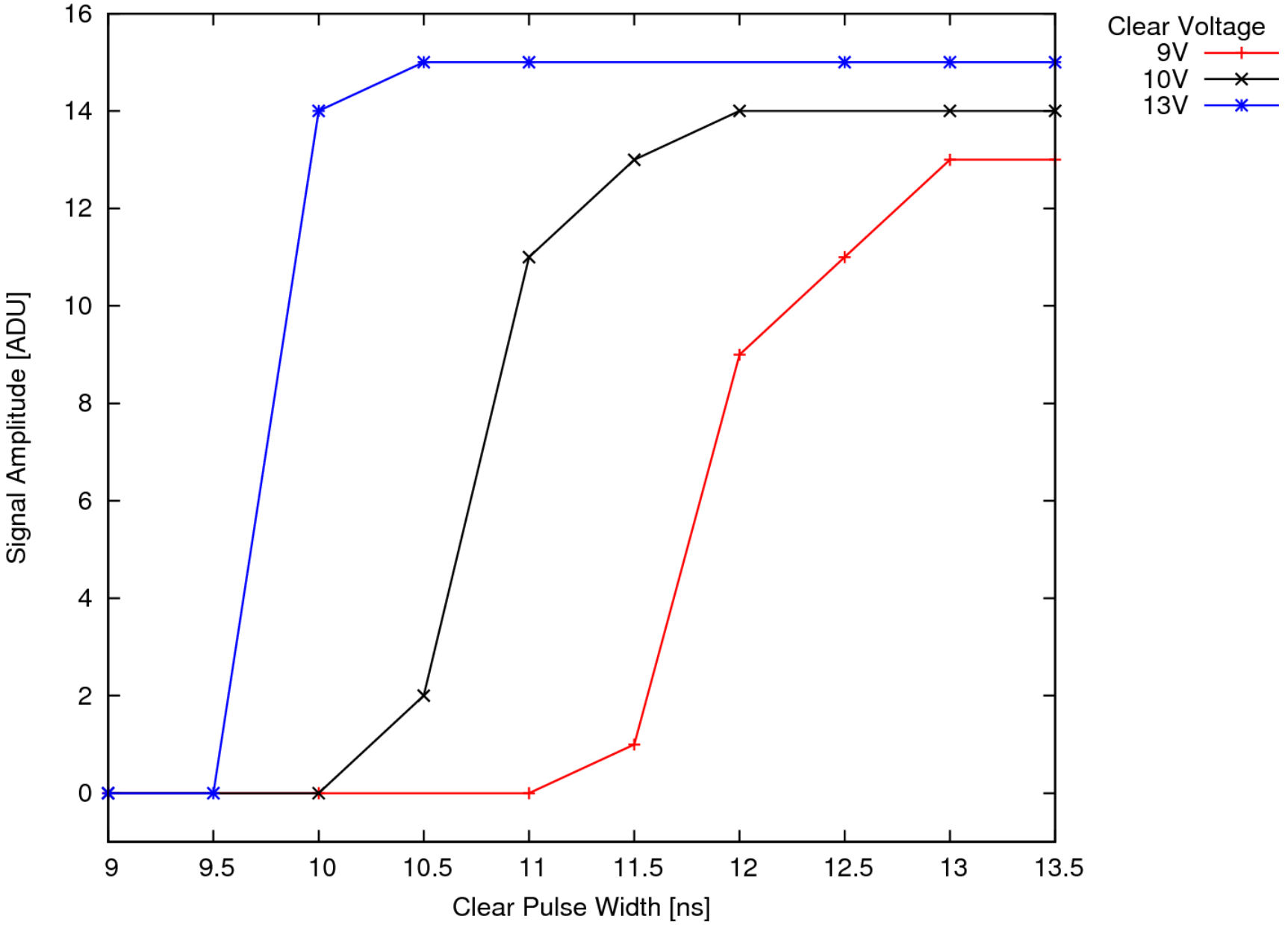
- Supply voltages
  - Matrix source: 5.74V (rel. to ground)
  - Clear voltages (rel. to matrix source potential)
    - Clear-Low: 0V
    - Clear-High: 13V
  - Gate voltages (rel. to matrix source potential)
    - Gate-Low: -3.24V
    - Gate-High: 6.76V
  - SwitcherB supply voltage: 3.3V (rel. to ground)
  - DCDB supply voltage: 1.8V (rel. to ground)

- Scenario
  - Scanning through the Matrix in a rolling shutter mode
  - DCDB operates in single sampling mode, ~50uA pedestal subtraction
  - SwitcherB settings:
    - Gate pulse width: 320ns
    - Clear pulse of 40ns at the end of a gate pulse
  - Matrix settings:
    - Pixel 0 and 2 are initially loaded (→ signal!)
    - Pixel 1 initially unloaded (→ no signal!)

Simulation Example: Screenshot



Simulation Example: Clear Pulse Width vs. Signal Amplitude



Open Issues

Open Issues

1. Get more realistic models
   - DCDB, SwitcherB: Use RC-extracted Spectre netlists
   - DEPFET Matrix: Include coupling caps between transistor terminals, …
   - Extract RC of the chip interconnections

   → Need simulation performance

2. Fight simulation software bugs
   - Finding / exploring bugs
   - Developping work-arrounds

   → Need several runs for debugging (performance!)

Open Issues

3. Solve simulation performance issues

- Suitable hardware infrastructure is available:
  2x Quad-Core Intel Xeon 3GHz CPU with 32GB RAM
- Simulation runs on only two threads, one for each simulator
  (CPU usage: ~140%)

→ Possible solution: Cadence Accellerated Parallel Simulator (APS)

- We have the licences
- Used routinely by us for analog and mixed-signal simulations
- Measured: CPU usage constantly 400-600%
- The SpectreCMI model of the DEPFET transistors is not ready to support APS

Summary

- The DEPFET system simulation environment is set up and running!

- Included models:
  - SwitcherB
  - DCDB
  - DEPFET Matrix

- There are still some open issues

→ We have a powerful tool for checking the correct chip interaction!

Thank you!