Vertex Ladder Engineering: from the STAR experience to an ILC design

A Vertex Detector for the ILC, Workshop at Ringberg Castle

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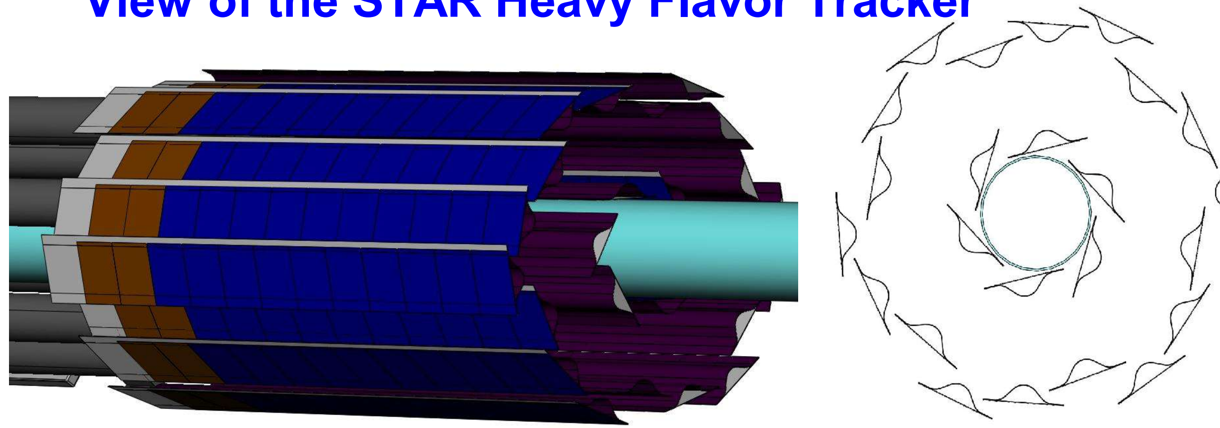
Outline

- Introduction: the STAR Heavy Flavor Tracker
- Test facilities at LBNL
- STAR HFT prototype ladder testing
- Back-thinning studies
- Outlook: towards a ladder design for the ILC

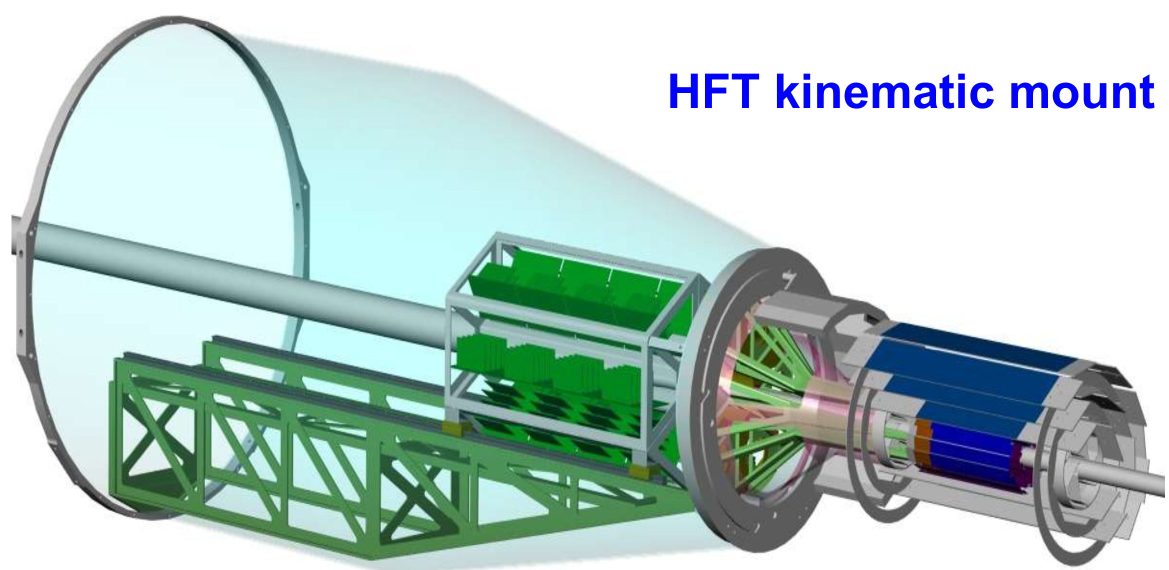
The upgrade of the STAR vertex detector

- **New high-resolution vertex detector inside existing one**
- **Improve D meson tag**
- **2 layers** at 1.5 cm and 4.5 cm radii
- **24 ladders**
  - 2 cm × 20 cm each
  - **~100 Mpixels, 30×30 μm^2**
  - 4 ms readout time
  - Rad-hard to 2 kRad/yr
- **Project approved:** funding for 2 years R&D followed by construction
- **LBNL leadership of project**

View of the STAR Heavy Flavor Tracker



HFT kinematic mount

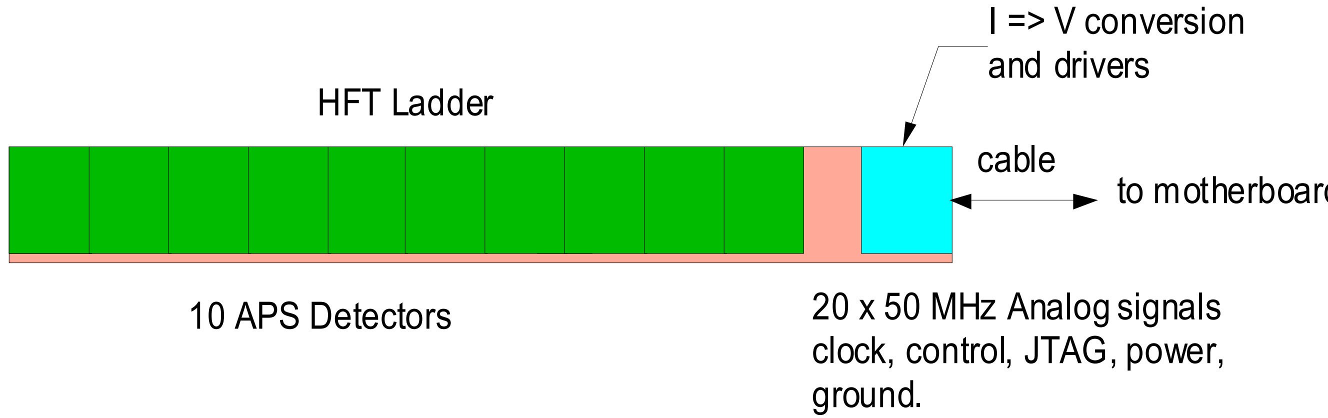


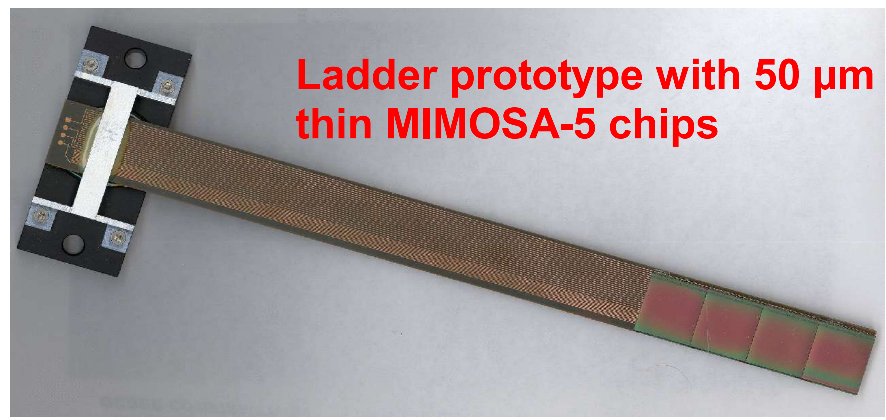
STAR/ILC VXD comparison

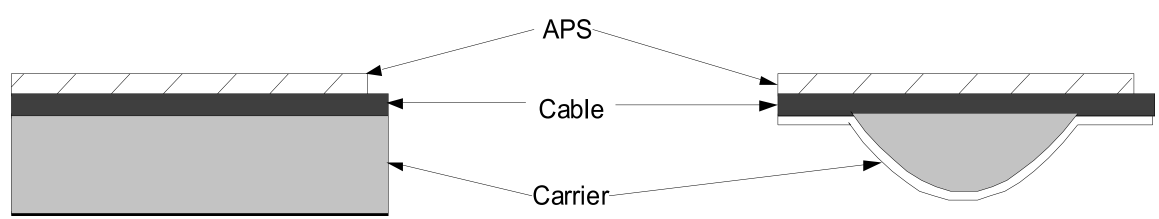
	STAR	ILC
Performance drivers	Low p_T D	b/c/τ tagging
Position resolution	~10 µm	2-4 µm
Radiation length	0.3% X_0/layer	0.1% X_0/layer
Number of layers	2	5-6
Ladders/layer	6+18	?
Operational T	40ºC	-10ºC ... 20ºC
Cooling	Air flow	?
VTX mount	Side mount	Two sides

Prototype STAR HFT Ladder

- **10 CMOS sensors**
- At the **end of the ladder**:
  - 20 I → V converters and drivers
  - Additional clock, control and JTAG connections
  - Power and ground
- Analog signals and clock/control transferred to motherboard via fine twisted pair cable
- **3 basic ladder constituents**:
  1. **APS sensor**
  2. **Cable**
  3. **Mechanical Carrier**







End view of 2 prototype designs

Test facilities at LBNL

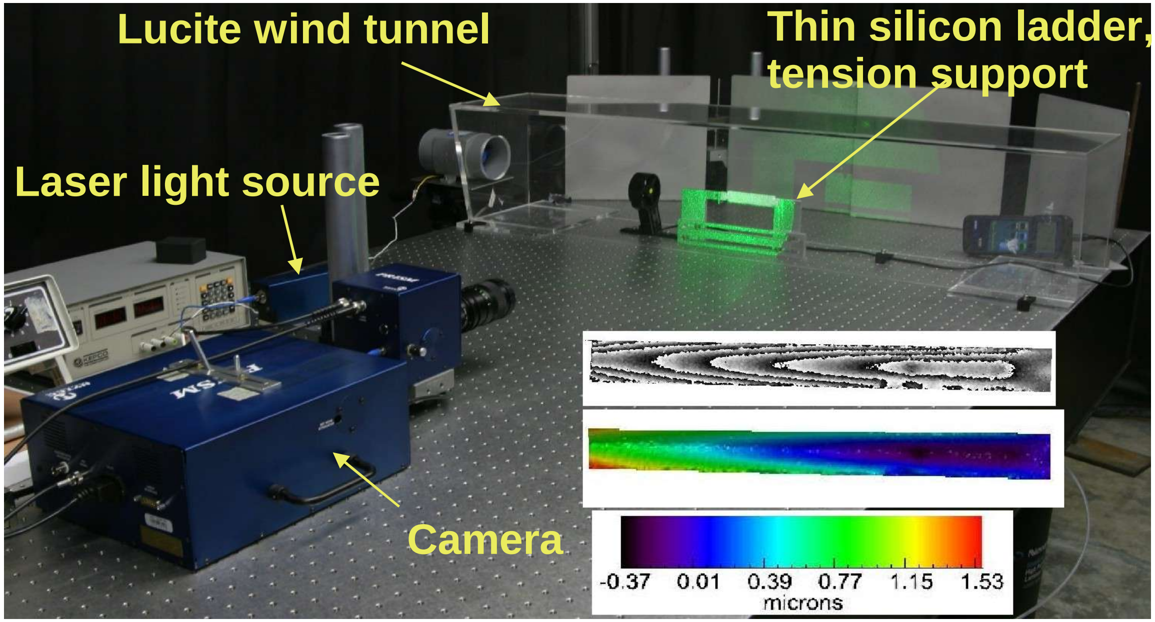
• **Environmental chamber (down to -70ºC)** for characterization of temperature cycling and humidity effects on prototype ladders

• **High resolution IR camera** for studying temperature gradient of prototype ladders, e.g. to study heat dissipation under power cycling

• **Facility for studies of cooling and mechanical stability with nitrogen and air flow**, equipped with a **laser holography system** for real time measurement of distortions in prototype structures with sub-μm resolution

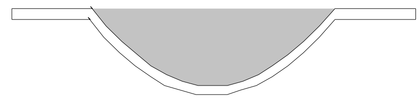
• **Capacitive probe system** for sub-μm resolution measurement of reference positions. Bandpass of 1 KHz, above typical resonant frequencies of ladders → study displacements and vibrations induced by air cooling or other forces

• **Composite lab material** for fabrication of light structures



Test of STAR HFT Ladder Prototype

2 carrier candidates



Top layer = 50 µm CFC

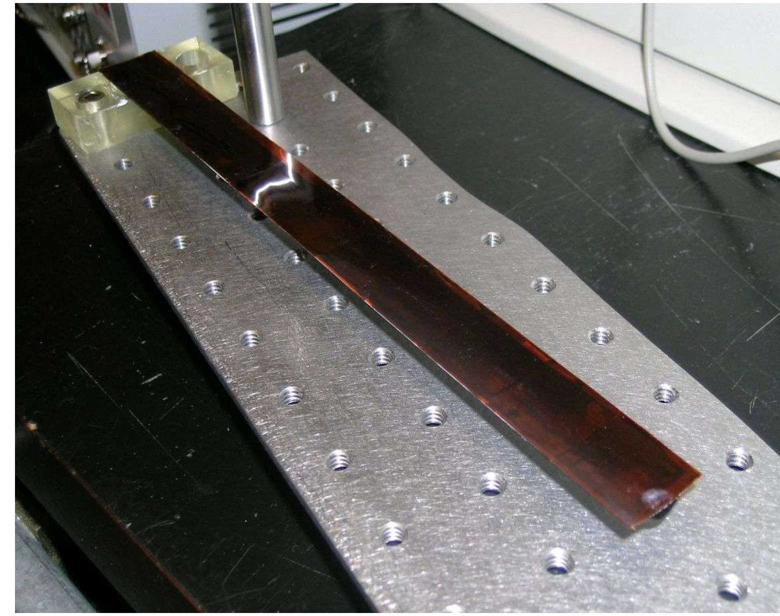
Middle layer = 3.2 mm RVC

Bottom layer = 50 µm CFC

Outer shell = 100 µm CFC

Fill = RVC

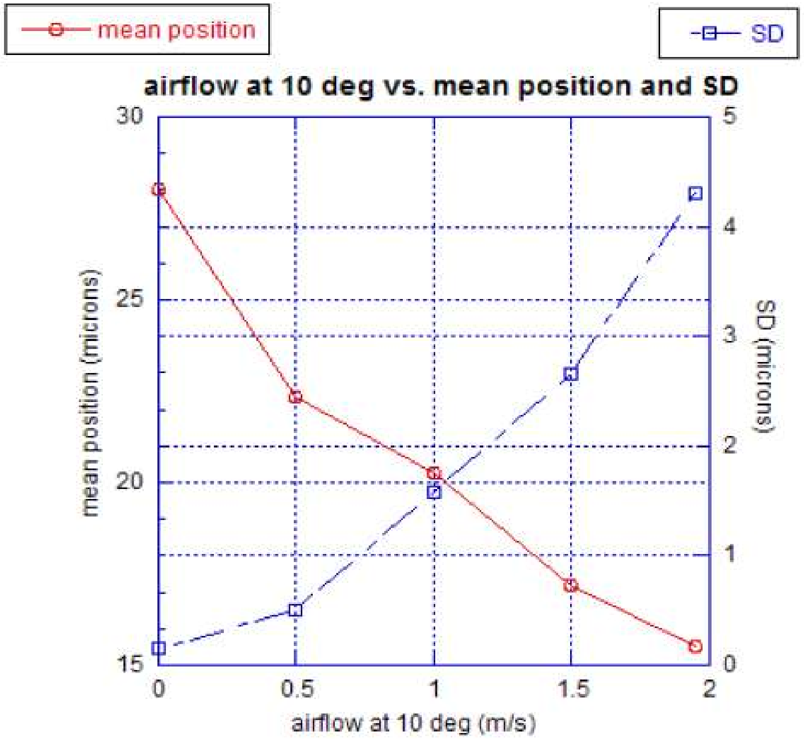
X_0 =0.11 %



- Displacement as a function of time measured using capacitive probe at unsupported end of prototype ladder (carrier+kapton+50 µm silicon)

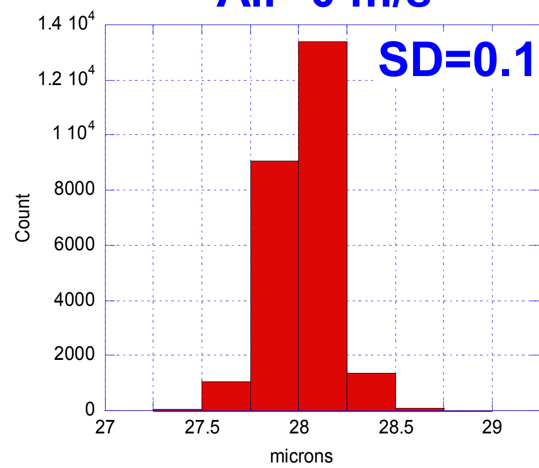
- Fundamental resonance frequency measured from FFT of oscillations:
  - Measured = 139 Hz
  - Calculated = 135 Hz

Vibration from air cooling

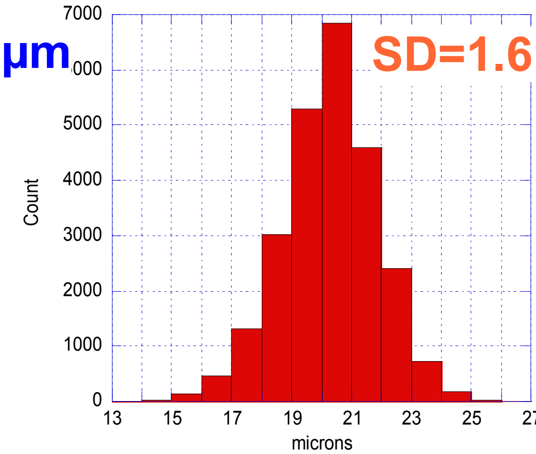


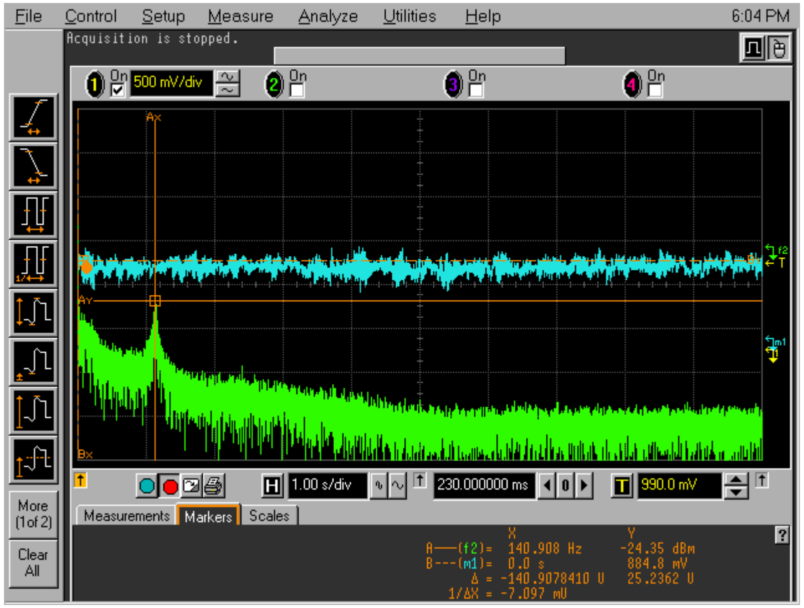
http://www.lbnl.leog.org/writeup.htm

Air=0 m/s SD=0.16 µm



Air=1 m/s SD=1.6 µm

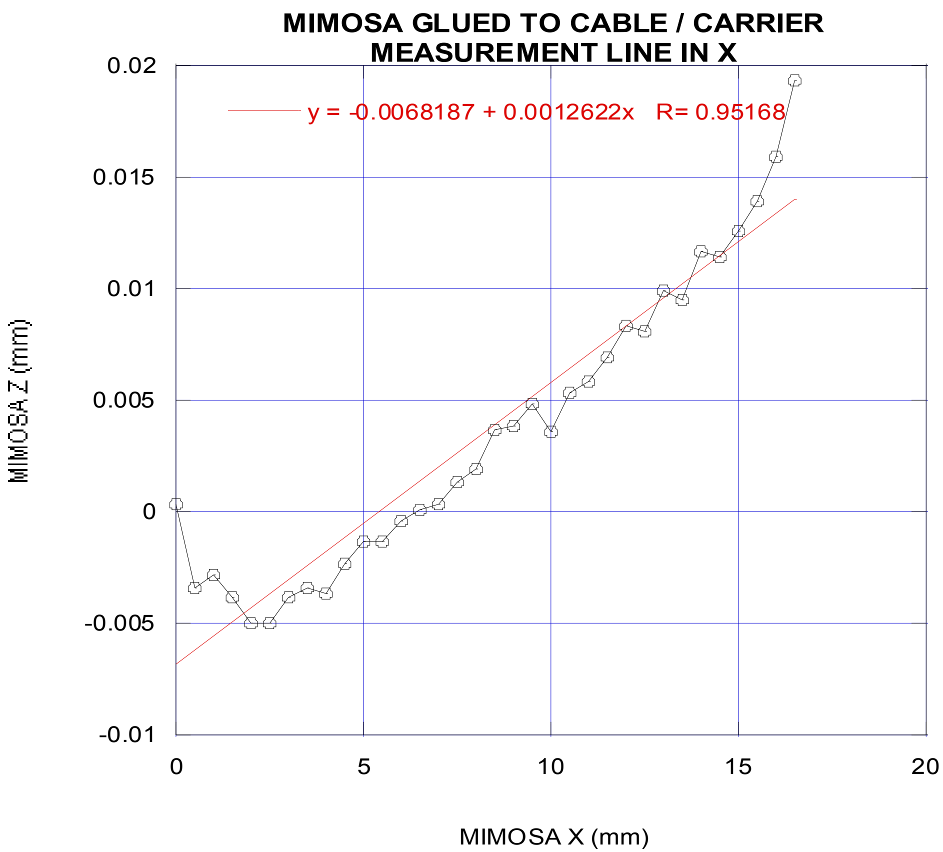


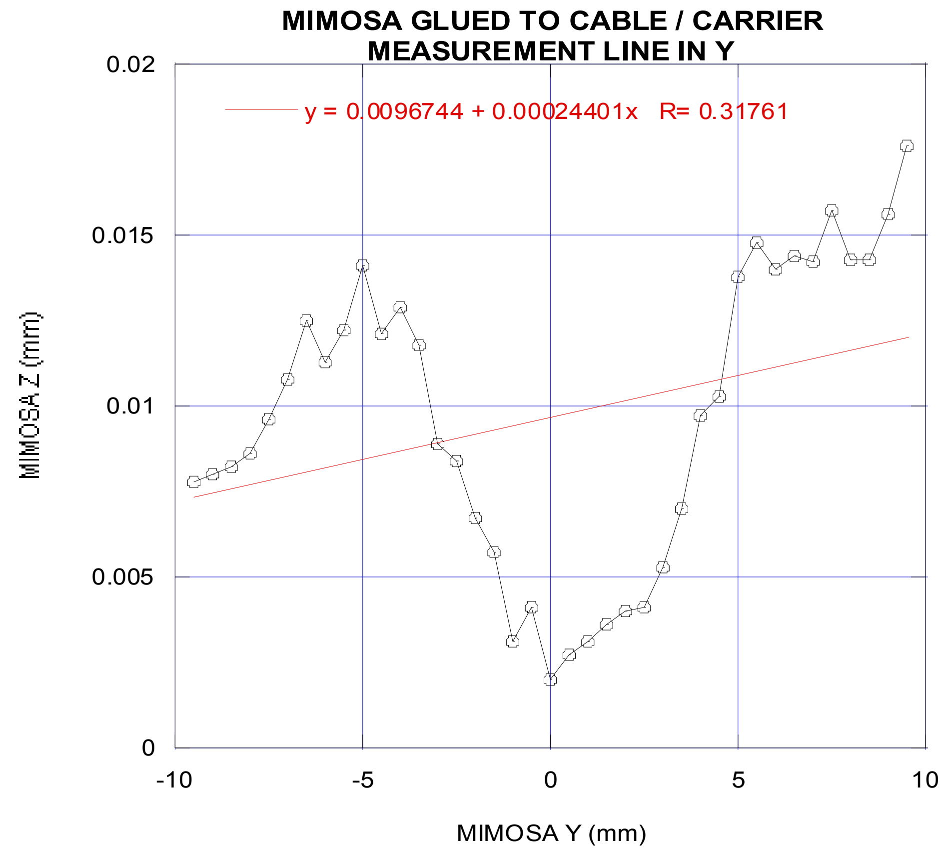


- Airflow at 10º onto prototype ladder measured at unsupported end gives measured location distribution with SD~1.6 µm at 1.0 m/s of airflow

- As the airflow increases, the free end of the ladder moves away from the capacitive probe, and the magnitude of the induced vibrations increases

Test of prototype Si flatness



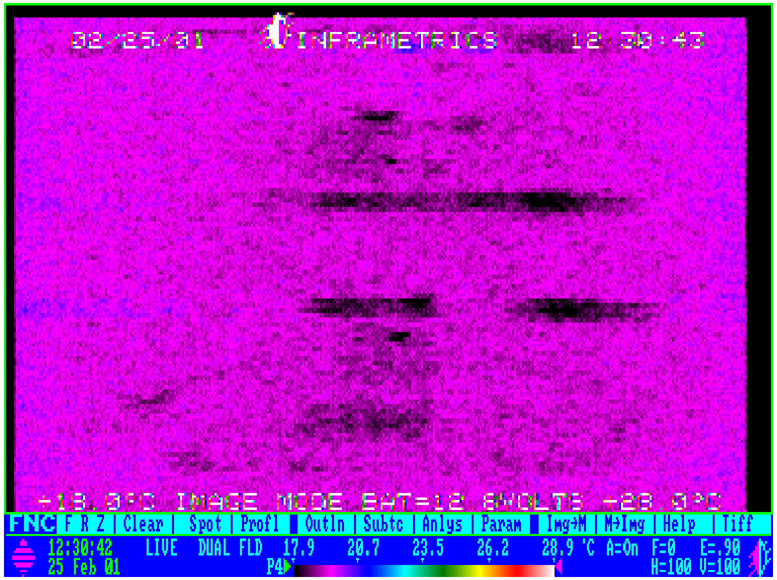


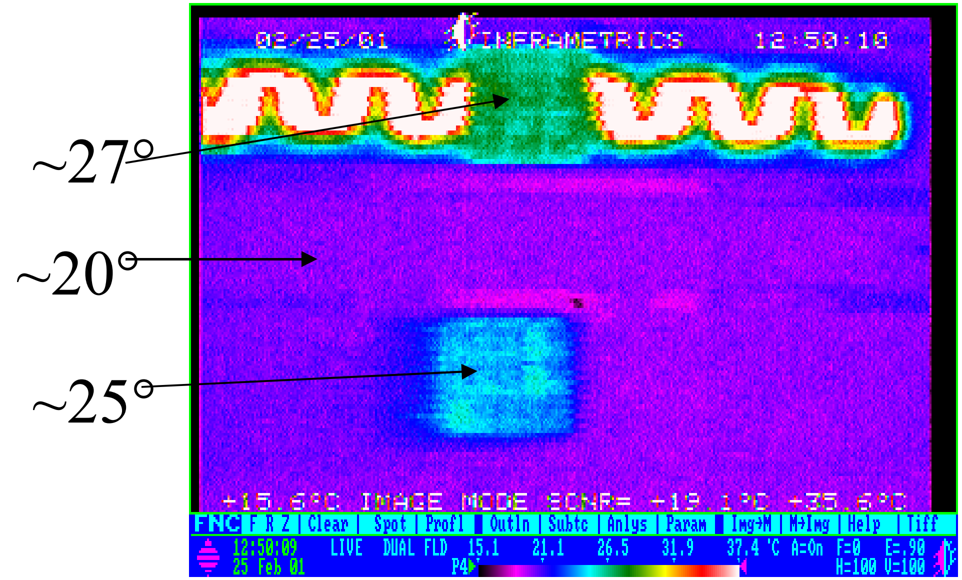
- Measurements performed at optical measuring machines at LBNL inspection and metrology shop
- 50 µm thin MIMOSA-5 sensors glued to cable and to support carrier
- Variations within 20 µm in both directions on sensor surface
- Individual pixel position can be located to the required accuracy by a parameterized location function

Air cooling tests

Airflow = 0
Heaters = off

Airflow = 0.8 m/s
Heaters = on





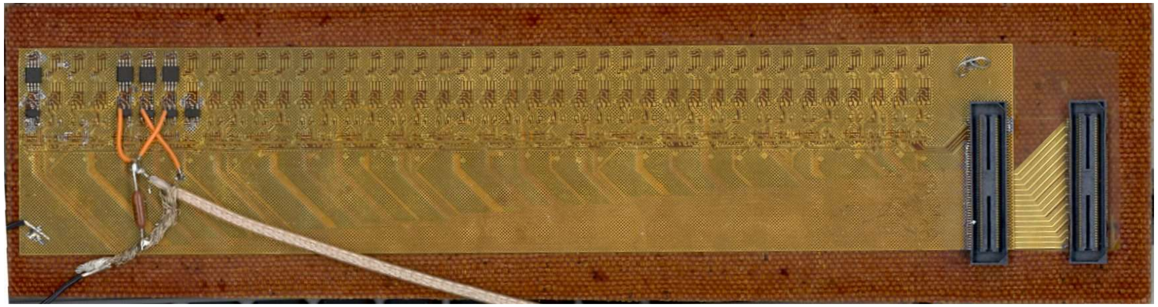
Emissivity of Si and Kapton is uniform

Si temperature rises ~5-7ºC above ambient
Good uniformity in temperature over sensor

- **IR thermal imaging of Si and Kapton**
- **Upper test piece**: 2 layers of 2 cm x 2 cm x 50 µm thick Si glued to Pt heater serpentine strip at 100 mW/cm^2
- **Lower test piece**: 2 layers of 2 cm x 2 cm x 50 µm thick Si with resistor heating at 164 mW along the upper edge and 90 mW distributed over the rest of the piece

http://www.lbnl.leog.org/ir_prelim_writeup.htm

STAR HFT Ladder Prototype Cable



Prototype with Al conductor

Prototype with Cu conductor and several MIMOSA-5 chips mounted

- ~100 traces (2 LVDS pairs/sensor, clock, power, ground, control signals)
- 4 layer design, 25 µm kapton, 20 µm Al conductor
- Impedance controlled signal/clock pairs with power and ground geometrically arranged as shielding

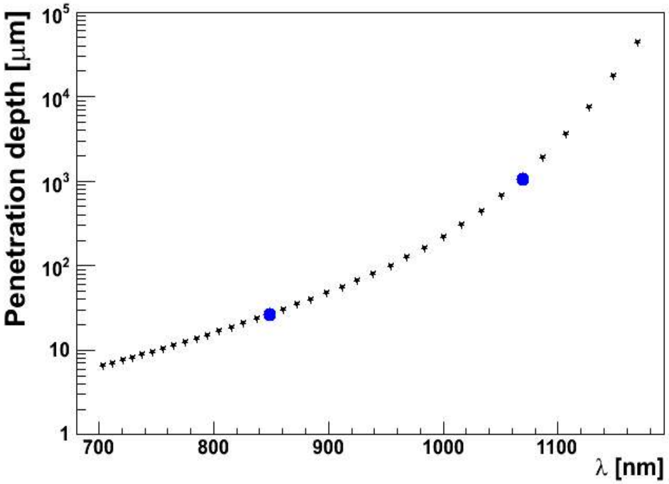
X_0 =0.090 % **(for Al conductor)**

STAR HFT Ladder Material Budget

Component	% radiation length	Si equivalent (µm)
MIMOSA detector	0.0534	50
Adhesive	0.0143	13.39
Cable assembly	0.090	83.92
Adhesive	0.0143	13.39
Carbon fiber / RVC carrier	0.11	103
Total	**0.282**	**263.7**

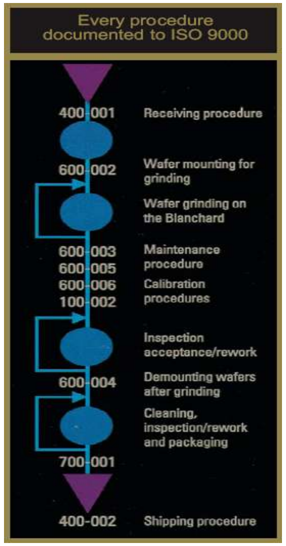
Back-thinning studies

- Tests performed on diced MIMOSA-5 chips from IPHC/IReS (Strasbourg)
- AMS 0.6 µm, 14 µm epilayer, 1 Mpixels on reticle-size area of 1.7×1.9 cm^2, 17 µm pixel pitch

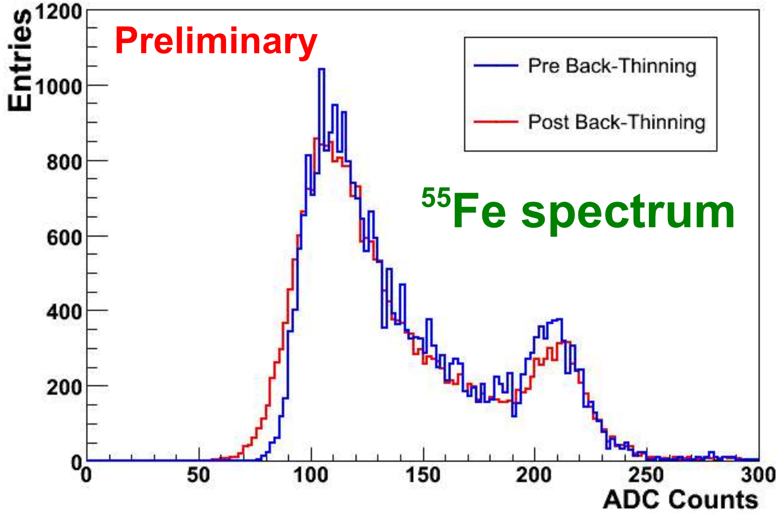


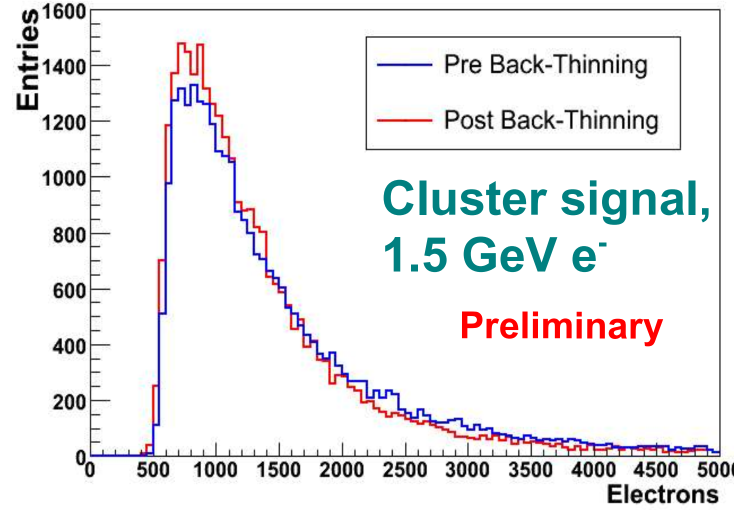
- Chips initally mounted to PCB with reversible glue and fully tested with 1.5 GeV e$^-$ beam and lasers of different wavelengths → probe signal from different silicon depths and estimate substrate contribution

- Chips removed by heating to 120ºC
- Back-thinning to 25-50 µm performed by Aptek (San Jose, CA), www.aptekindustries.com
  - Proprietary hot wax formula for wafer mounting to stainless grinding plates
  - Wet grind process + polishing
  - In-situ thickness measurement
- Re-mounting and re-characterization



Back-thinning to 50 µm: latest results

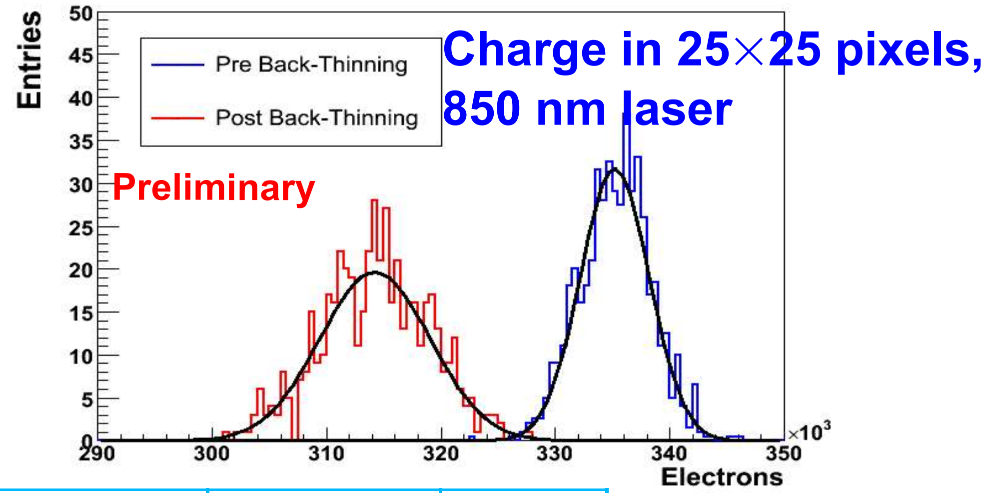




- Negligible variation of charge-to-voltage conversion gain

- No charge losses for MIP detection

- Small variations from laser tests: no significant contribution from substrate to collected charge



	Noise	^{55}Fe peak	850 nm	1060 nm	ALS
Mean	+3%	-8%	-16%	-16%	-5%
RMS	7%	8%	6%	10%	5%

ILC LCRD Project at LBNL

- New Linear Collider R&D (LCRD) project for FY 2006-2008
- Design and prototype low mass detector modules
- Fully characterize mechanical behavior with thinned Si chips
- Assess sensor technology specifics for CMOS and DEPFET pixels
- Study air flow cooling in terms of heat extraction and ladder stability
- Investigate off-line software alignment procedures using existing algorithm developed for BaBar
- Project recently approved! Funds starting with 55 k$ for 2006, to be increased in 2007-2008