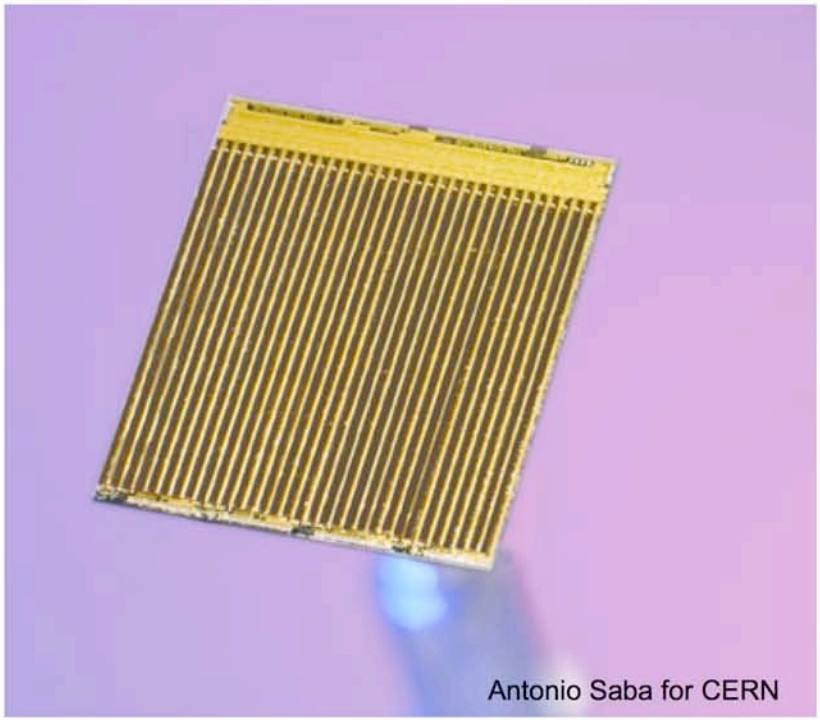
A Vertex Detector for LHC - Physics and Technologies
Workshop at Ringberg Castle, Germany, May 28-30, 2006

The ALICE Silicon Pixel Detector



P. Riedler/CERN

On behalf of the SPD Project in the ALICE Collaboration

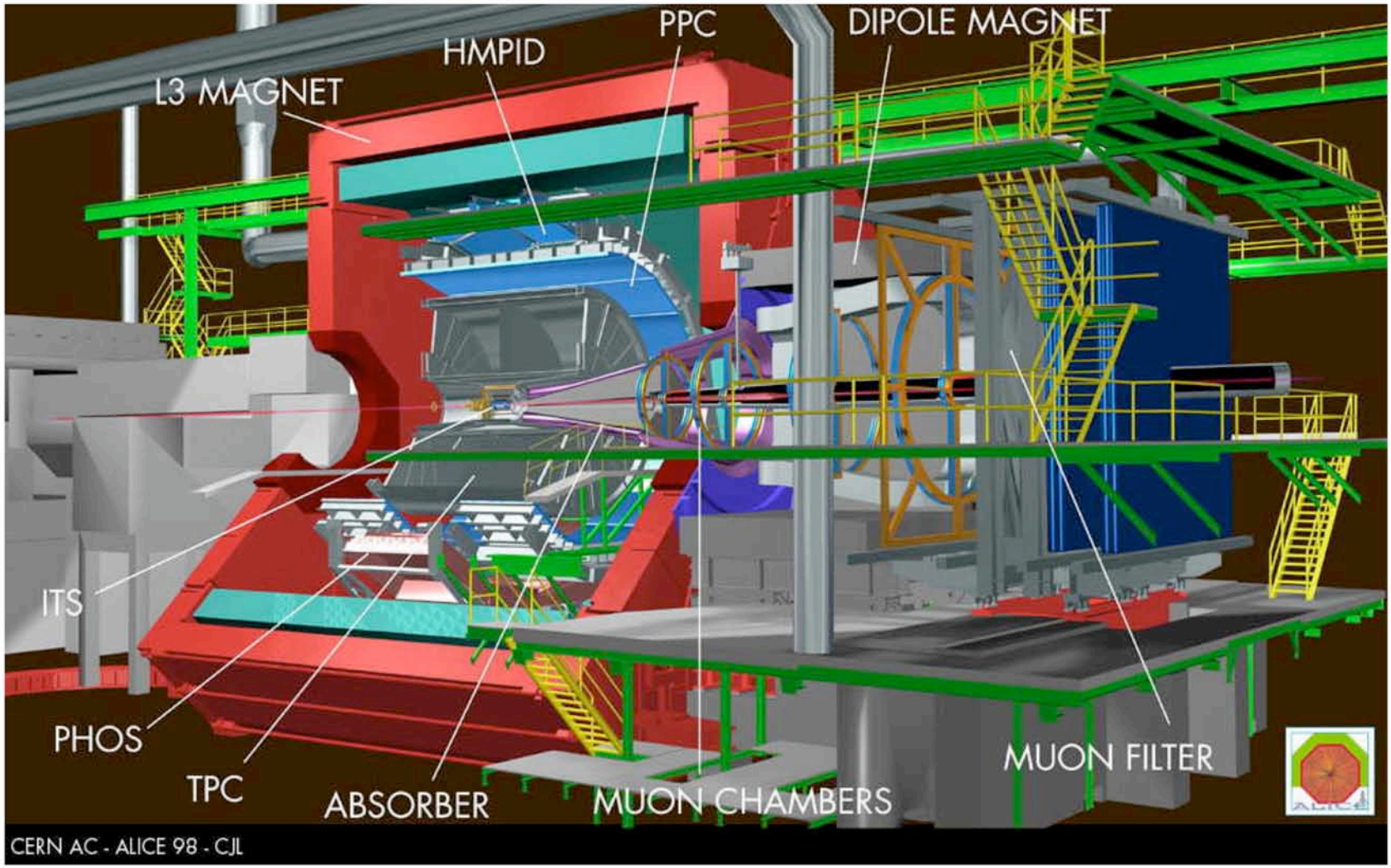
Universita e Sezione INFN Bari, Universita e Sezione INFN Catania, CERN, Slovak Academy of Sciences Kosice, LNL, Universita e Sezione INFN Padova, Universita Salerno, Universita e Sezione INFN Udine

Outlook

- Overview of the ALICE SPD
- Components
- Integration of the detector
- Summary

ALICE Experiment

- ultra-relativistic heavy ion collisions
- p-p collisions



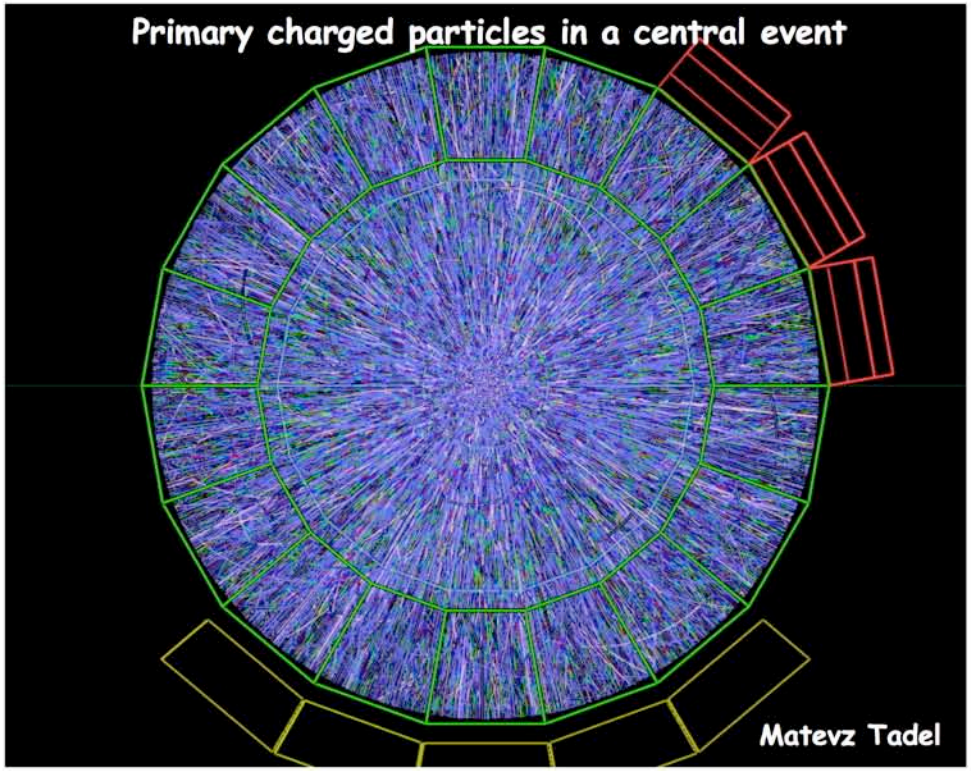
ALICE Experiment

Major challenge:

In central HI collisions up to 8000 charged particles/ $|\eta|$ are expected.

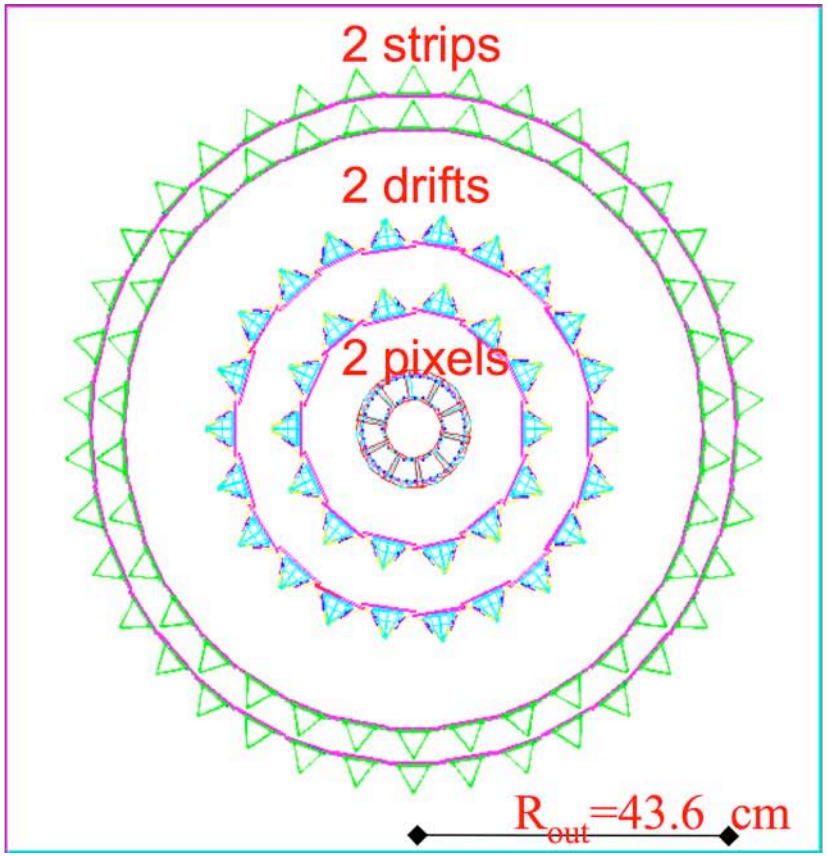
⇩

Large tracking detector (TPC)
+
inner tracking system (ITS)
consisting of **silicon detectors**



ITS and SPD

The Inner Tracking System (ITS)



Radial coverage defined by beampipe and requirements for track-matching with the TPC

Inner layers:

- high multiplicity environment (~80 tracks/cm^2)
- unambiguous 2D-readout
- secondary vertexing capability

⇒ 2 layers of **S**ilicon **P**ixel **D**etectors

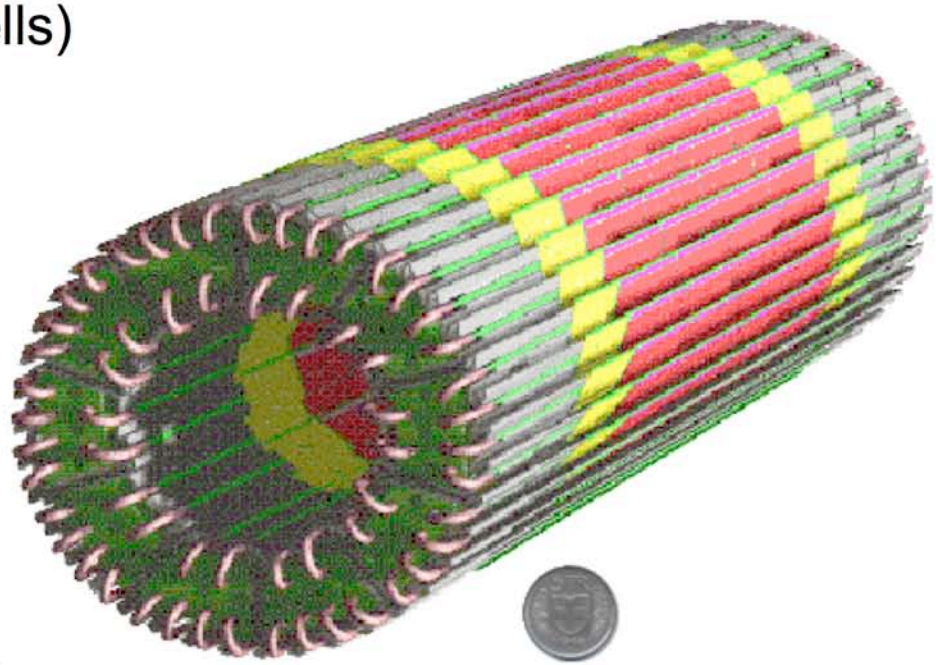
S P D

ITS and SPD

SPD in Numbers (I)

System parameters (I):

- 2 barrel layers (radii 3.9 cm and 7.6 cm, Δ z= 28.6 cm)
- 1200 readout chips (~ 10^7 pixel cells)
- 120 modules (half-staves)

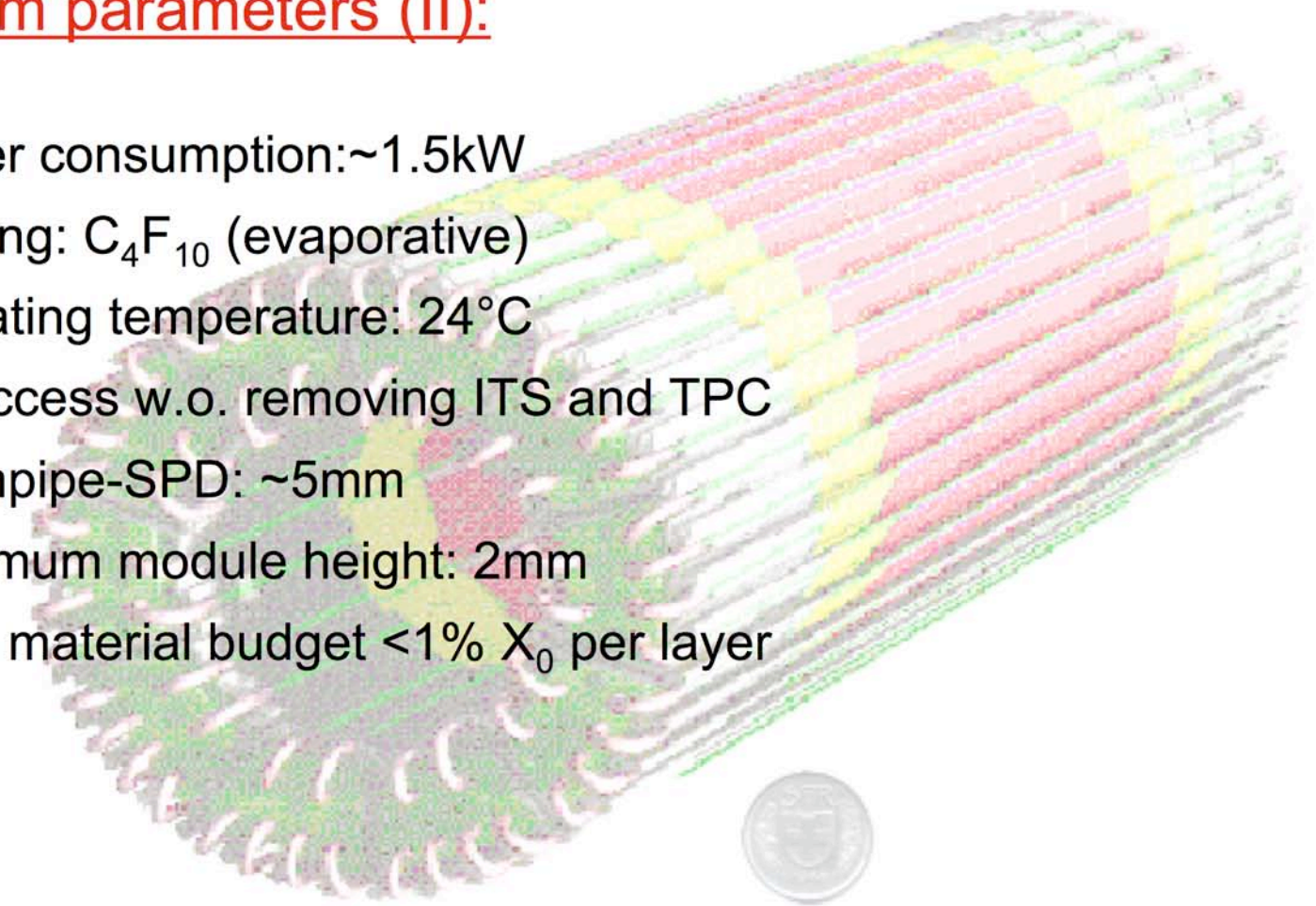


- L1 after 6 μs, L1 rate 1 kHz
- L2 after 100 μs, L2 rate 40 - 800Hz
- Readout upon L2 (~ 1 GB/s raw data)
- Radiation: 250 krad/3 x 10^{12} 1MeV n/cm^2 (10yrs)

SPD in Numbers (II)

System parameters (II):

- Power consumption:~1.5kW
- Cooling: C_4F_{10} (evaporative)
- operating temperature: 24°C
- No access w.o. removing ITS and TPC
- beampipe-SPD: ~5mm
- Maximum module height: 2mm
- Total material budget <1% X_0 per layer



SPD Challenges

Main challenges:

Cooling

- 1.5kW,24°C
- light weight, comply with 1% X_0 material budget limit per layer

Accessibility

- no access without removing TPC and ITS
- connection of services only after TPC and ITS are in place

Space constraints

- maximum component height 2 mm per module
- average distance beam pipe -inner layer: 5 mm

Material budget

- maximum of 1% X_0 per layer
- influences design of all components

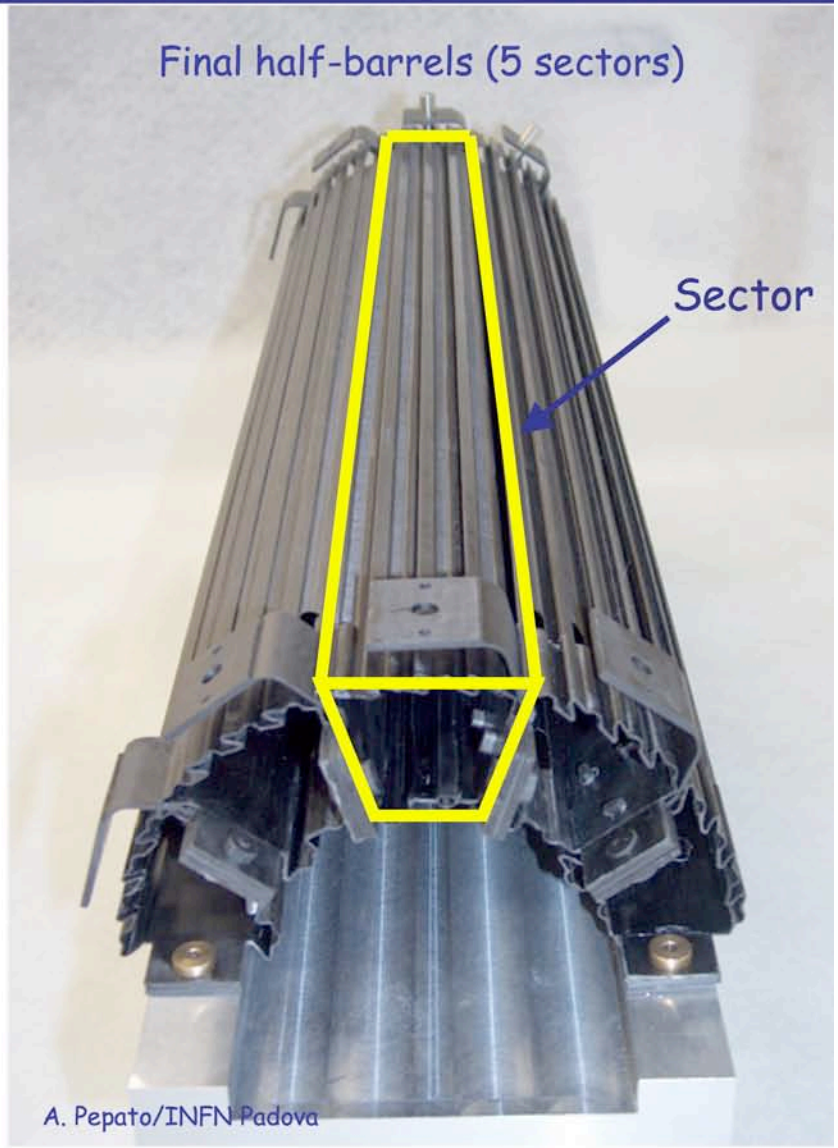
Sector Assembly (I)

- 200μm carbon fiber (CF) support

⇒ light weight
⇒ thermal efficiency
⇒ long term stability
⇒ low material budget

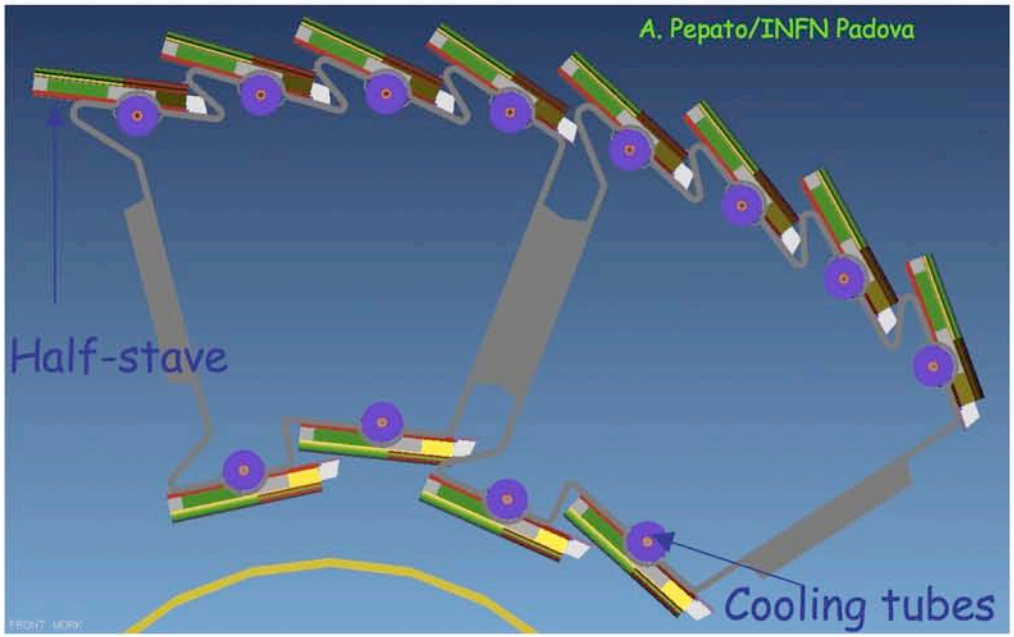
- 10 carbon fiber sectors to form 2 barrel layers

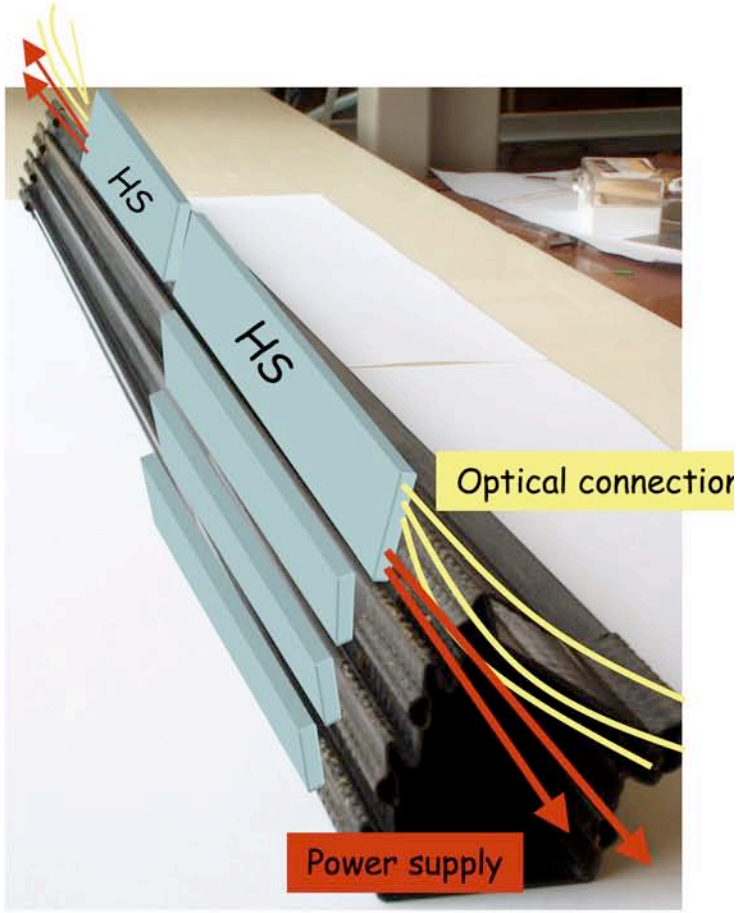
- PHYNOX cooling tubes (2.6 mm diameter, 40μm wall thickness) flattened and embedded in CF support



Sector Assembly (II)

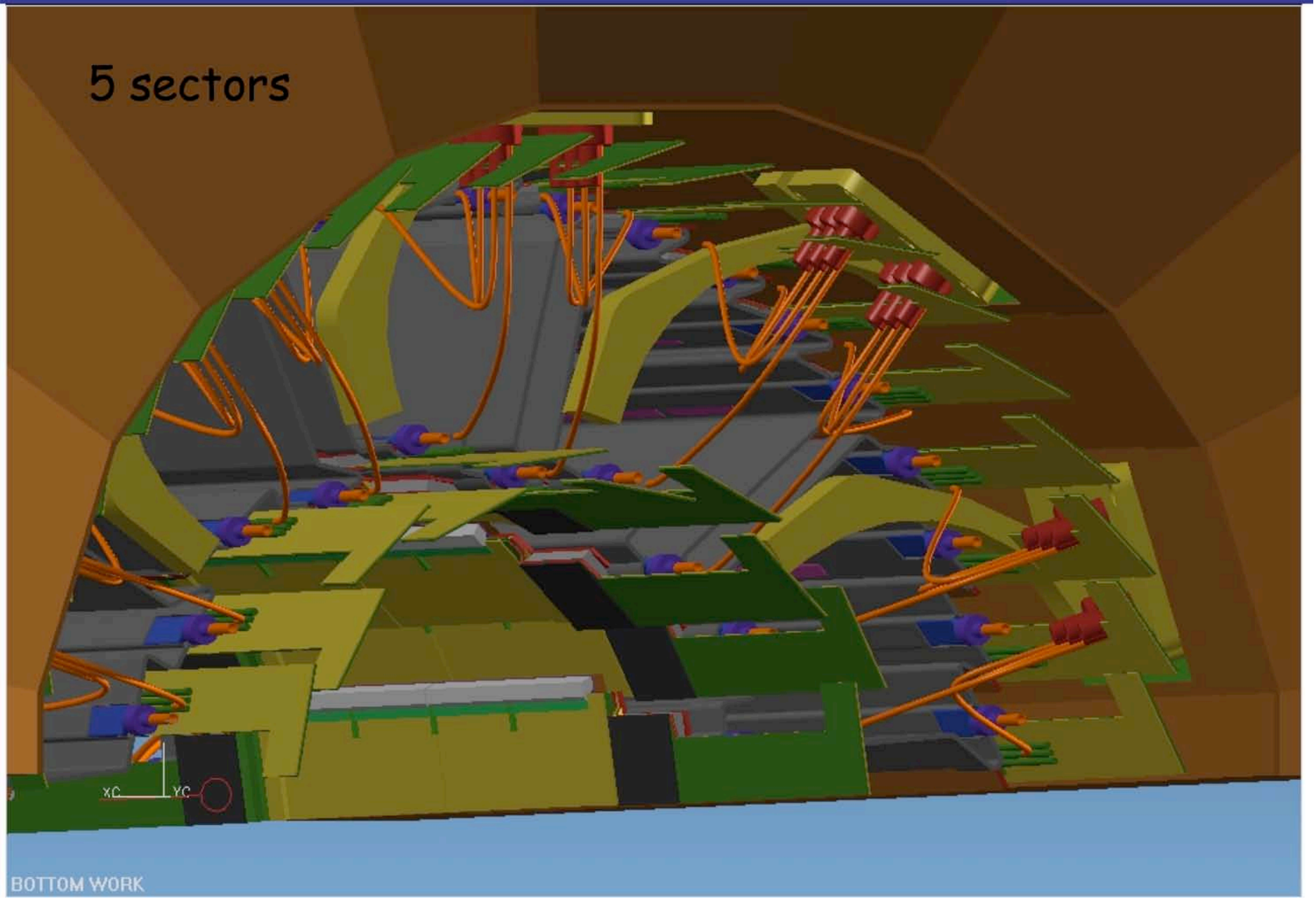
120 half-staves (HS) mounted in
- windmill configuration - outer layer
- staggered mounting - inner layer





Each HS is provided with power and optical connections on one side.

Sector Assembly (III)



Half-Stave Components

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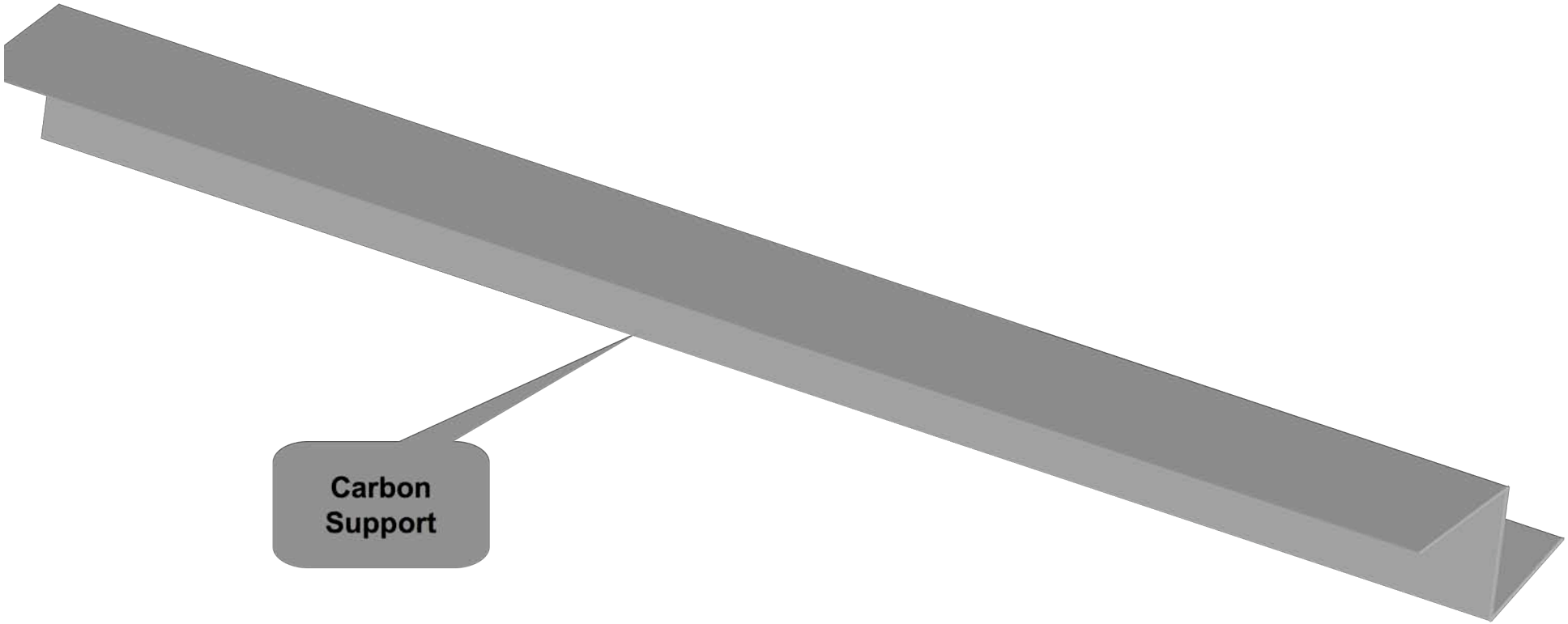

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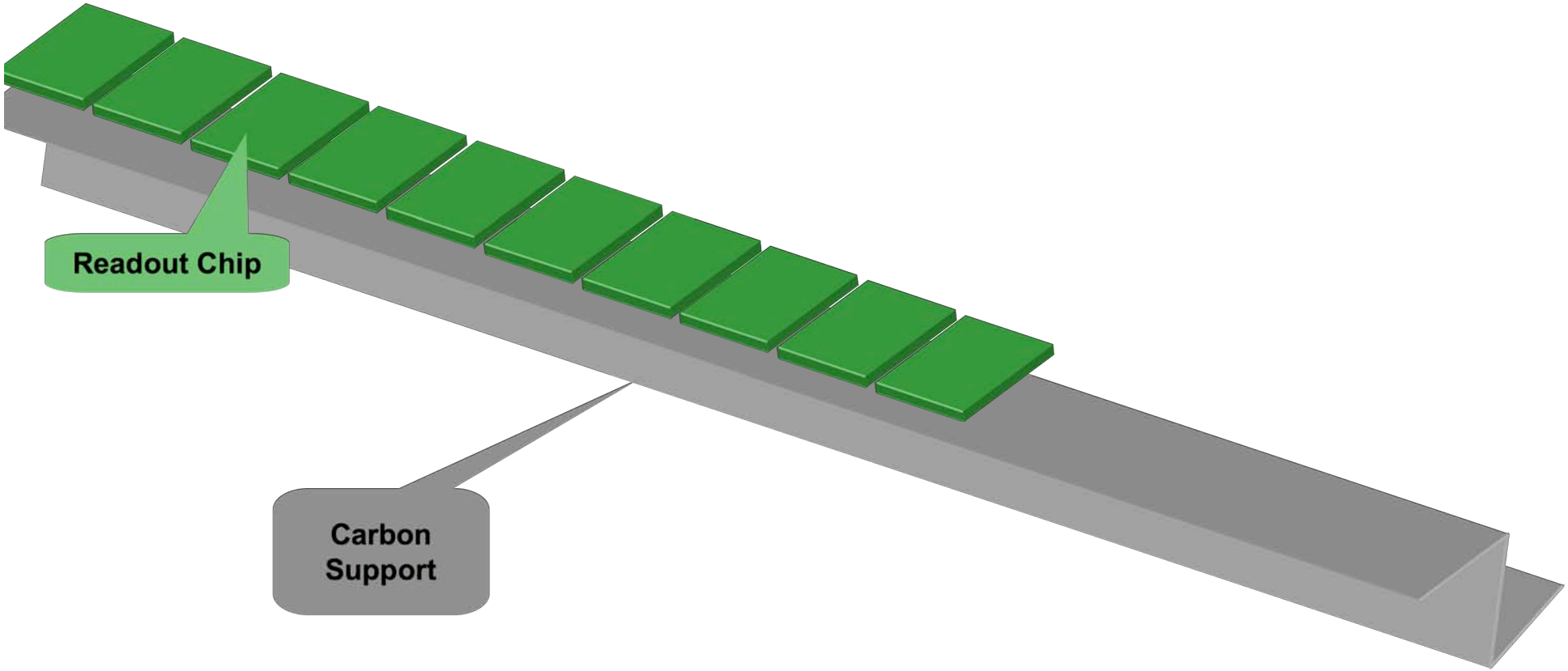

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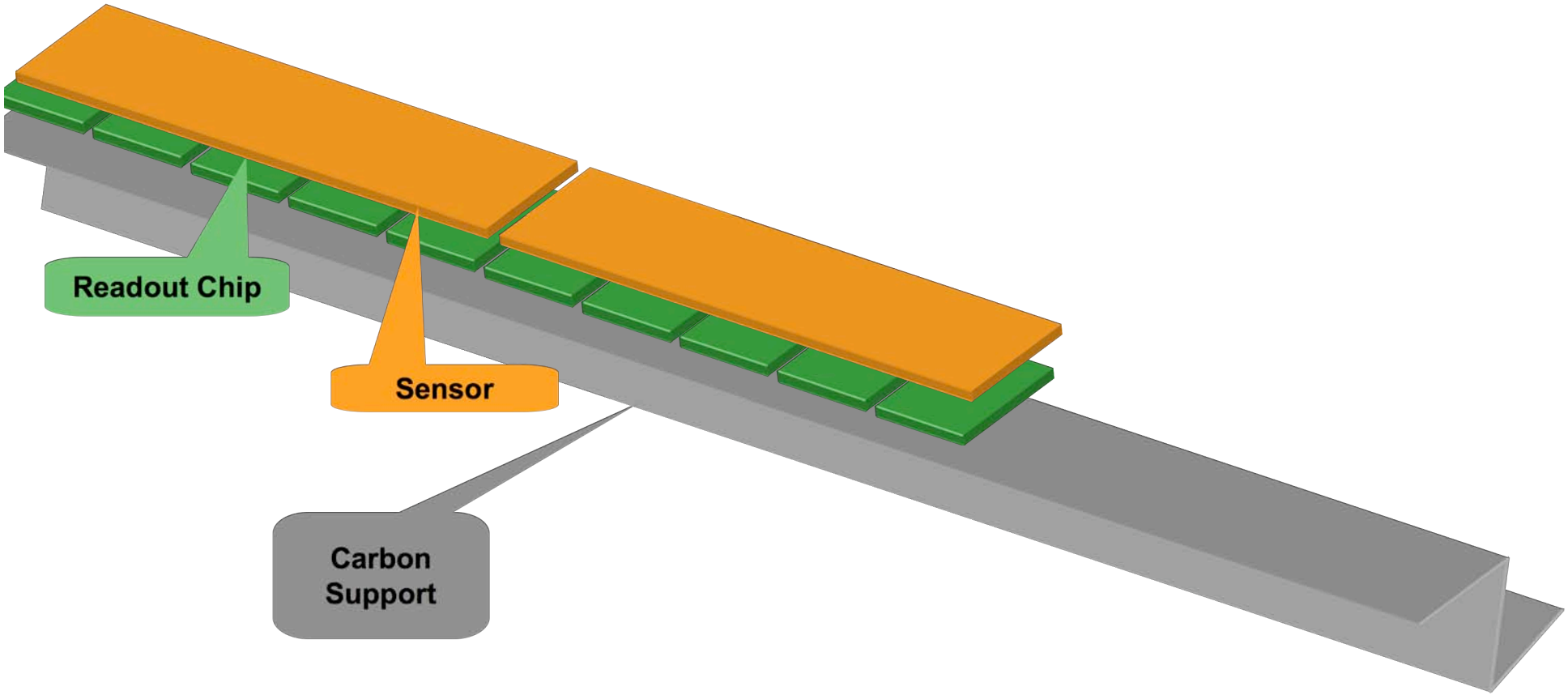
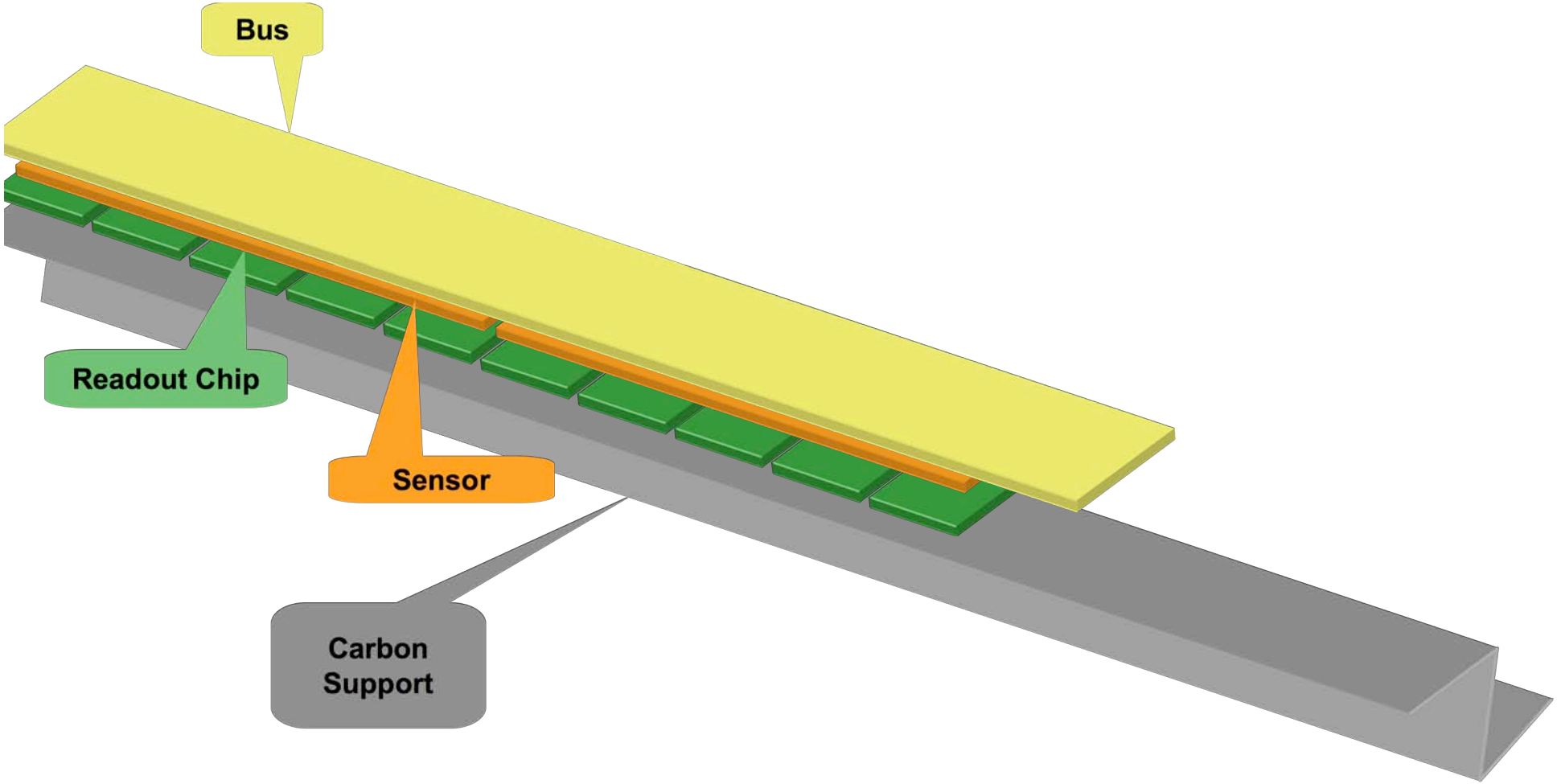


Half-Stave Components



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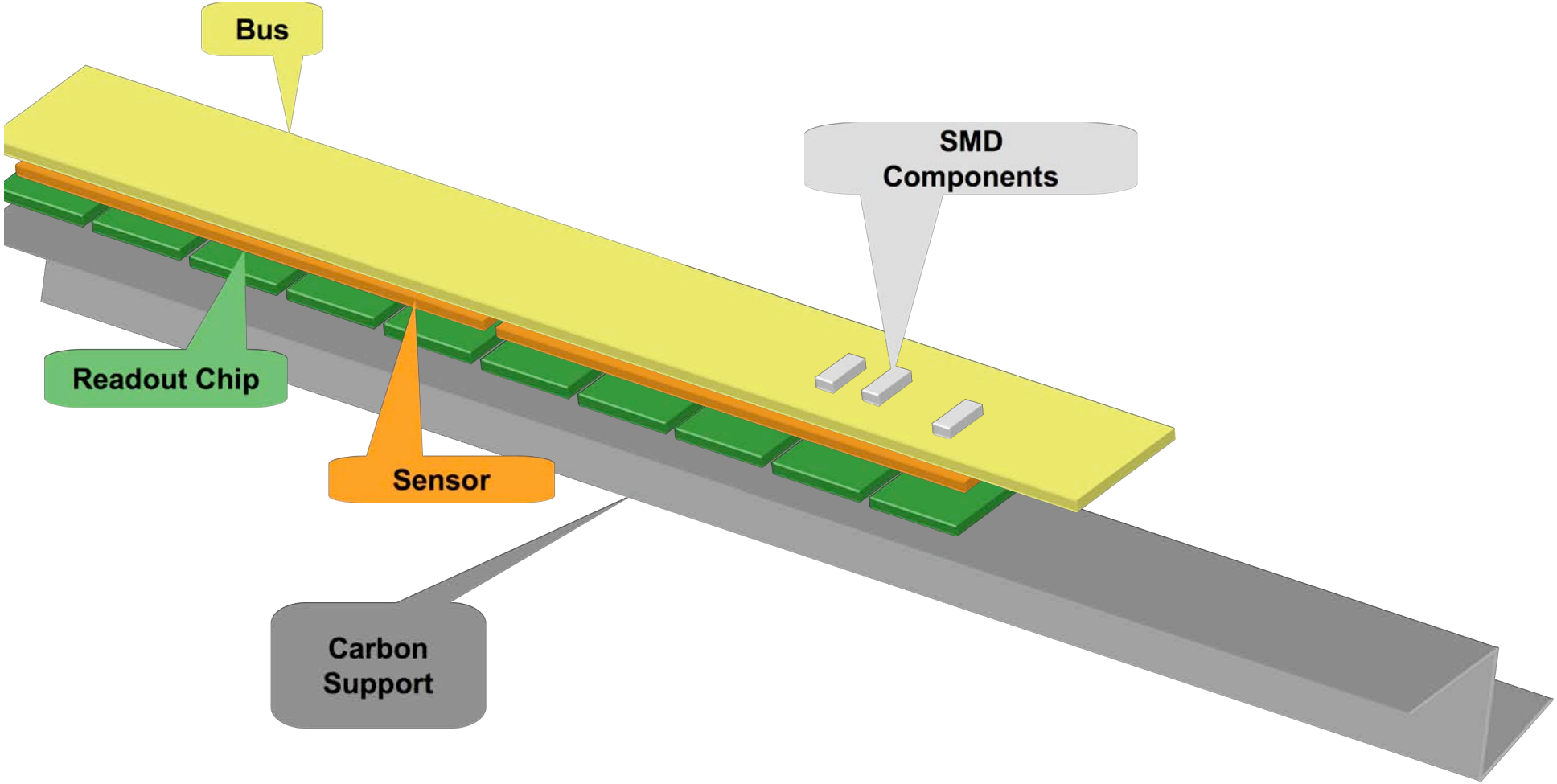

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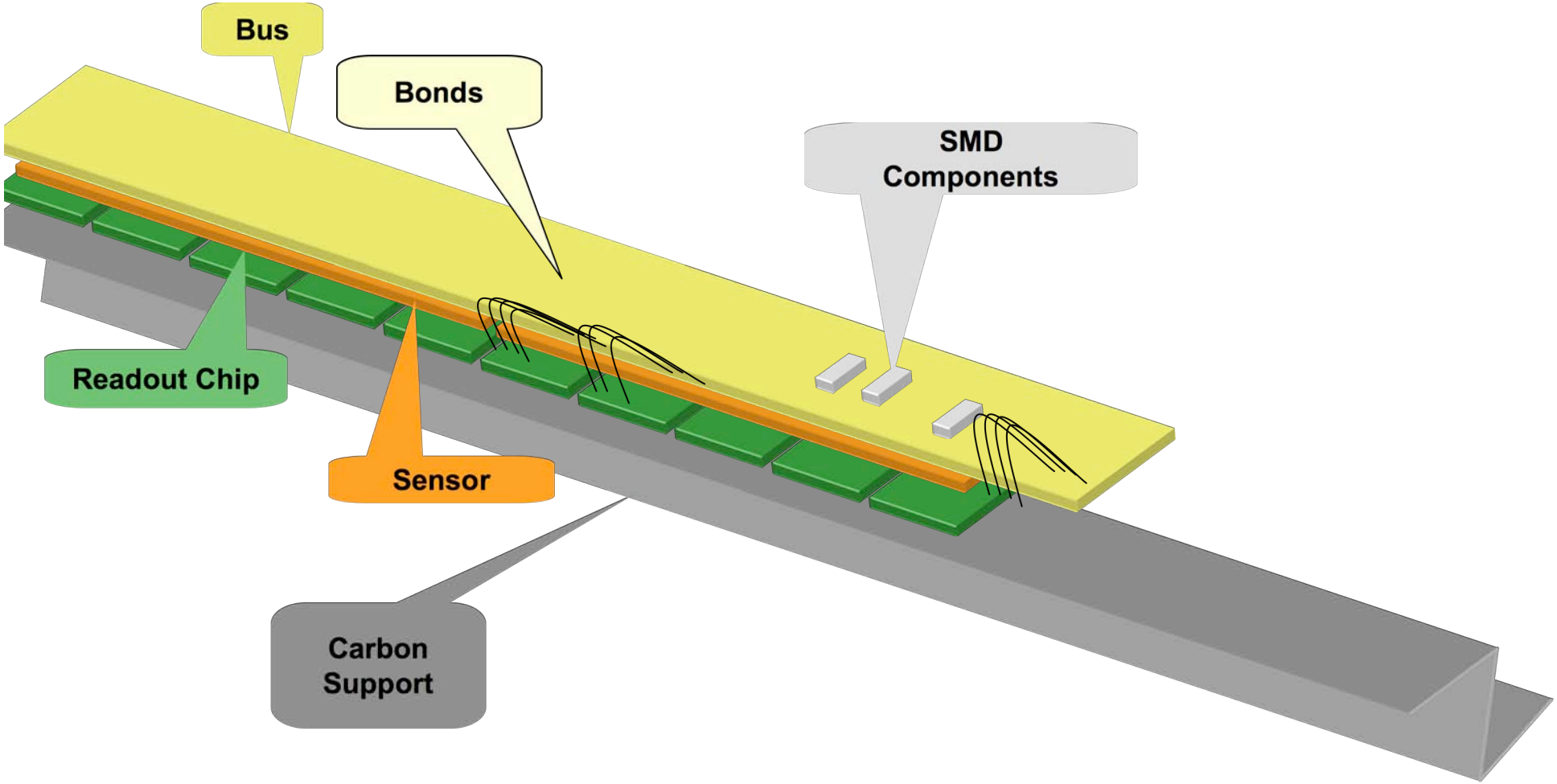

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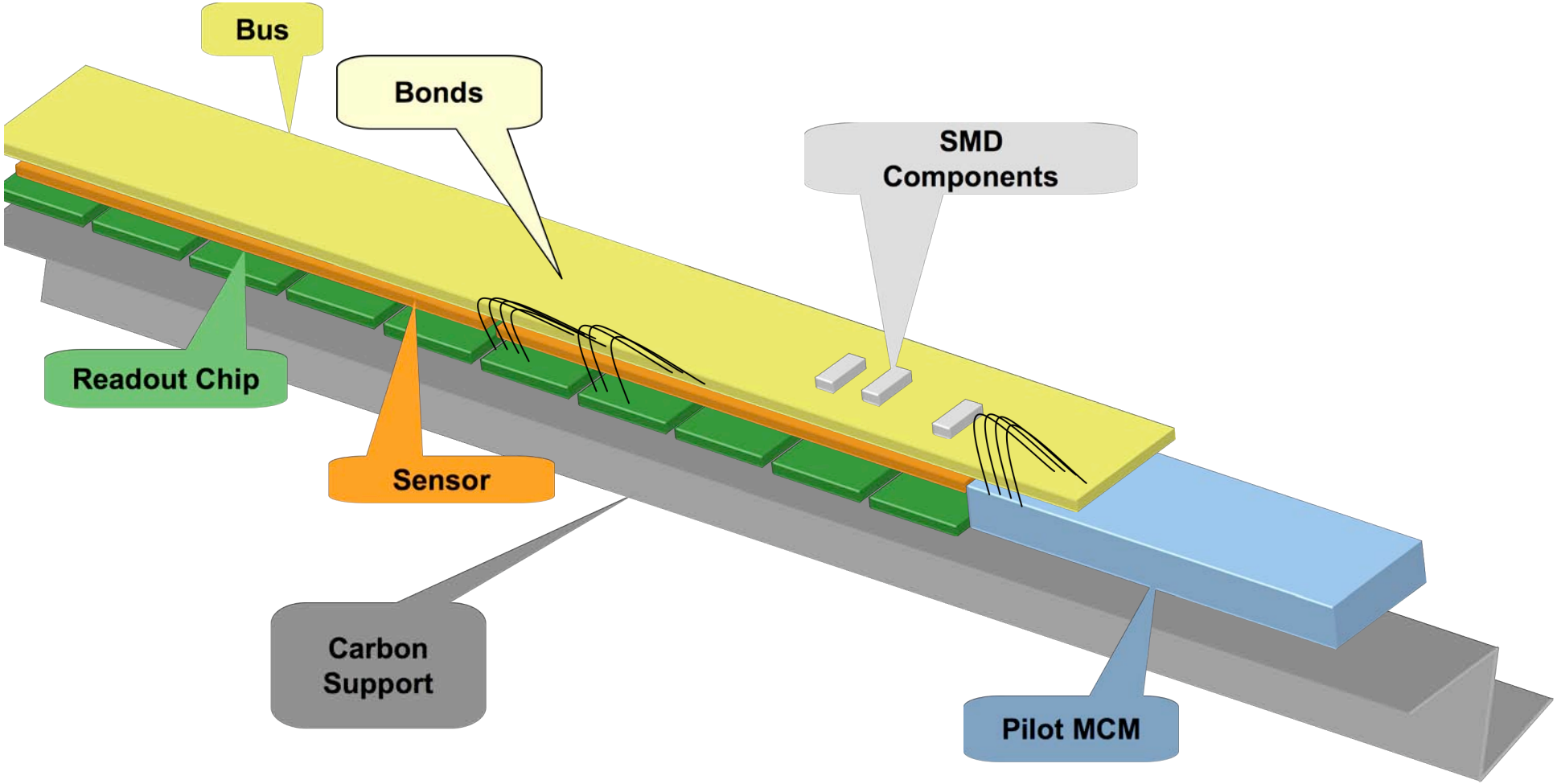

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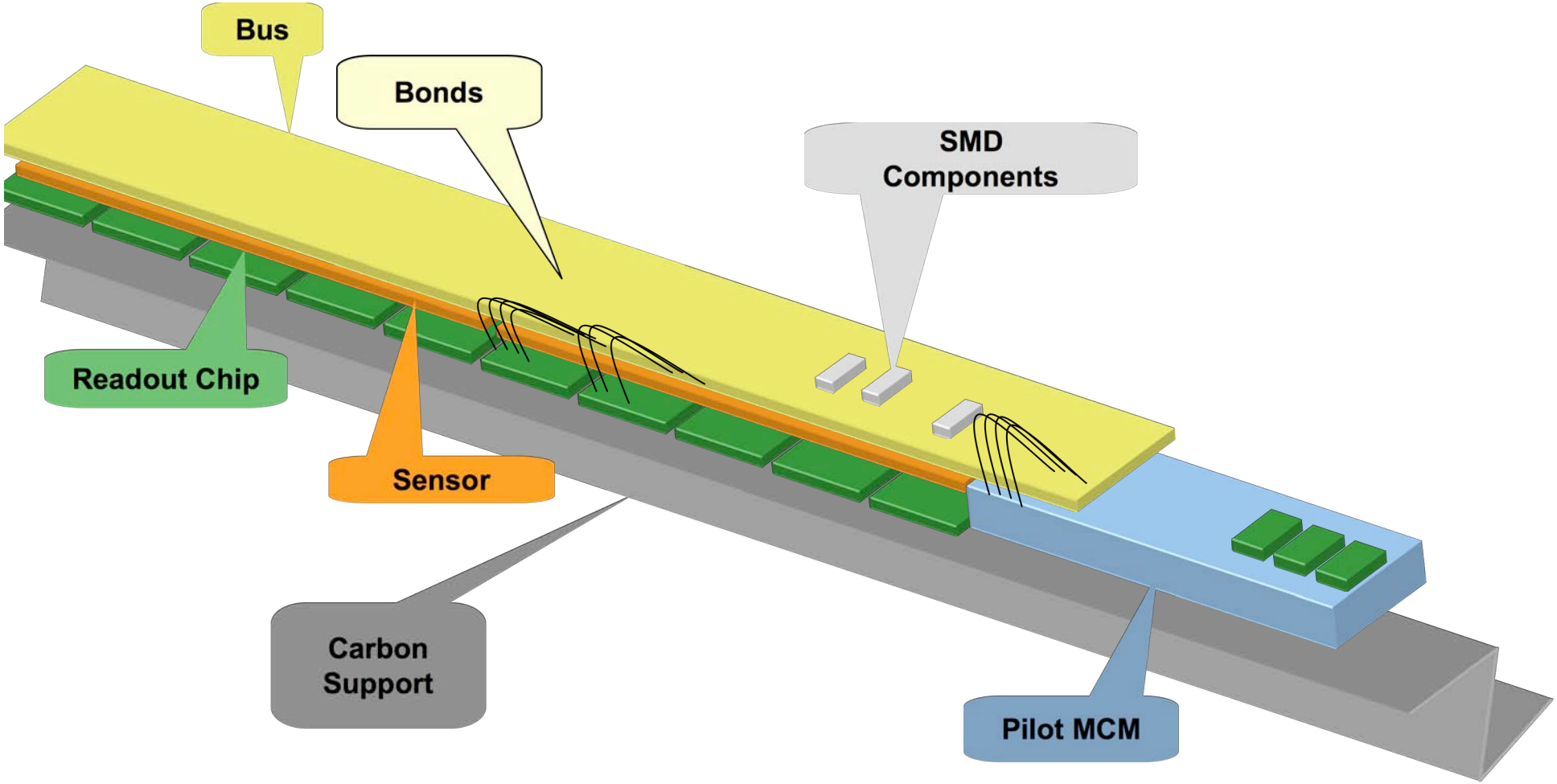

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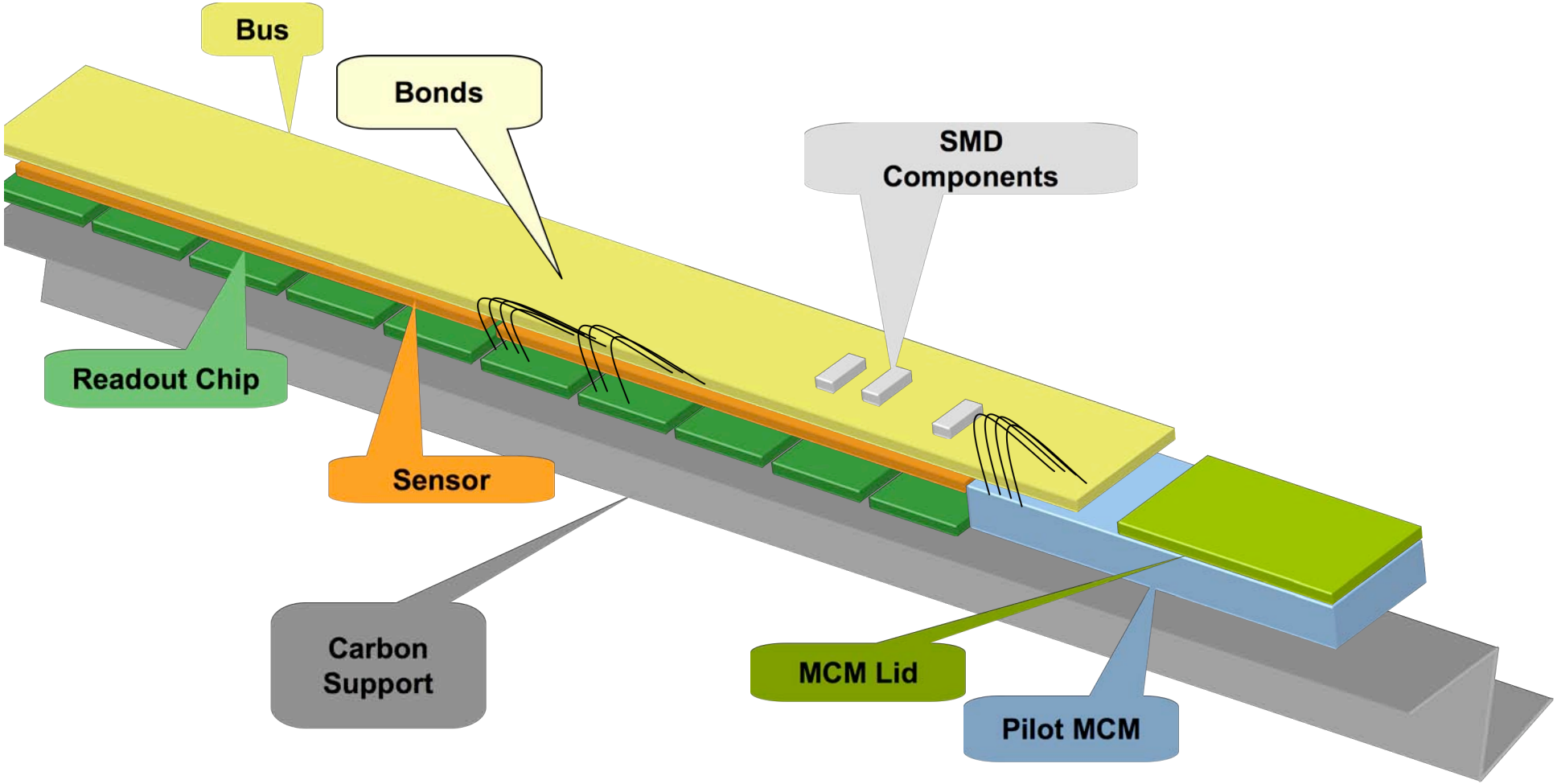
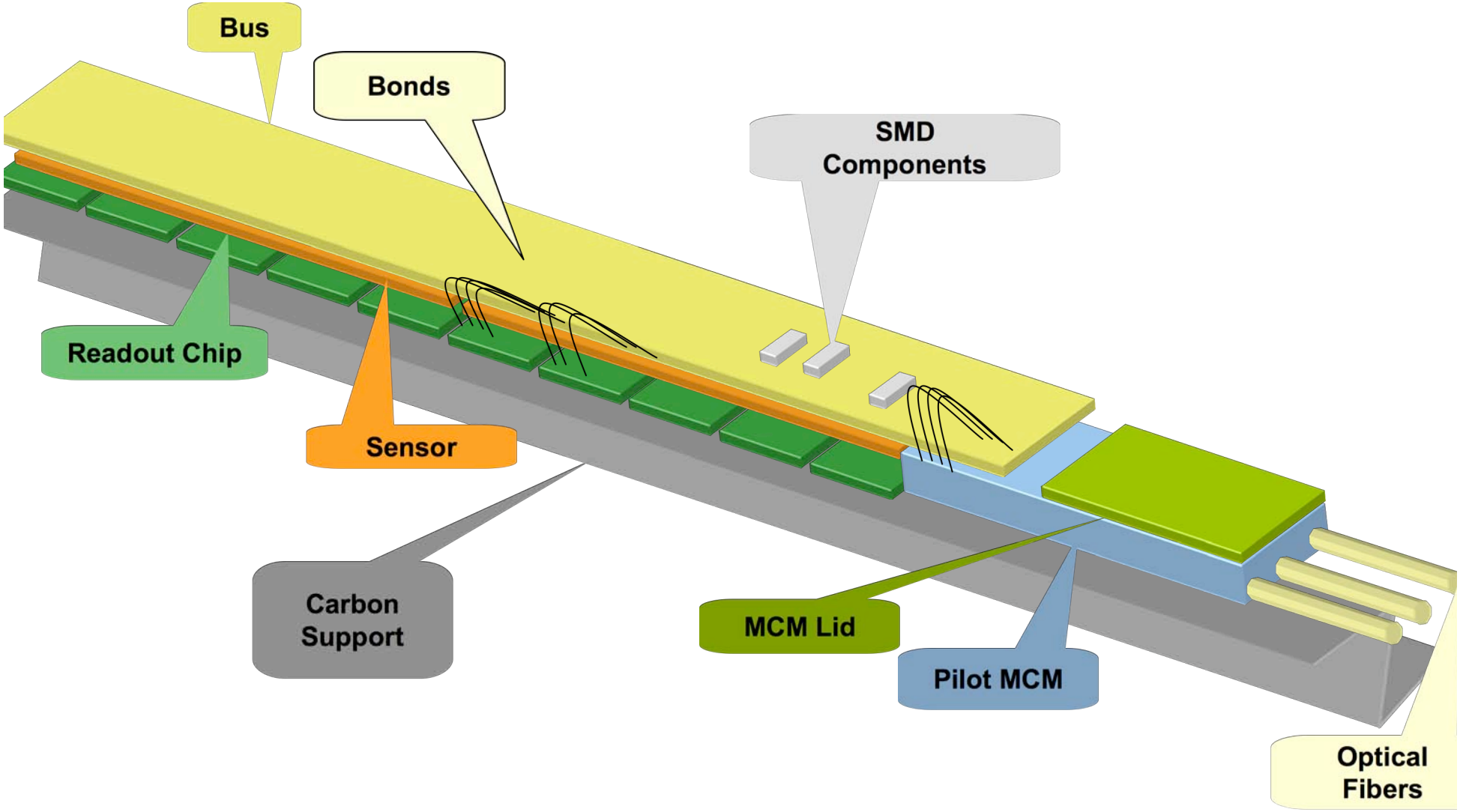


Half-Stave Components



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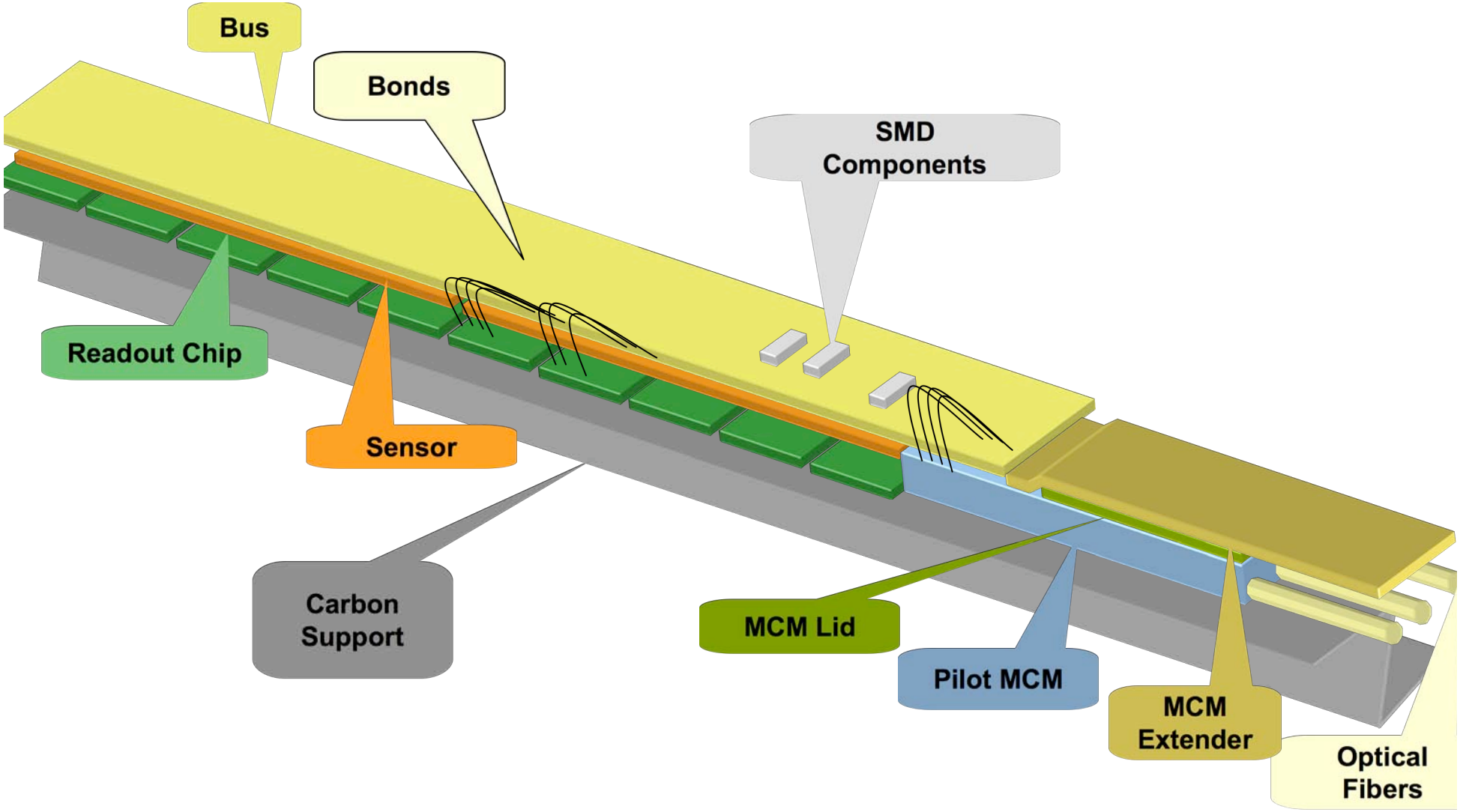

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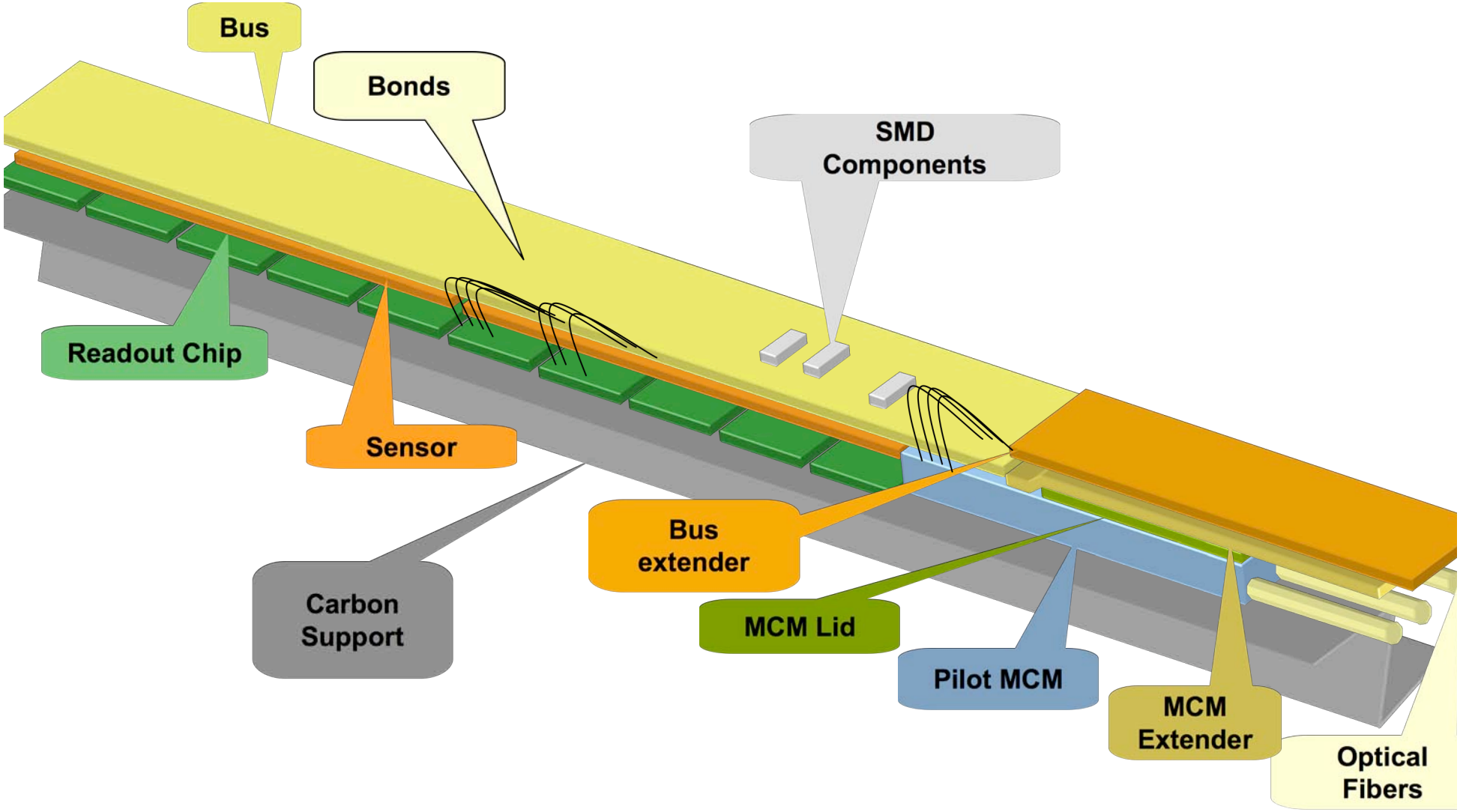
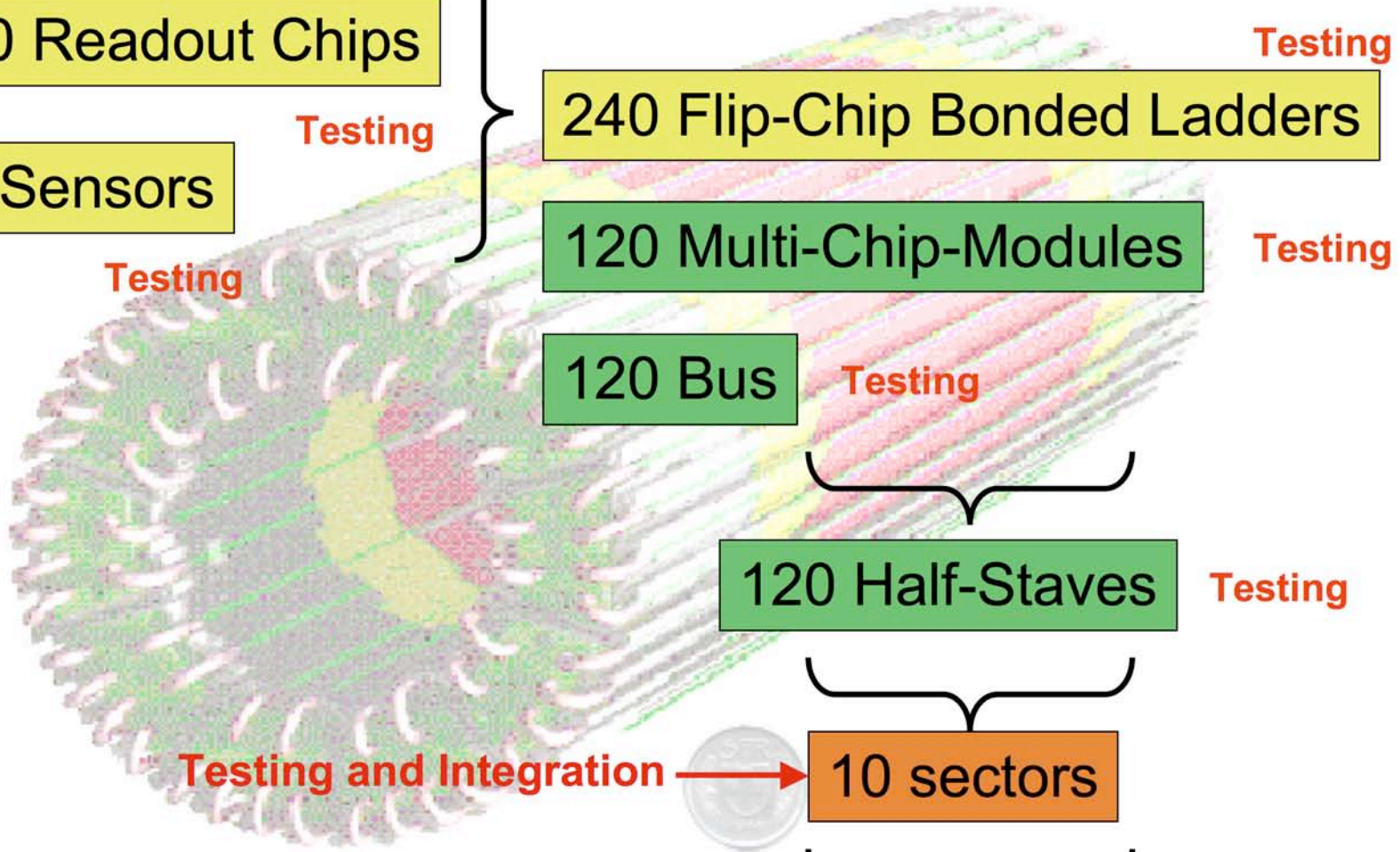
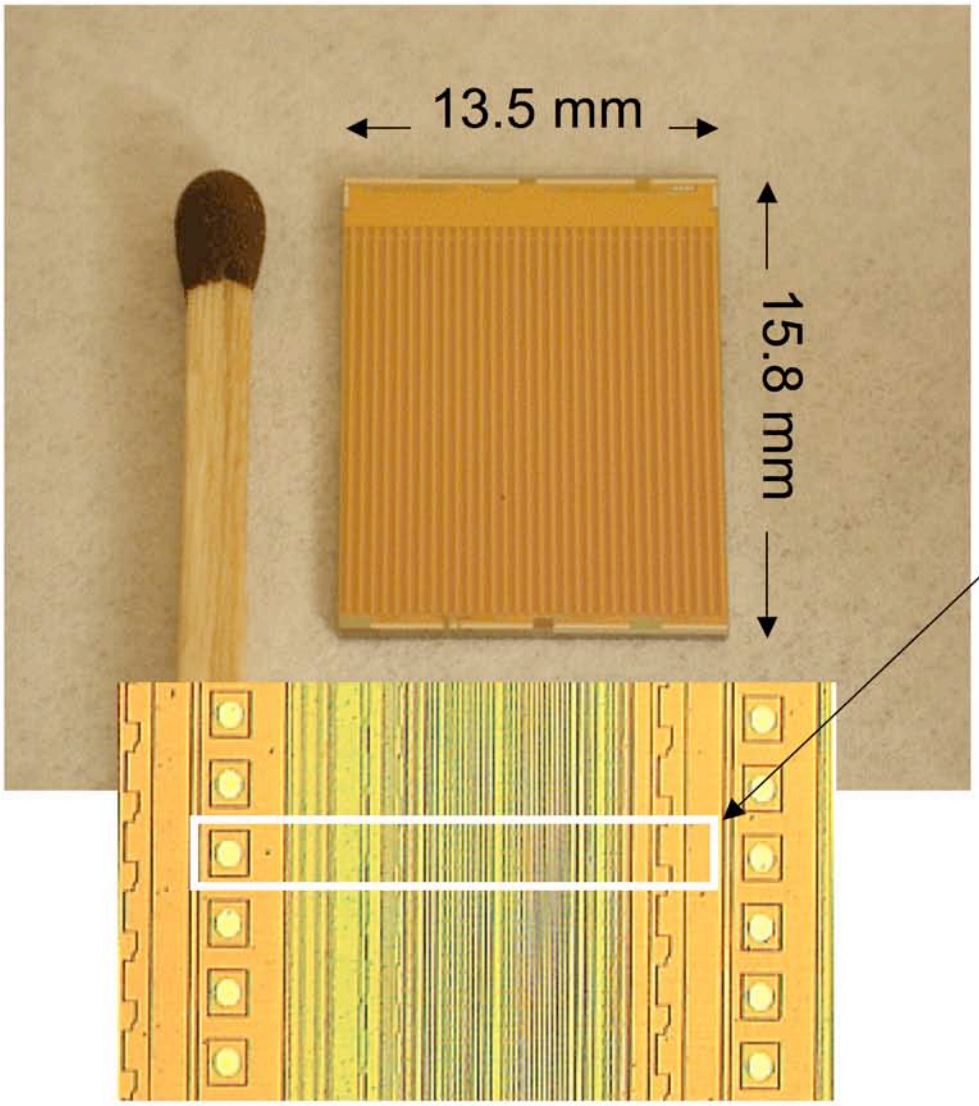


Components


1200 Readout Chips
240 Sensors
Testing
Testing
240 Flip-Chip Bonded Ladders
Testing
120 Multi-Chip-Modules
Testing
120 Bus
Testing
120 Half-Staves
Testing
Testing and Integration
10 sectors
2 Barrel Layers

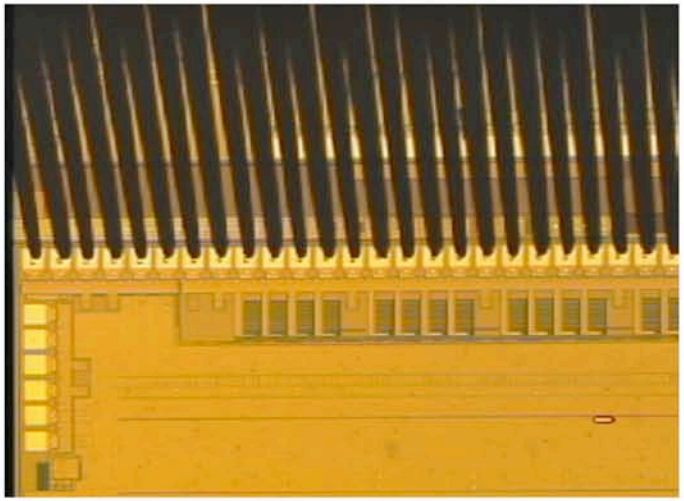
Readout Chip



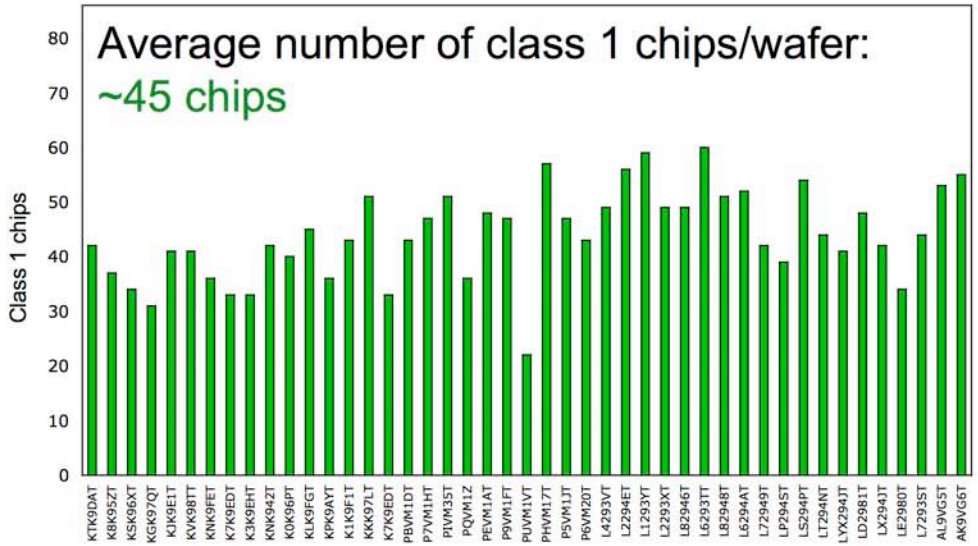
- Differential front end
- Binary synchronous readout
- Commercial 0.25μm CMOS process
- 8192 pixel cells
- 50 μm (rϕ) x 425 μm (z) pixel cell
- Configuration loading via JTAG
- FastOR output for trigger
- ~100 μW/channel
- ~1000 e^- mean threshold (~200 e^- RMS)
- ~110 e^- mean noise

Readout Chip - Tests

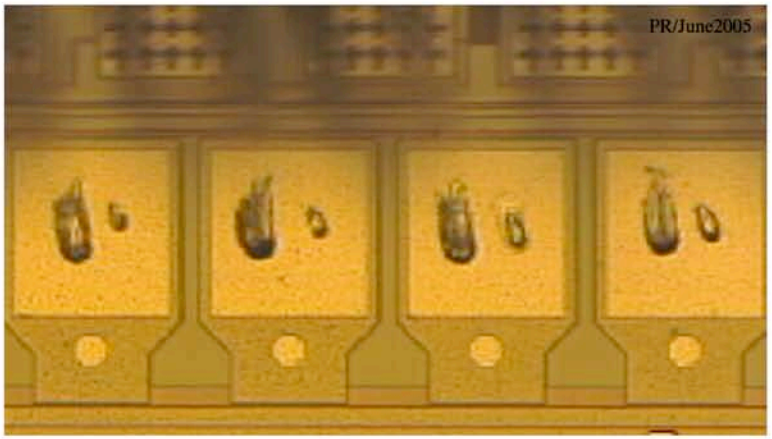
KGD - Chip Classification Scheme:
Class I: Chips for bump bonding
Class II: Minor defects
Class III: Major defects



- 86 chips/200 mm wafer
- 58 wafers (4988 chips) tested

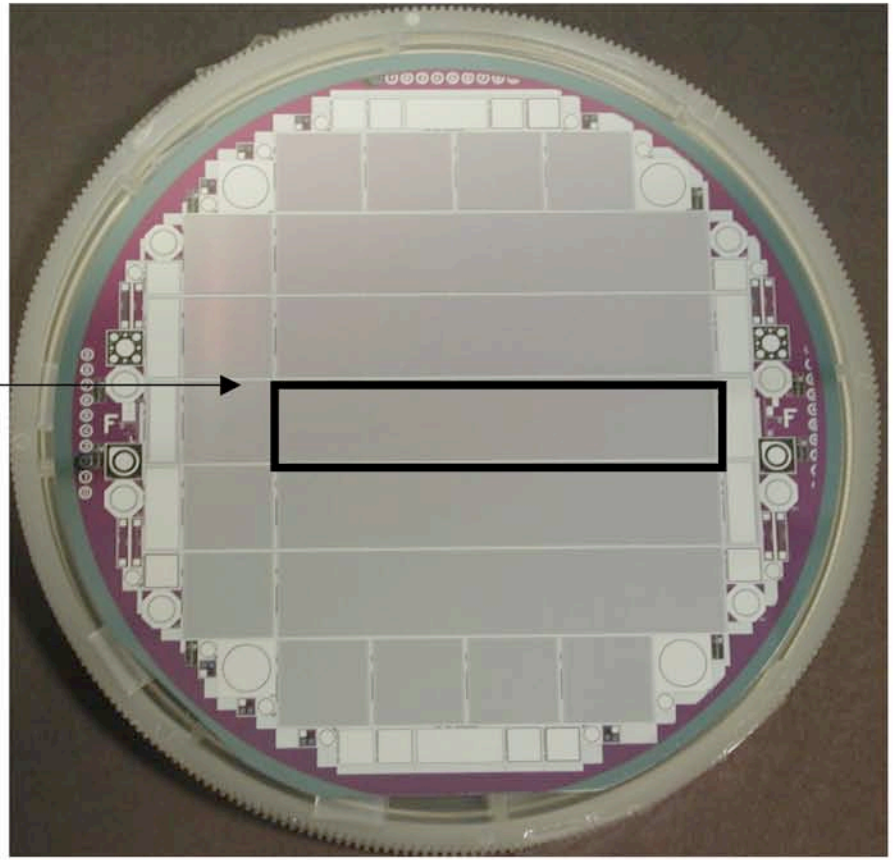


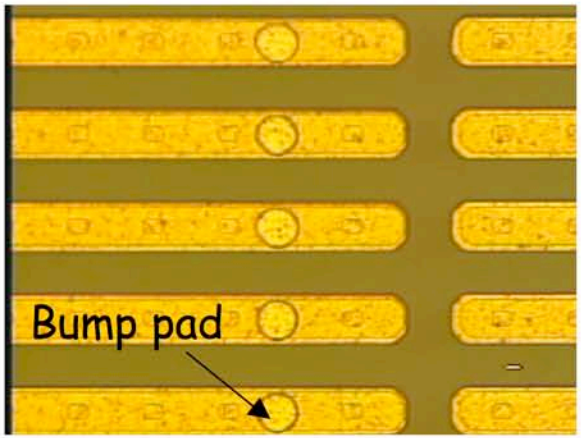
Only one contact pad for tests on the prober and for wire bonding (space constraints)



Sensor

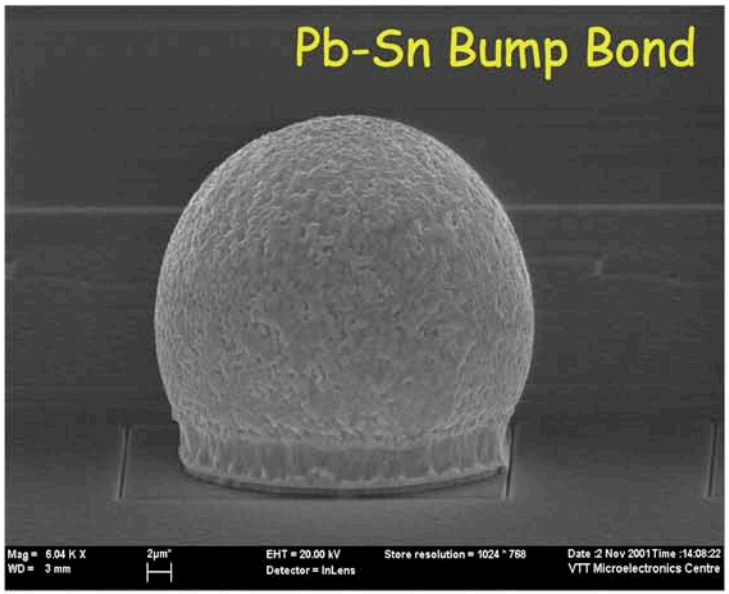
- CANBERRA p-in-n sensor
- SiO_2 passivation
- Sensor shape:
  12.8 mm x 70 mm
- Matrix:
  5 x 32 x 256 pixels
- Pixel dimensions:
  50 μm x 425 μm
  (625μm at chip junctions)
- **200 μm thick (material budget constraints)**





Pre-bonding tests:
Diode I-V, C-V
Visual inspection
~4 out of 5 sensors accepted (visual inspectio

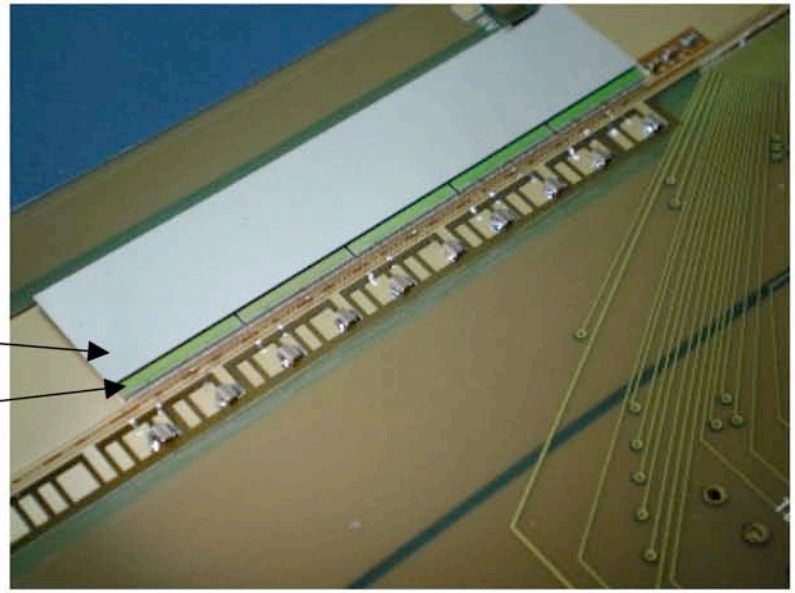
Flip Chip Bonding



- VTT/Finland
- Pb-Sn solder bumps: ~25 μm diameter
- Readout chips: 725 μm native thickness **thinned to 150 μm** after bump deposition (material budget constraints)

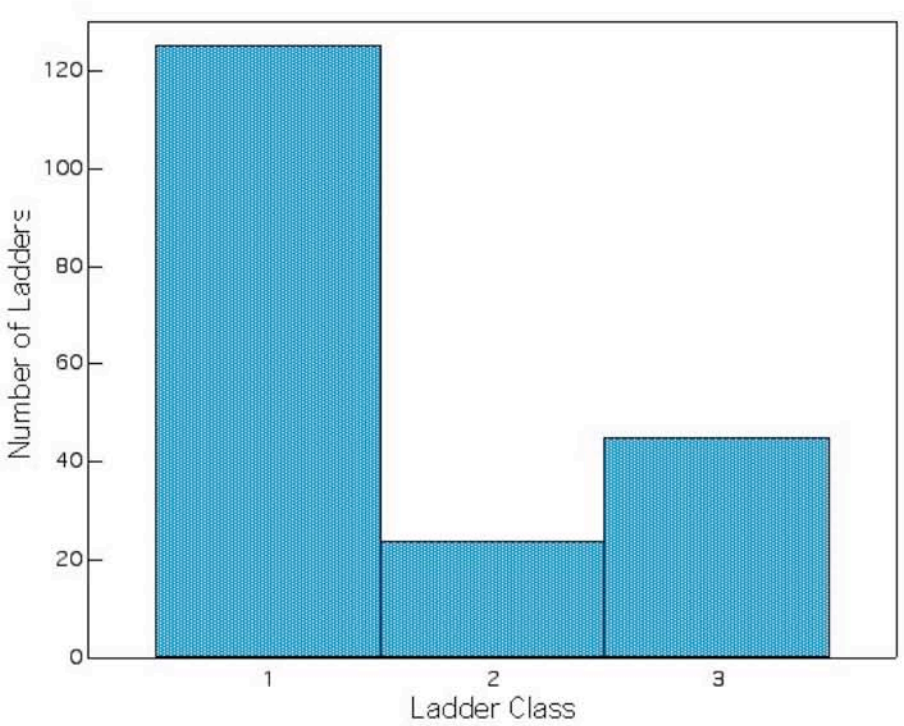
Ladder=

1 sensor
+
5 R.O. chips



Flip Chip Bonding -Testing

Testing (on PA200 probe station):
- Visual inspection
- Sensor leakage current
- Full el. test
- Source-test
- FO trigger test



Ladder classification:

Class 1: used for assembly

Class 2: back-up for assembly

Class 3: not useable

Total number of ladders tested: 194

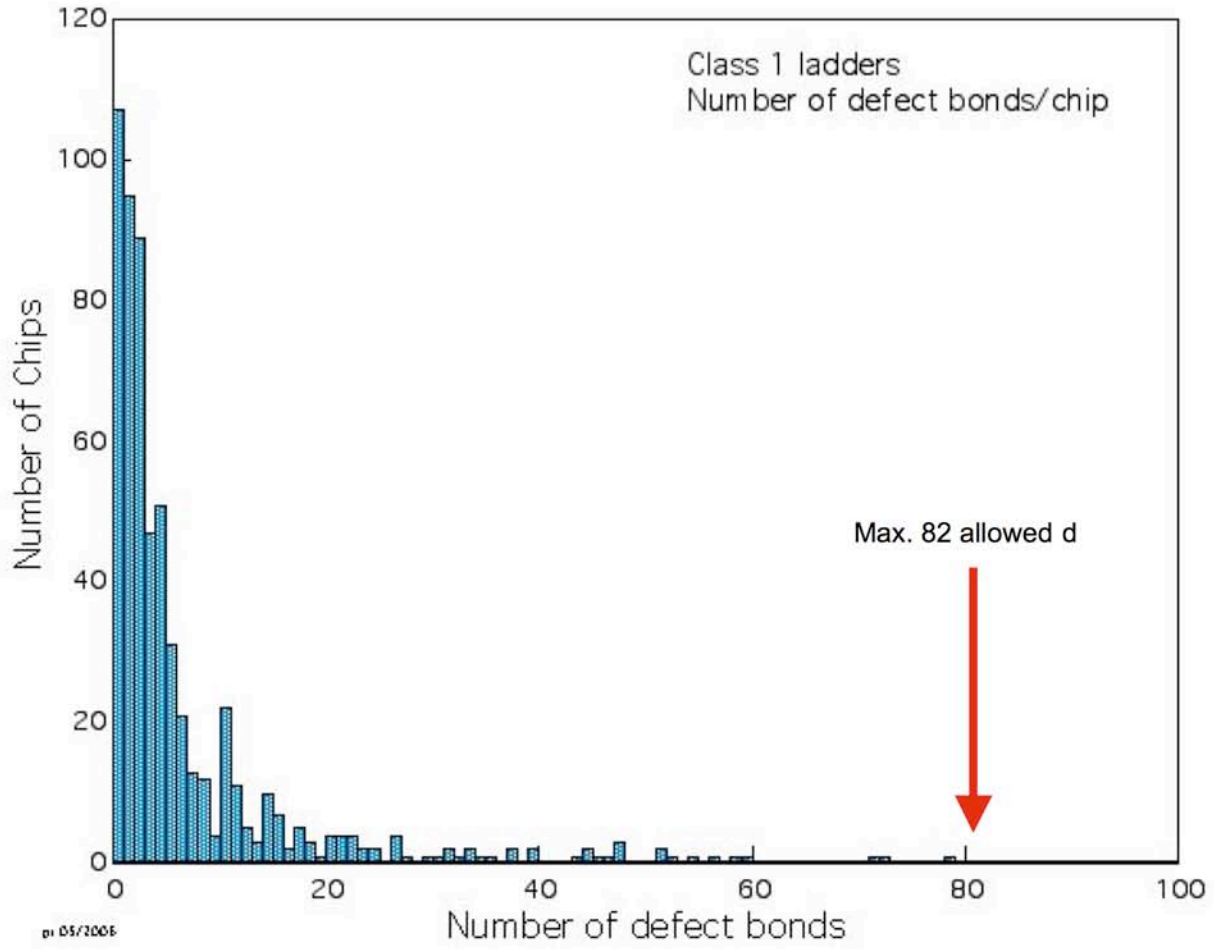
Class 1: 64%

Class 2: 12%

Class 3: 24%

Flip Chip Bonding -Testing

Class 1 ladders used for HS mounting: defects/chip (max. 1%)



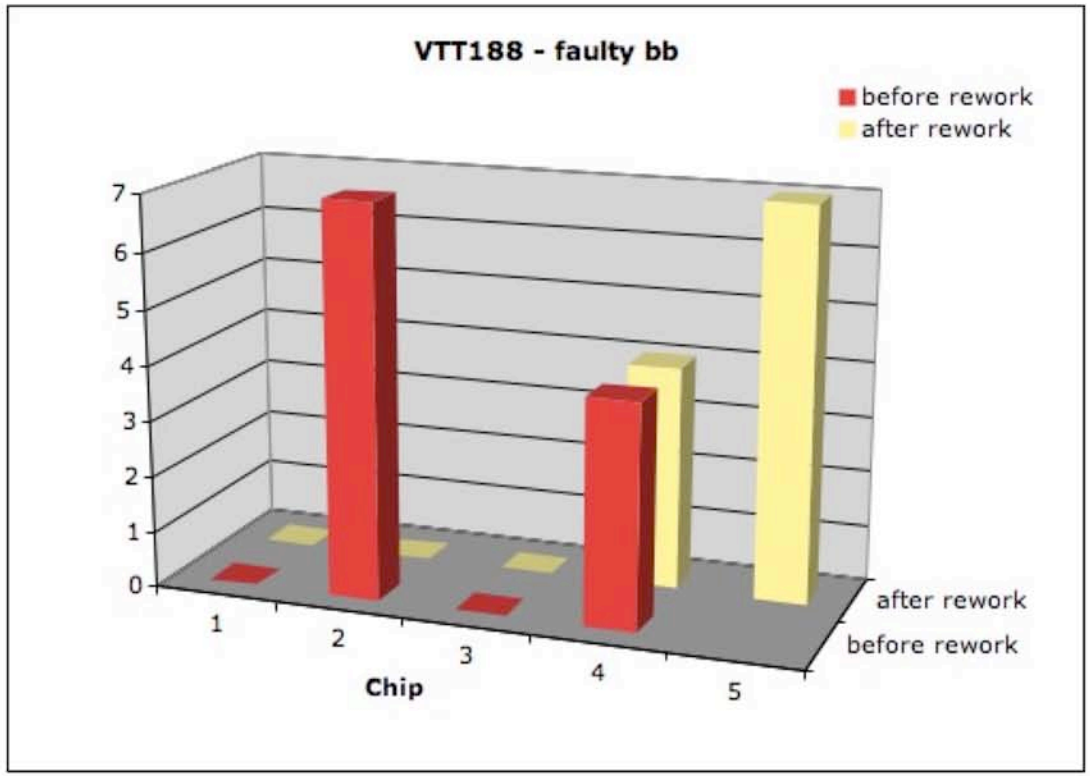
Flip Chip Bonding -Testing

Failure modes:

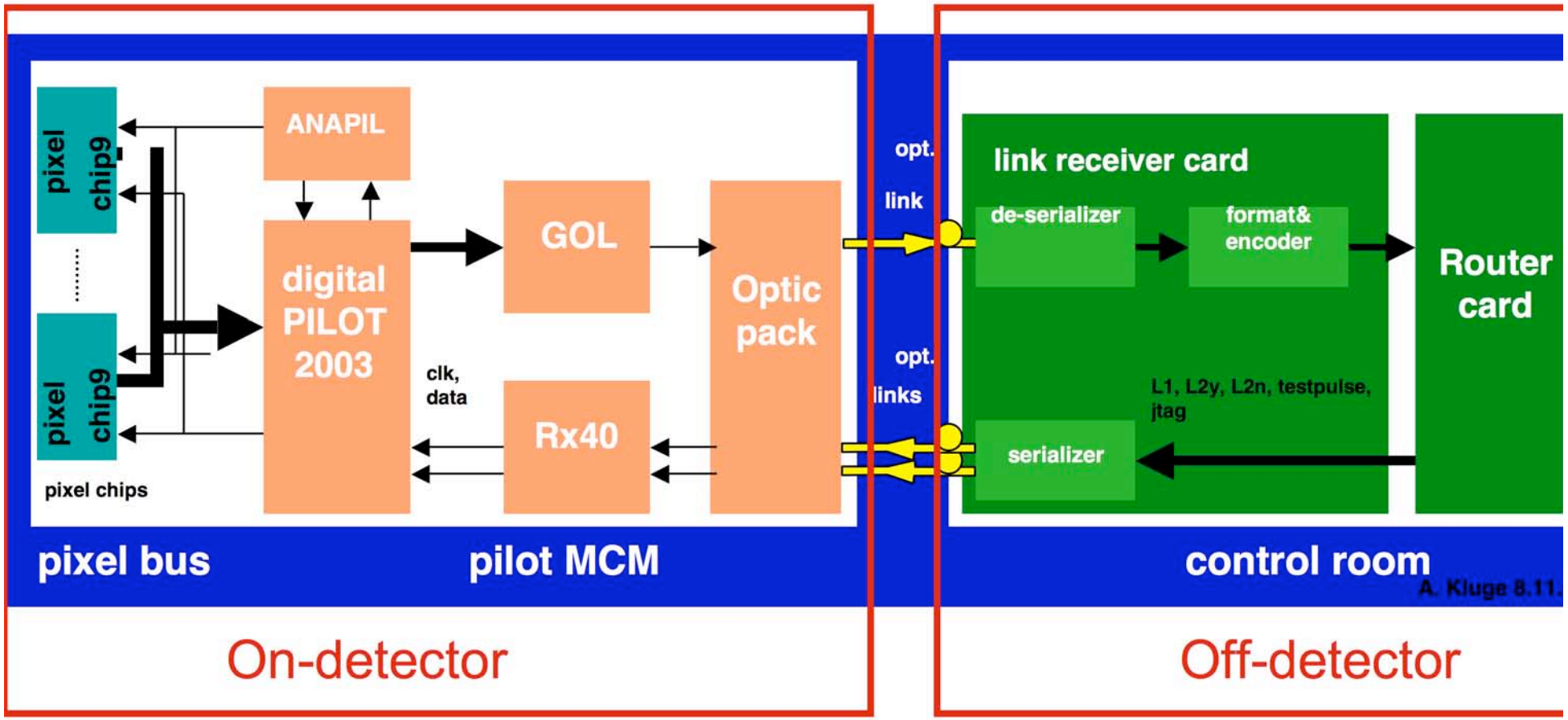
- Leakage current >2μA (26)
- Bump bonding failures >82/chip (24)
- Chip errors (22)
- Or combination of several modes

Reworking procedure:

replace individual or several chips on the ladder
(~ 80% success, but still low statistics ~20).



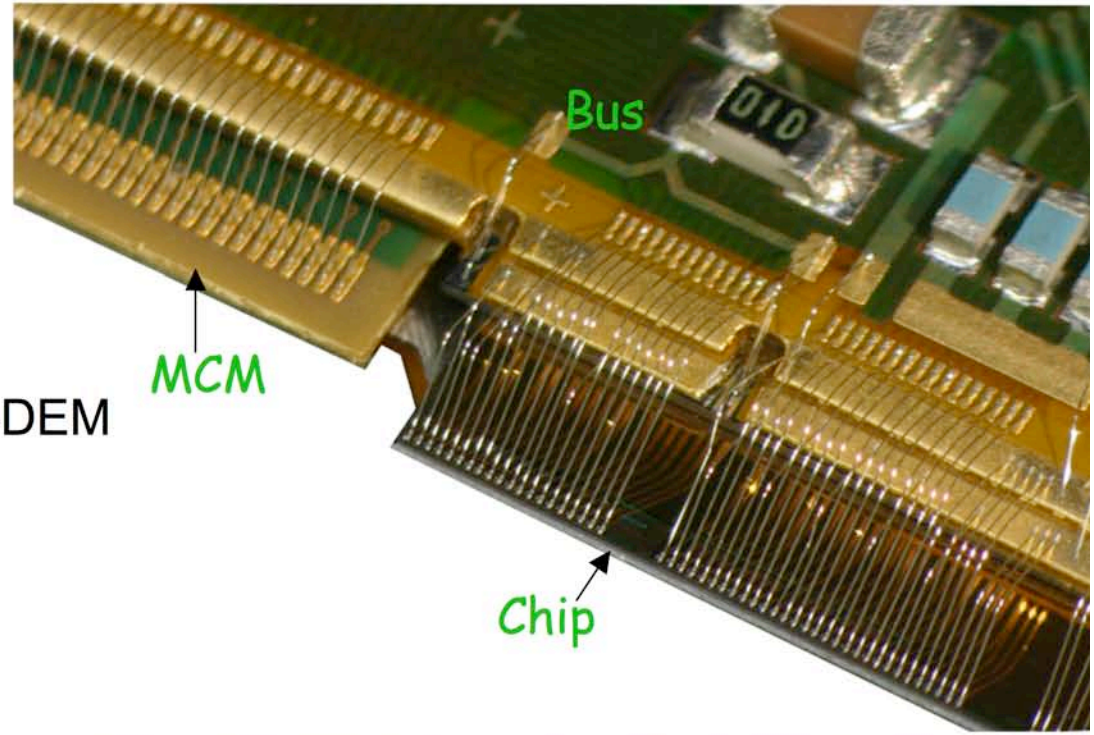
Readout System

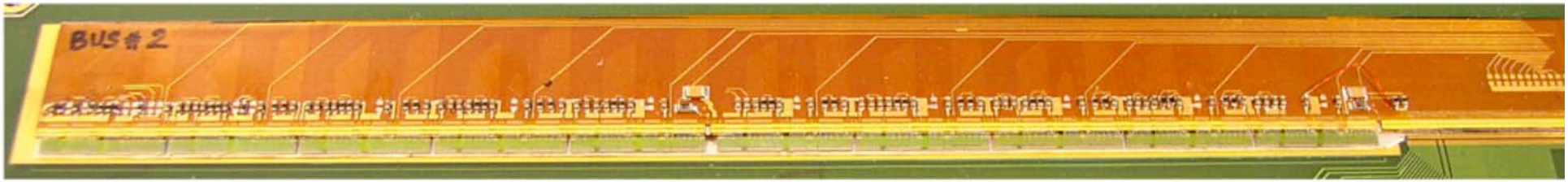


Multilayer Bus

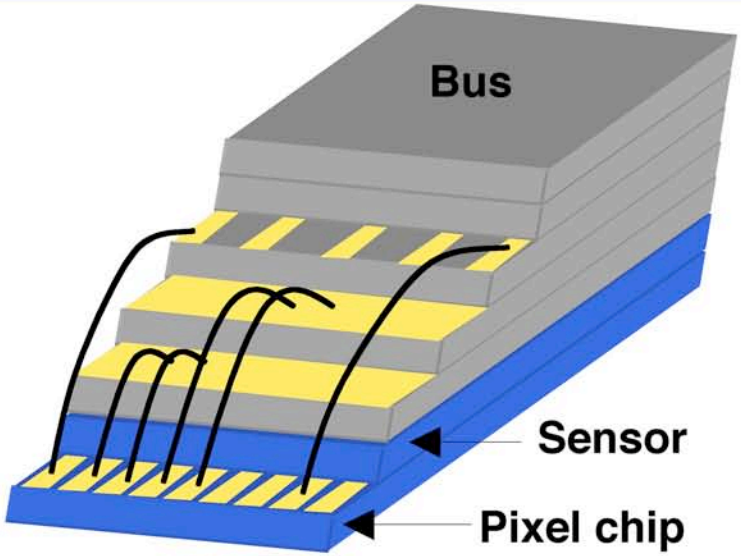
5 layer Al-Polyimide flex 240 μm thick

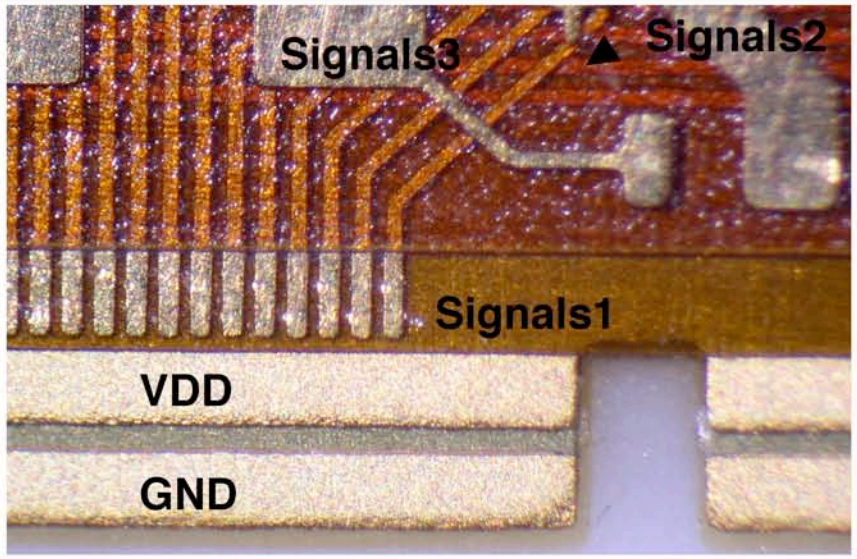
- wire bonds to the readout chips+MCM
- data, control and power-lines
- 20 cm long, 13 mm wide
- 5 layers
  (power, GND, 3 signal layers)
- **material budget: thickness, Al**
- vias for signal layers (difficult)
- developed+produced CERN TS-DEM
- ~60% of production done



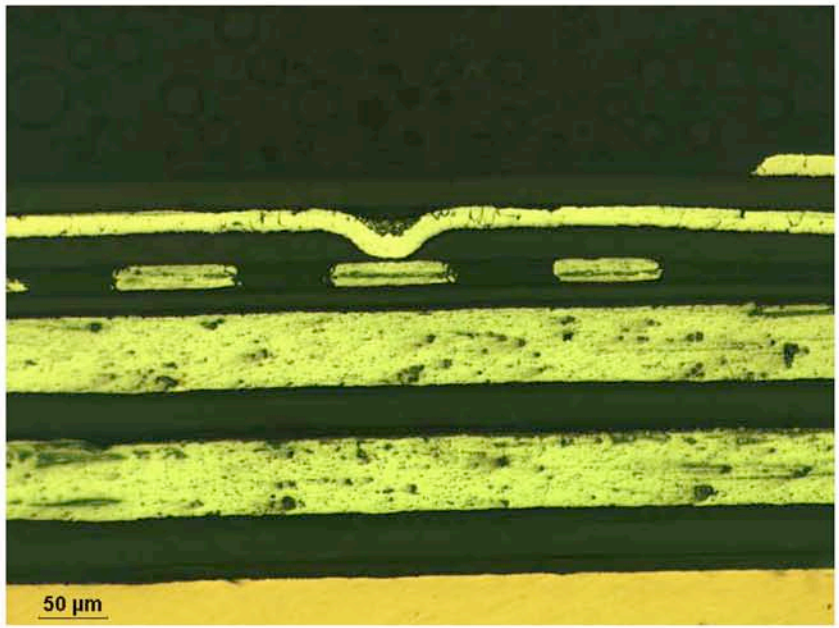


Multilayer Bus





~ 1000 wire-bonds
Tested on board before HS mounting
(temp. wire-bonding)



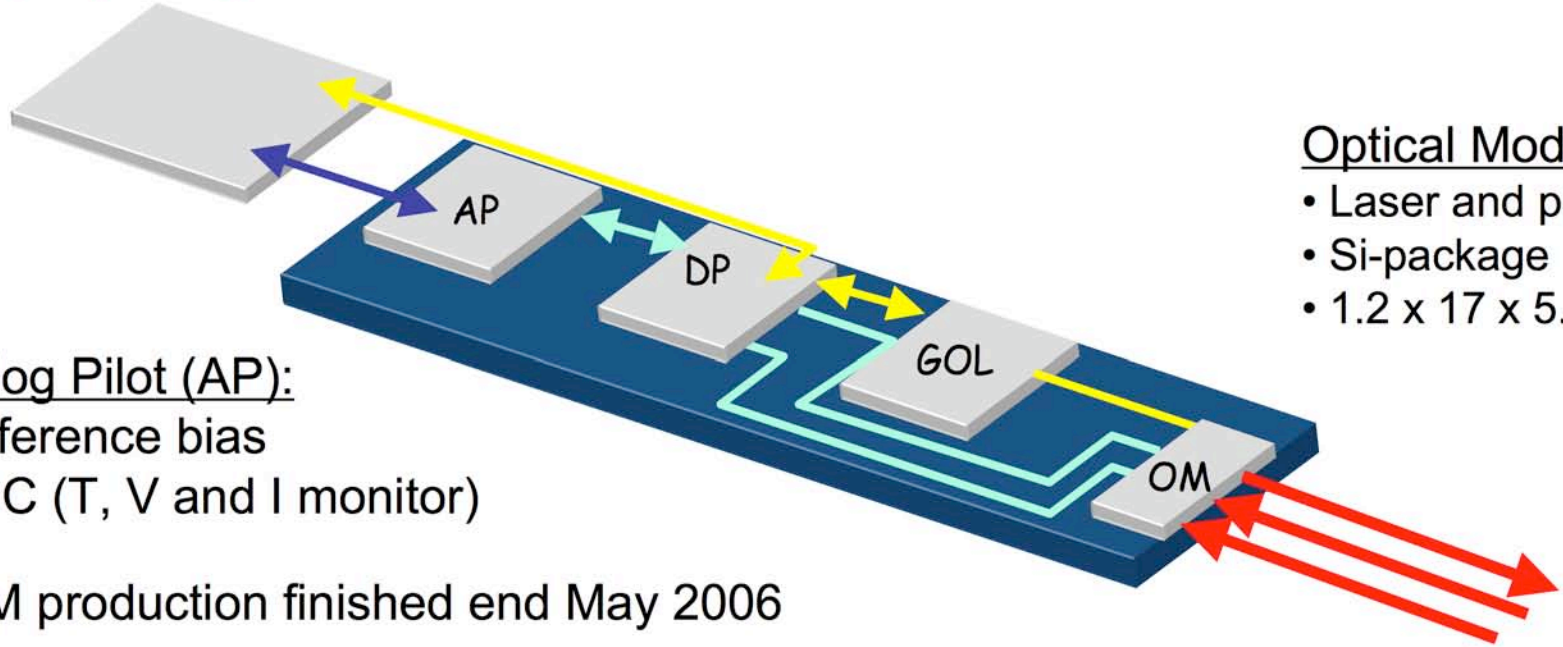
Multi Chip Module (MCM)

< 2mm thick (space constraint)

Routing (analog (10mV), digital (800MHz))

Fragile, no packages

- Digital Pilot (DP)
- GOL (Giga-bit optical link)



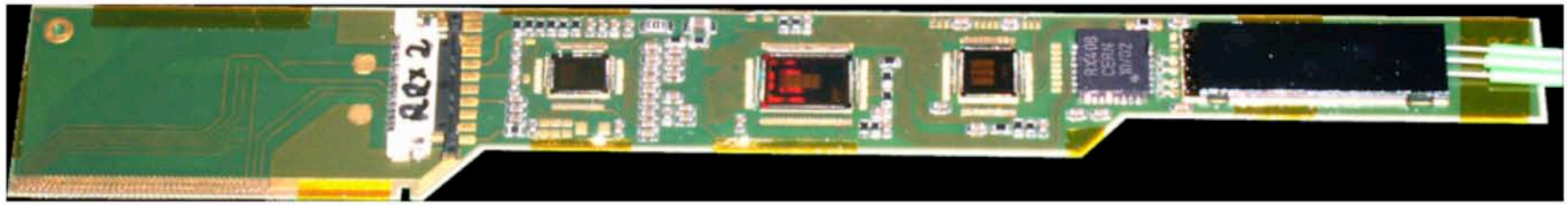
Optical Module (OM)

- Laser and pin diode
- Si-package
- 1.2 x 17 x 5.5 mm^3

Analog Pilot (AP):

- Reference bias
- ADC (T, V and I monitor)

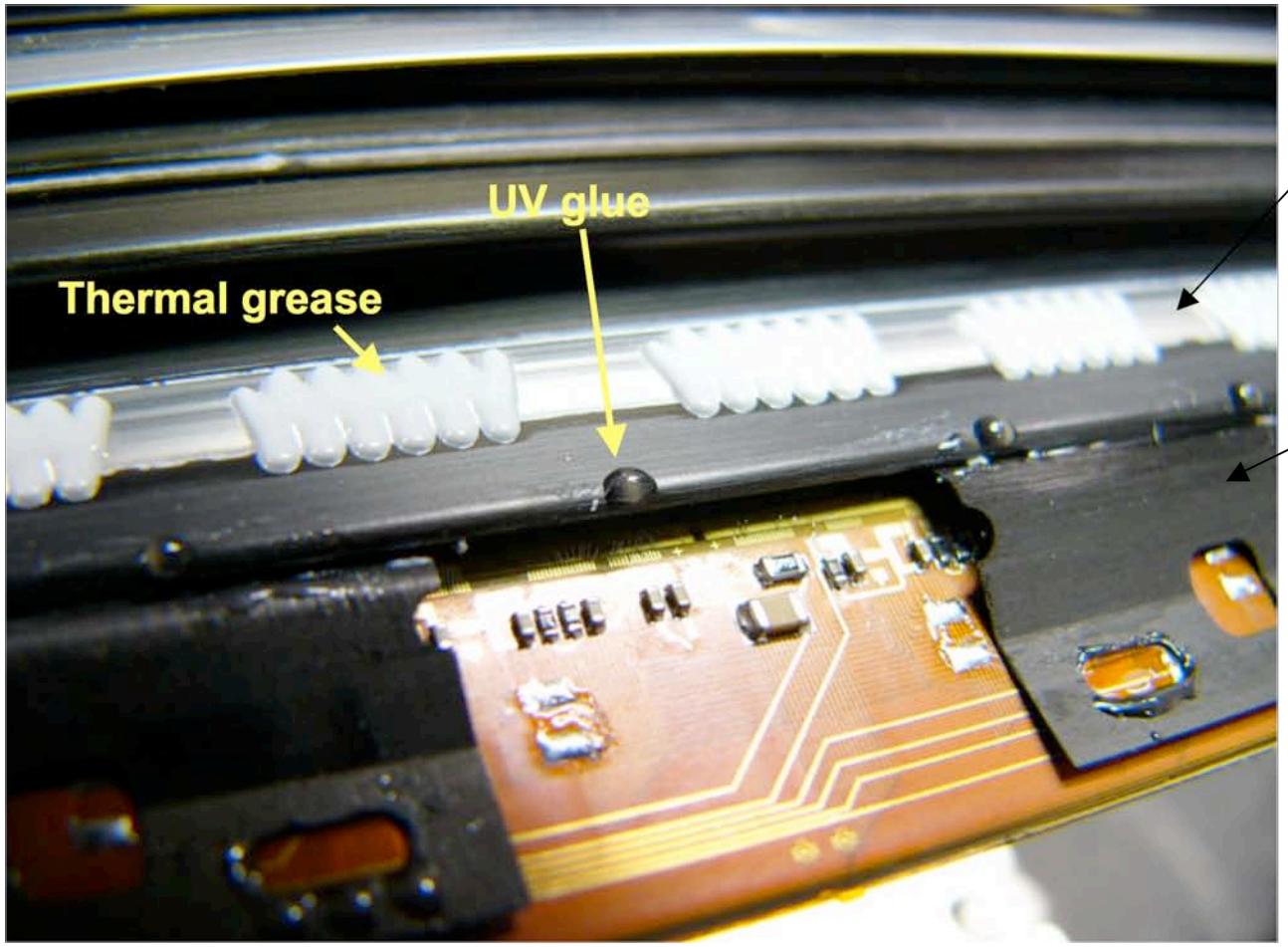
MCM production finished end May 2006



Sector Assembly

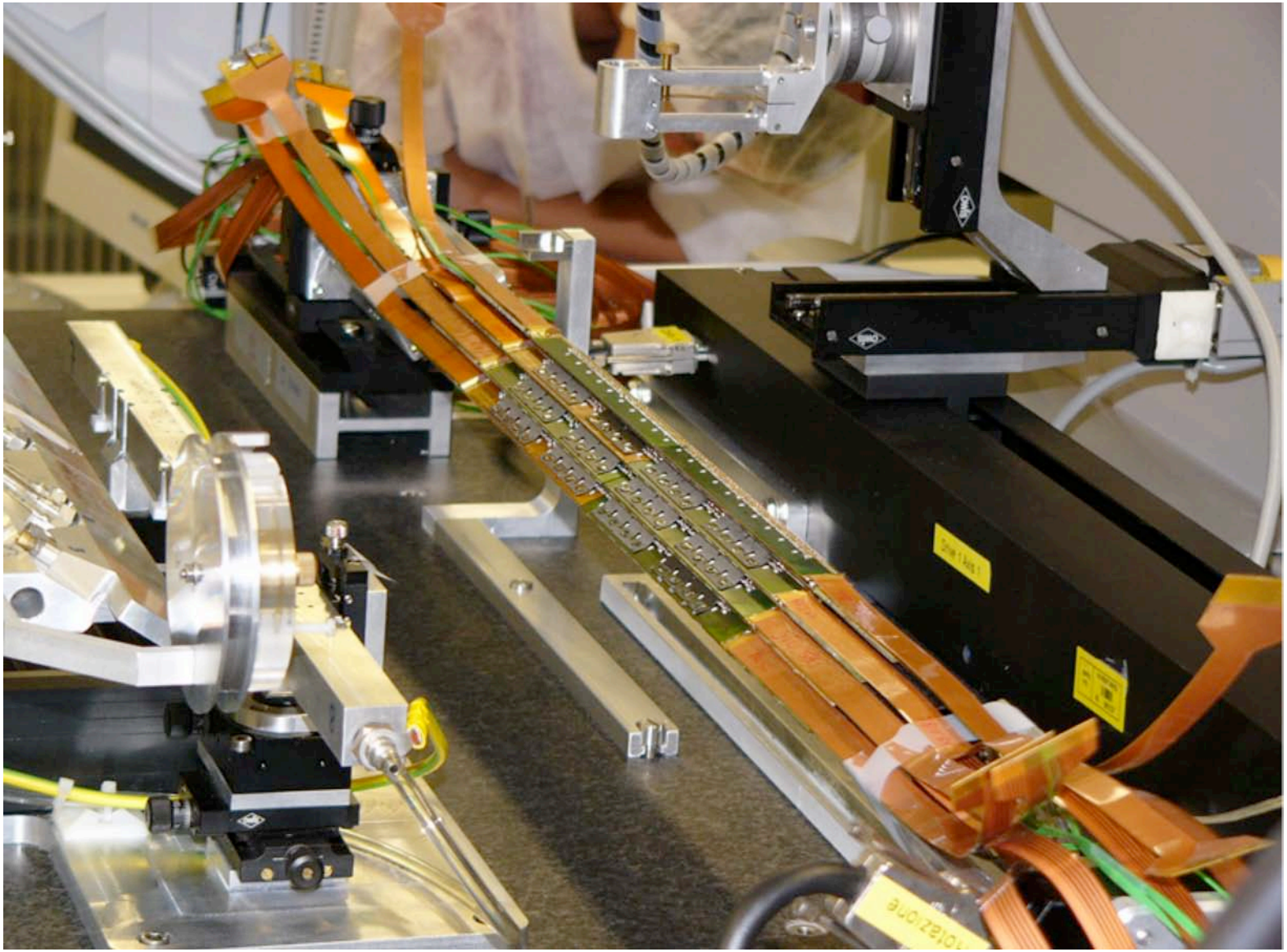
Mounting on the CF sectors in INFN Padova/LNL:

- Thermal grease underneath the chips (coupling to cooling tubes)
- UV-glue drops and CF clips to fix the HS position



Sector Assembly

Sector Assembly



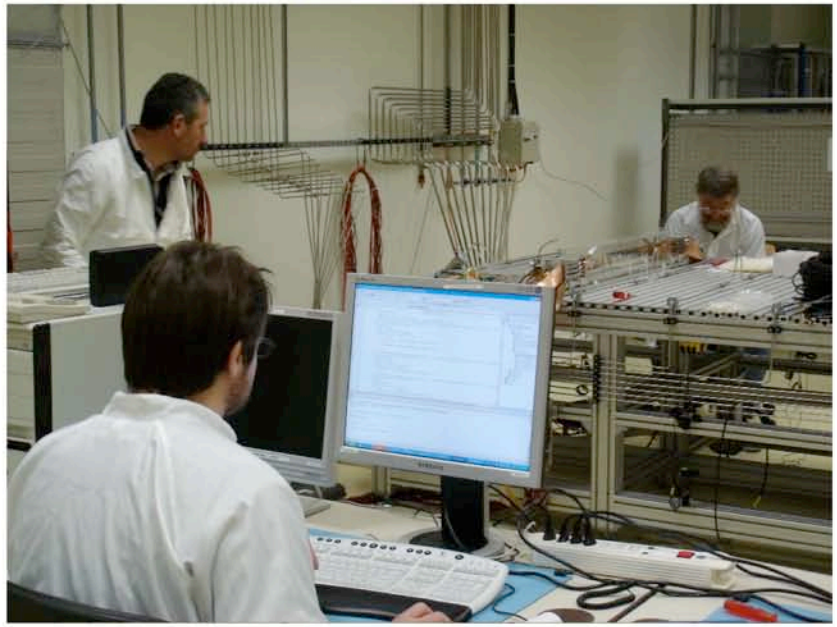
Integration

Test of each sector in the Divisional Silicon Facility (DSF) at CERN

- Class 100.00 cleanroom

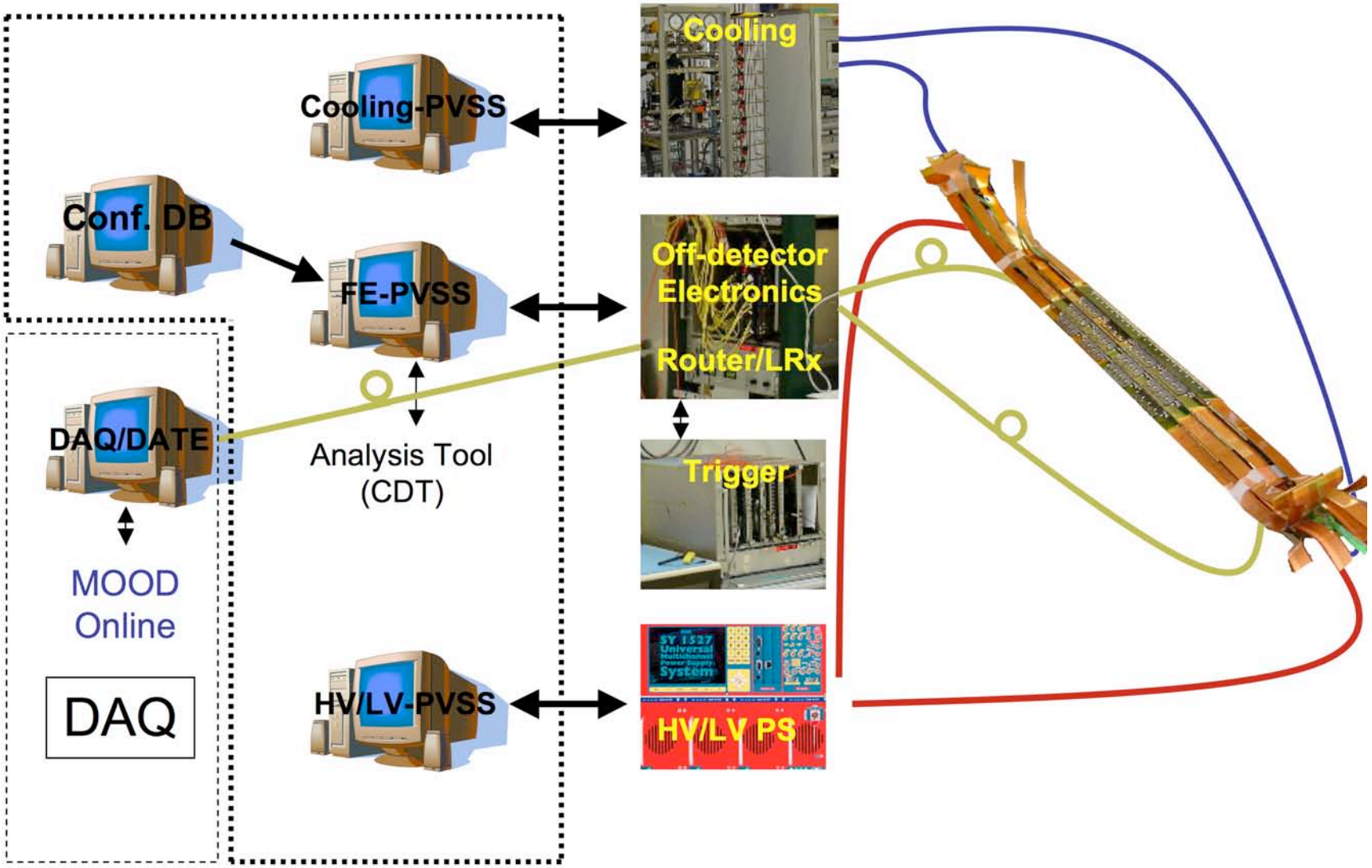
Qualify each sector before 5 sectors are mounted together
>>Detector will be mounted as two half-shells (5 sectors) around the beam-pipe

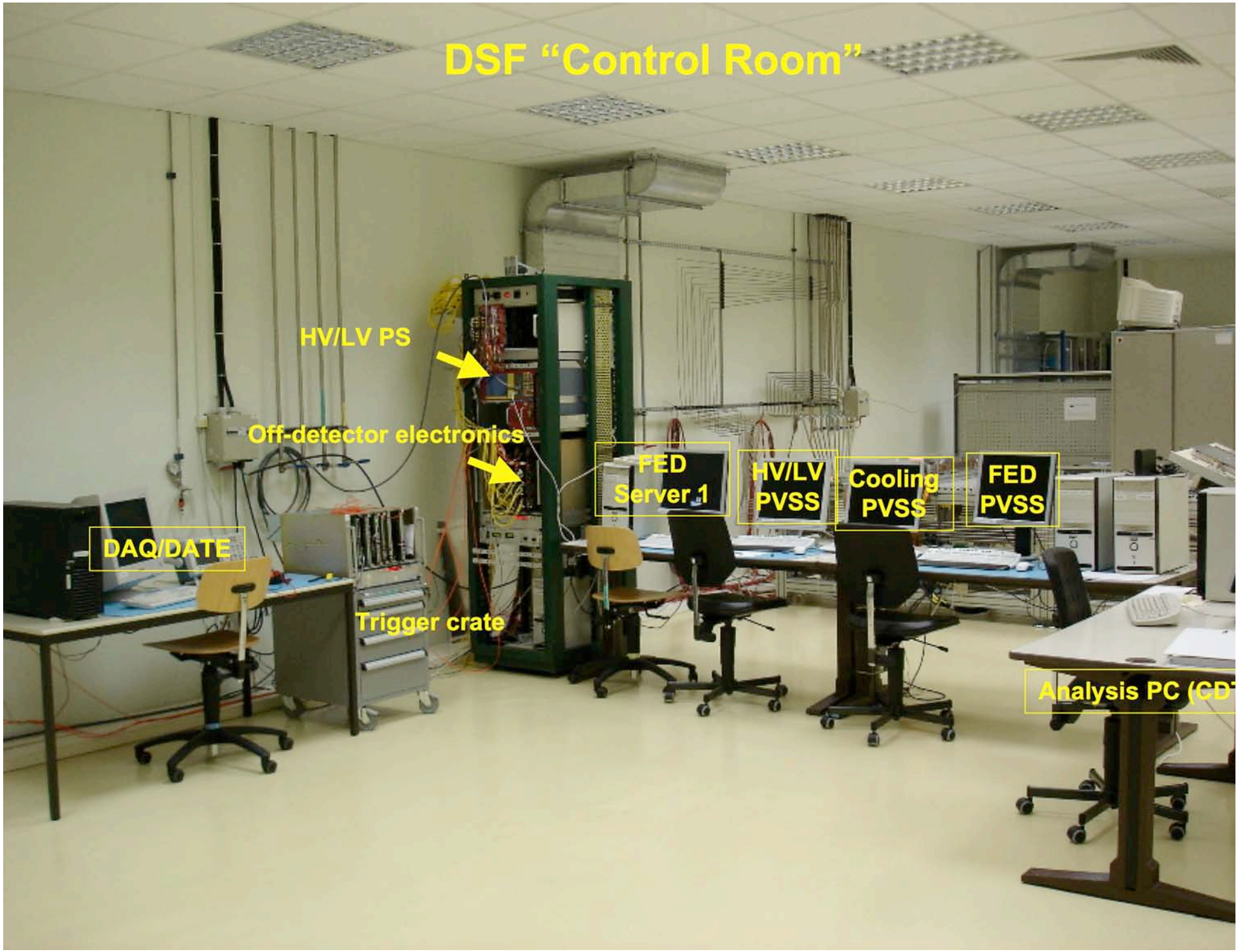
⇒Test of **final cooling system**
⇒Test of **DCS and interlocks**
⇒Test of **final cables** (30 m LV, 100 m HV)
⇒Test of **final power supplies**
⇒Test of **off-detector electronics**
⇒ ALICE **trigger modules**
⇒ ALICE **DAQ system and online monitoring**
⇒Test of **calibration procedure** in the ALICE framework



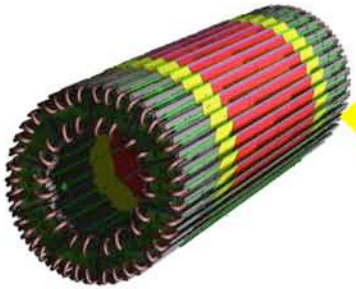
Goal: check every component before it is moved to the pit.

Integration




DSF “Control Room”
HV/LV PS
Off-detector electronics
FED Server 1
HV/LV PVSS
Cooling PVSS
FED PVSS
DAQ/DATE
Trigger crate
Analysis PC (CD

Integration - Data and Control



Data & Ctl

OFF-DETECTOR ELECTRONICS

(Routers & LinkRxs)

Data

ALICE DAQ

(AliRoot)

Comm. & Ctl

Data

Data

MOOD

Optical

VME

Ethernet (DIM)

FED Server

Comm & Status

Data

ANALYSIS TOOLS

DB

PVSS

I.A. Cali

Integration - Online Monitoring

-Develop software within ALICE framework
-Hit displays
- Data format consistency checks

H. Tydesjö

Integration

- 3 sectors mounted and being tested (30% of detector)
- Integration tests proved to be very useful in many aspects:
  Cabling, software, training, test procedures,…
- Mounting of first detector half-shell foreseen this summer
- Installation of the detector in the experiment: end of this year

FastOr Trigger

• Prompt FastOR pulse generated in each chip on detection of one (or more) pixel hits

•FastOR data embedded in outgoing data stream on optical fibre (800Mb/s)

•Extraction via fibre optic splitters at CTP (central trigger processor) location

•Multiplicity trigger, minimum bias (pp), event topology

Implementation presented at FEE Perugia, May 17-20, 2006 (A.Kluge)

Summary

- SPD : the two innermost layers of of the ALICE inner tracker.
- ~ 10^7 pixel cells of 50 μm (rϕ) x 425 μm (z).
- Severe constraints in material budget and device packaging.
- Testing at every component level.
- Integration and commissioning of the first 3 sectors is well advanced.
- Contribution to L0 trigger (multiplicity).
- Installation in the experiment currently scheduled end 2006.