CMOS Sensors for an ILC Vertex Detector

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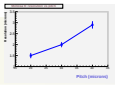
OUTLINE

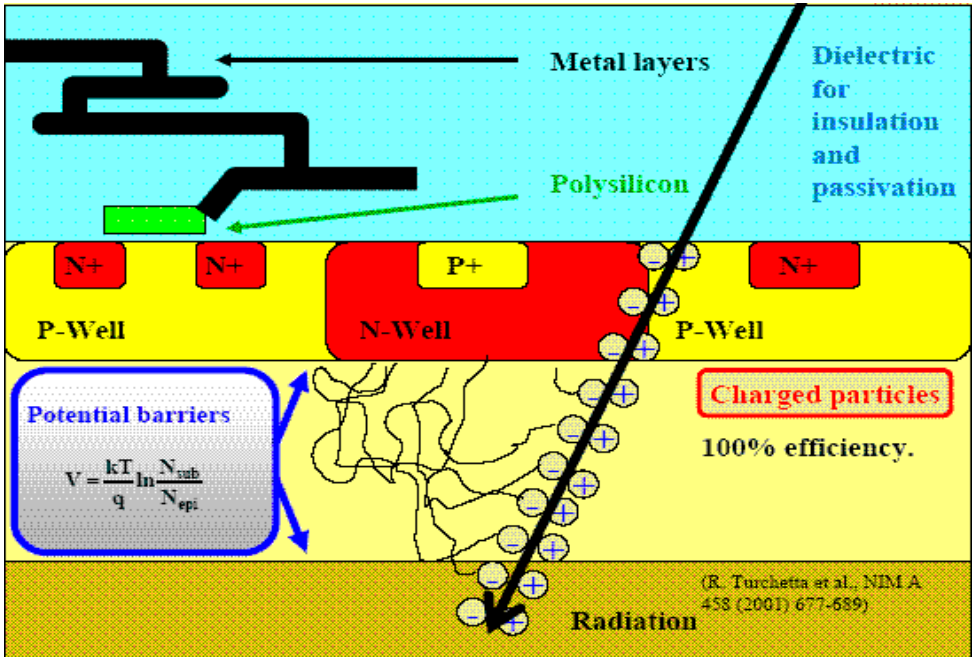
- **Introductory remarks on CMOS sensors:**
  - **Specific advantages**
  - **Main R&D directions**
  - **Teams involved**
- **Achieved performances :**
  - **S/N**
  - **Detection efficiency**
  - **Single point resolution**
  - **Thinning**
  - **Radiation tolerance**
  - **Read-out speed**
  - **Power dissipation**
  - **Operating temperature**
- **Main ILC VD requirements $\longrightarrow$ remaining R&D needs $\longrightarrow$ Plans for 2006 – 2009**
- **Summary**



MAIN FEATURES OF CMOS SENSORS

Main Features and Advantages of CMOS Sensors

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 80 e-h / μm $\mapsto$ signal $\lesssim$ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)



- Specific advantages of CMOS sensors:
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\lesssim$ 30 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation

Main R&D Directions

- **High r.-o. speed, low noise, low power dissip., highly integrated signal processing architecture:**
  - ※ analog part (charge collection, pre-amp, CDS, ...) inside pixel
  - ※ mixed (ADC) and digital (sparsification) micro-circuits integrated inside pixel or aside of active surface

- **Optimal fabrication process:**
  - ※ epitaxial layer thickness
  - ※ number of metal layers
  - ※ yield
  - ※ (dark current)
  - ※ cost
  - ※ life time of process

- **Radiation Tolerance:**
  - ※ dark current
  - ※ doping profile
  - (※ latch-up)

- **Room temperature operation:**
  - ※ minimise cooling requirements
  - ※ performances after irradiation

- **Industrial thinning procedure:**
  - ※ minimal thickness
  - ※ mechanical prop.
  - ※ individual chips rather than wafers
  - ※ yield

CMOS Sensor "Community"

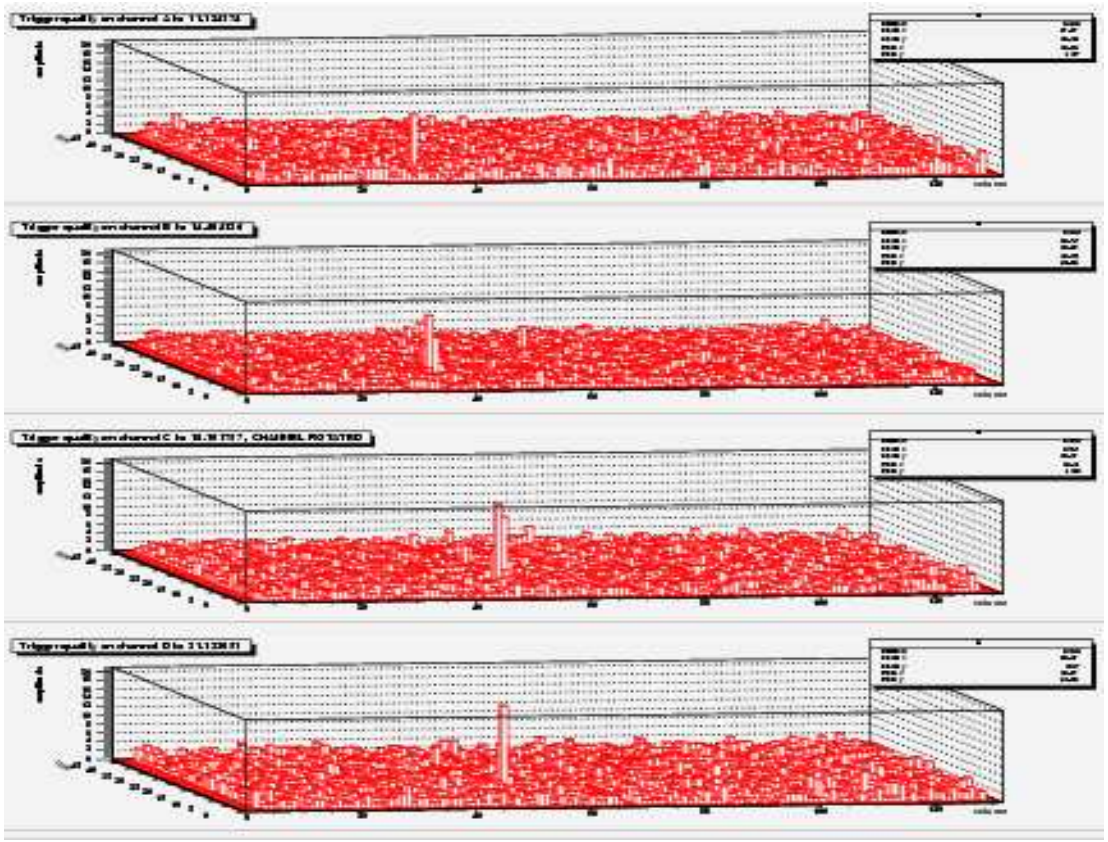
- **Several groups design CMOS sensors for charged particle tracking :**

  - **BELLE upgrade ⟼ SuperBELLE:**
    Univ.Hawaï

  - **STAR upgrades:**
    IReS/IPHC (Strasbourg)

  - **ILC (EUDET ⊂ E.U. FP-6):**
    IReS/IPHC (Strasbourg), DAPNIA (Saclay), LPC (Clermont), LPSC (Grenoble), Univ. Roma-3, Univ. Bergamo, Univ. Pavia, Univ. Pisa, RAL, LBL, BNL, Univ. Oregon & Yale (SARNOF), others (?)

  - **CBM (GSI):**
    IReS/IPHC (Strasbourg)



R&D for Super BELLE: hits in 1st beam telescope made of 4 CAP-2 sensors exposed to 4 GeV/c π^- (KEK)

- **Several additional groups involved in chip characterisation & detector integration issues :**
  DESY & Univ.Hamburg, GSI, Univ.Frankfurt, LBL-STAR, Univ. Geneva, INFN: Como, Milano, Roma-3, etc.

M.I.P. TRACKING PERFORMANCES:

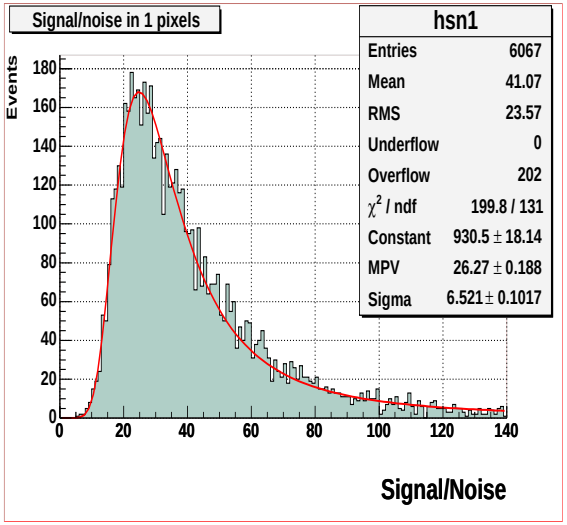
PIXEL & CLUSTER CHARACTERISTICS,

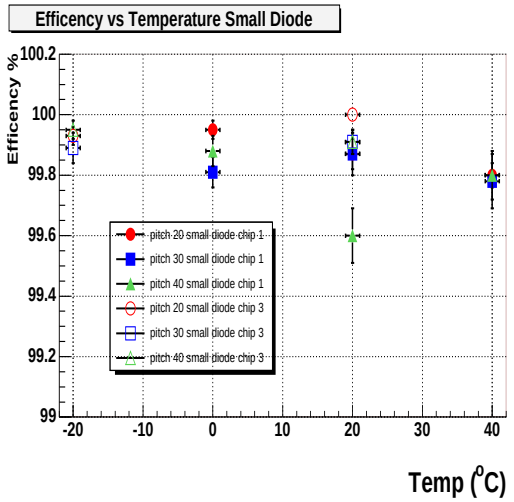
DETECTION EFFICIENCY

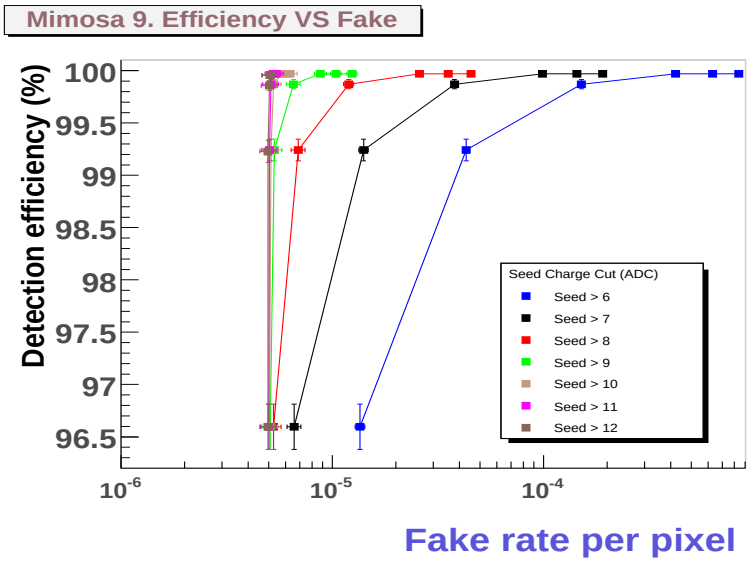
Detection Efficiency

Several MIMOSA chips tested on H.E. beams (SPS, DESY) $\mapsto$ well established performances :

- **Best performing technology: AMS 0.35 μm OPTO**
  (11–12 μm epitaxy $\rightarrowtail$ "20 μm" option tests in Fall'06)
- **N $\sim$ 10 e$^-$ $\mapsto$ S/N $\gtrsim$ 20 – 30 (MPV) $\Rrightarrow$ ϵ_{det} $\gtrsim$ 99.5 %**
- **T$_{oper.}$ $\gtrsim$ 40 °C**
- **Technology without epitaxy also performing well :**
  very high S/N but large clusters (hit separation $\searrow$)
- **Macroscopic sensors : MIMOSA-5 ($\sim$ 3.5 cm^2; 1 Mpix)**
  and CAP-3 (0.3 x 2.1cm^2; 120 kpix) for BELLE







Efficiency vs rate of fake clusters :

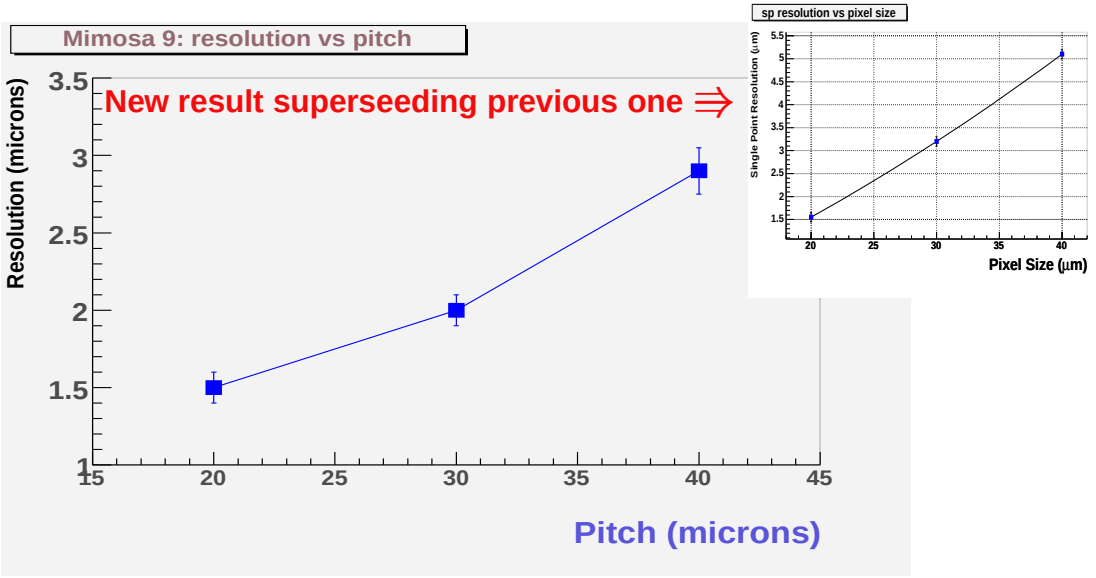
- **vary cut on seed pixel : 6 $\rightarrowtail$ 12 ADC units**
- **vary cut on Σ of crown charge : 0, 3, 4, 9, 13, 17 ADC units**

$\Rrightarrow$ **ϵ_{det} $\sim$ 99.9 % for fake rate $\sim$ 10^{-5}**

Spatial Resolution

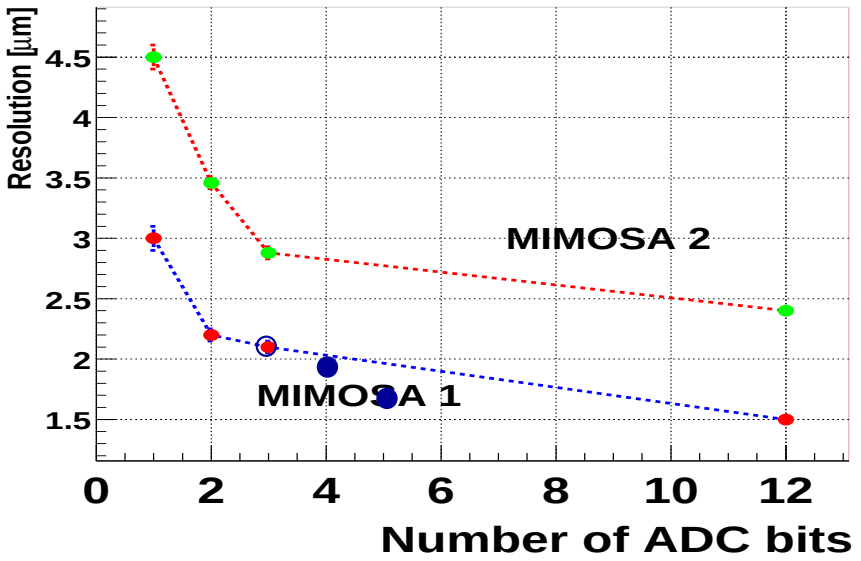
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
  $\longmapsto \sigma_{sp} \lesssim 3\ \mu m$ (40 μm pitch)



σ_{sp} dependence on ADC granularity:

- minimise number of ADC bits
  $\longmapsto$ minimise dimension and power dissipation
- effect simulated on real MIMOSA data
  (20 μm pitch ; 120 GeV/c π^- beam)

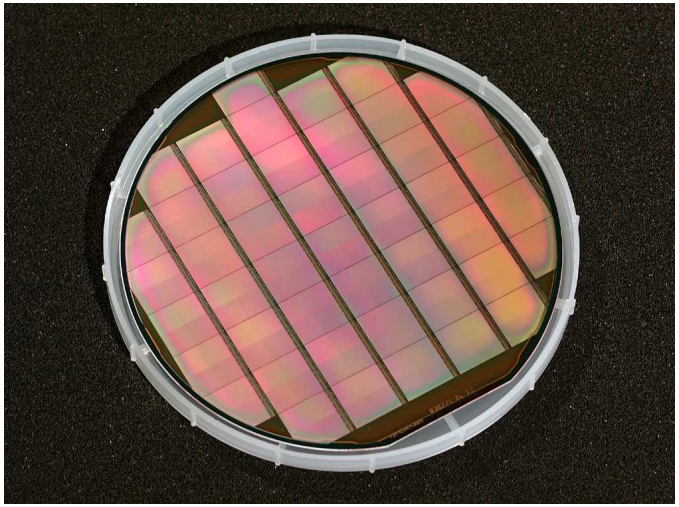


▷▷ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\longmapsto$ 1.7–1.6 μm (5 bits)
(MIMOSA-9 : 20 μm pitch; T= + 20 °C)

- Warning : foresee safety margin w.r.t. epitaxy thickness
  $\longmapsto$ ability to adapt to future fabrication processes

Thinning & Ladder Design

- **Thinning of MIMOSA-5 sensors (3.5 cm^2) for STAR detector upgrade:**
  - **3 wafers thinned via LBNL to 50 $\pm$ 5 μm**
  - **result satisfactory (after pre-dicing):**
    sensors can be manipulated and mounted on support
  - **3 ladder prototypes fabricated at LBL ($\gtrsim$ 0.25 % X_0)**
    $\longrightarrow$ up to 9 sensors mounted on ladder and tested
  - **Next: MIMOSTAR-3 prototypes will be thinned to 50 μm**
    in Autumn and mounted on ladders inside STAR

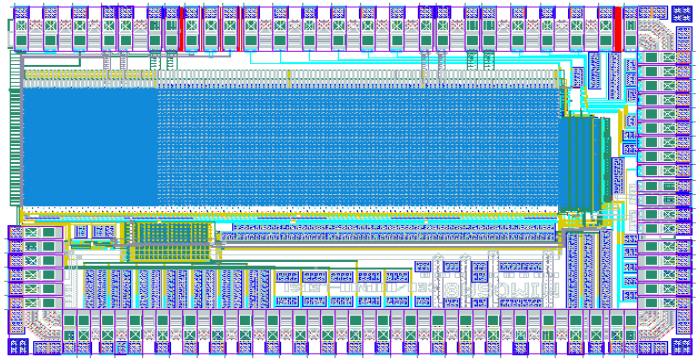


  - **studies will presumably be extended to ILC vertex detector (including cooling) via LBNL-ILC team**

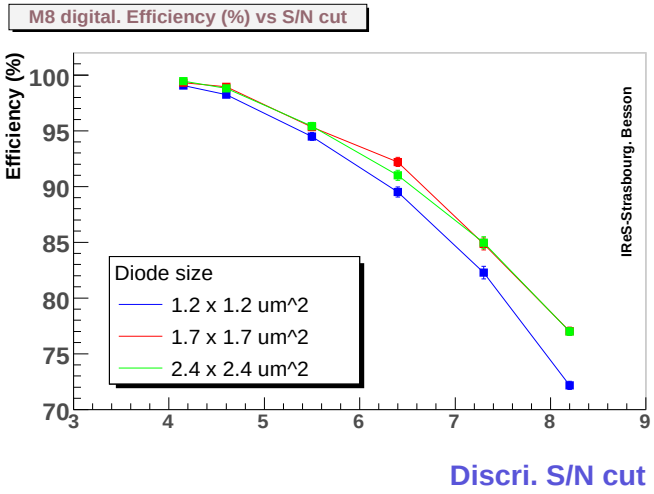
- **Thinning trials in Europe and Asia :**
  - **MIMOSA-5 chips thinned by TRACIT (near Grenoble) to 70 and 50 $\pm$ 5 μm (full wafers needed)**
    $\Rightarrow$ thinned chips are waiting for characterisation
  - **Thinning trials are also under way at ESIEE (Paris) and Dalian (China)**

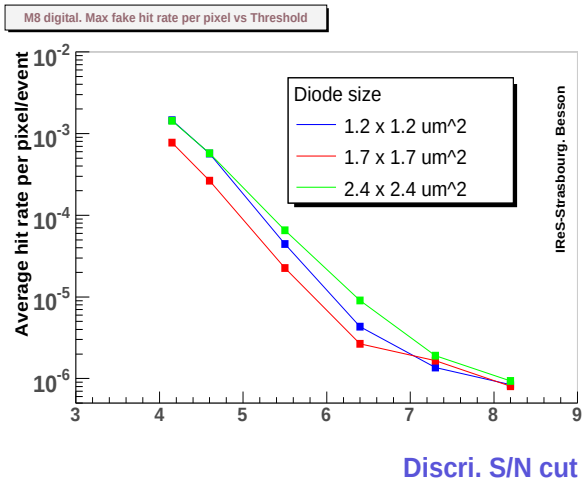
High Read-Out Speed Architecture

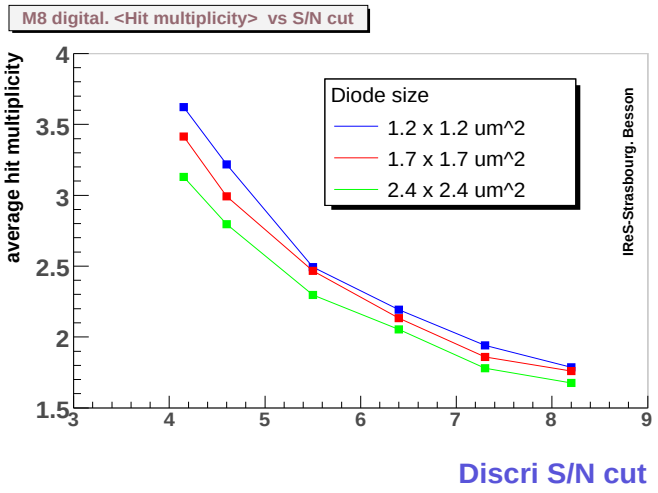
- **MIMOSA-8: TSMC 0.25 μm digital fab. process ($\lesssim$ 7 μm epitaxy)**
  - **32 // columns of 128 pixels (pitch: 25 μm)**
  - **read-out time $\sim$ 50 μs (resp. 20 μs) with (resp. without) DAQ**
  - **on-pixel CDS**
  - **discriminator (and CDS) integrated at end of each of 24 columns**



- **Detection performance with 5 GeV/c e^- beam (DESY):**







▷▷ **Excellent m.i.p. detection performances despite modest thickness of epitaxial layer**

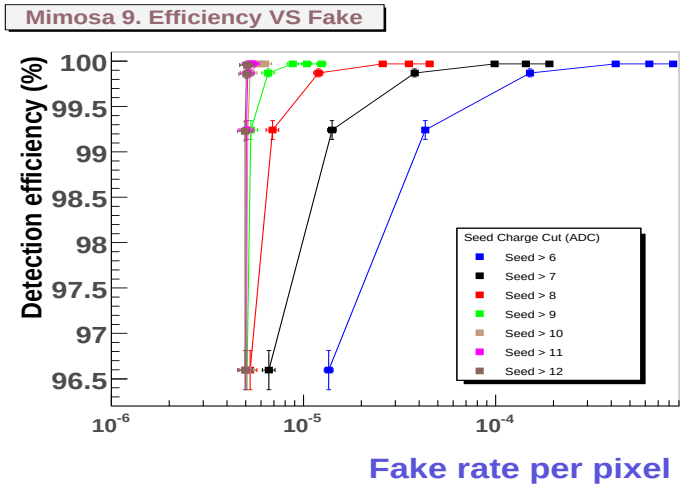
⁂ **det. eff. $\sim$ 99.3 % for fake rate of $\sim$ 0.1 %** ⁂ **discri. cluster mult. $\sim$ 3–4** ⁂ **$P_{diss} \lesssim$ 500 μW / col.**

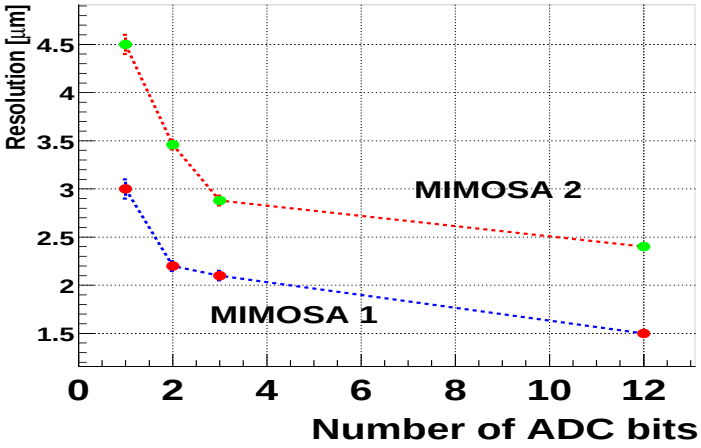
▷▷ **Architecture validated for next steps: techno. with thick epitaxy, rad. tol. pixel at T_{room}, ADC, $\emptyset$, etc.**

Constraints on Integrated ADC

- Ensure $\epsilon_{\mathbf{det}} > 99$ % with very few fake hits, $\sigma_{\mathbf{IP}} \sim$ few μm & efficient double hit separation

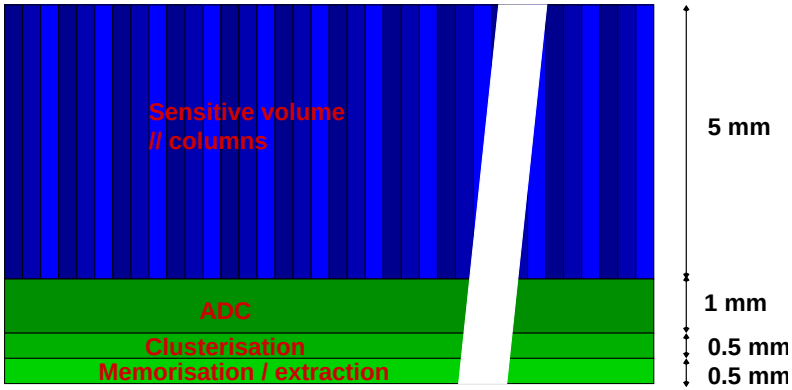
  $\Rightarrow$ distinguish small Q deposits due to: ✳ negative Landau fluctuations (seed) ✳ pixels in cluster crown





$\triangleright\triangleright\triangleright$ $\geq$ 3 effective bits OK $\mapsto$ base line: 4 – 5 bits $\rightarrowtail$ safety margin w.r.t. epitaxy thickness of final prod. techno.

- Read-out frequency : $\geq$ 10 MHz / column or $\geq$ 20 MHz / pair of columns
- Dimensions : 20–30 x 1000 μm^2 / column
  or 40–60 x 1000 μm^2 / pair of columns
- Power consumption : $\lesssim$ 0.5 mW / column or 1 mW / pair of columns



$\hookrightarrow$ several alternative ADC architectures studied in // by 5 teams :

Clermont (flash), Grenoble (semi-flash), Saclay (succ. approx.), Strasbourg (Wilkinson, succ. approx.), LBL

Application to ILC: Various FE Architectures

▷ **Fast col. // architecture (like MIMOSA-8), allowing to process signal (CDS, ADC, sparsification) during BX:**

↪ **complex, close to technology limits ↦ much design & test effort needed (but quite universal output)**

Alternative ↦ 2 phase μcircuit architecture exploiting beam time structure, reducing data flux (& EMI sensitivity ?):

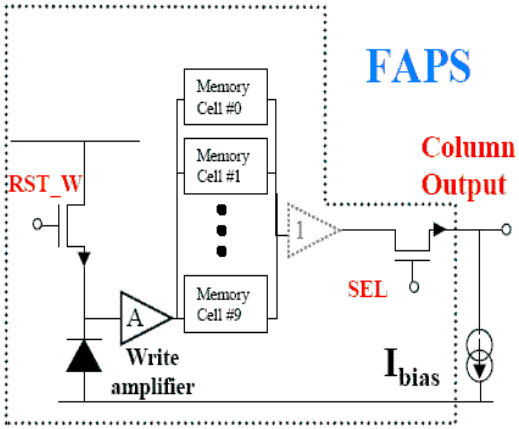
1) charge stored (eventually sampled) inside pixel during train crossing: O(1) ms

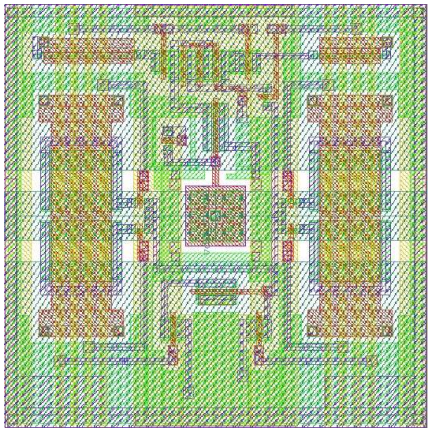
2) signal transfered and processed inbetween trains: O(100) ms

Different strategies of storage during train crossings (RAL, Hawaï, IPHC, Yale-Oregon):

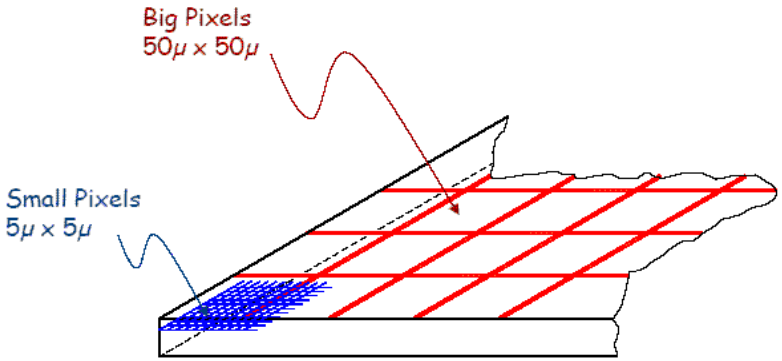
$\therefore$ 20 – 25 μm large pixels with $\gtrsim$ 20 capacitors

↪ **$\lesssim$ 50 μs long snapshots/capacitor**





$\therefore \lesssim$ 5 μm large pixels with 1 capa.(hit position) and 50 μm large pixels for hit zone selection + time stamp



▷ **Difficulty: are small capacitors precise enough ?**

▷ **Difficulty: can cluster size be $\lesssim$ 3 pixels ?**

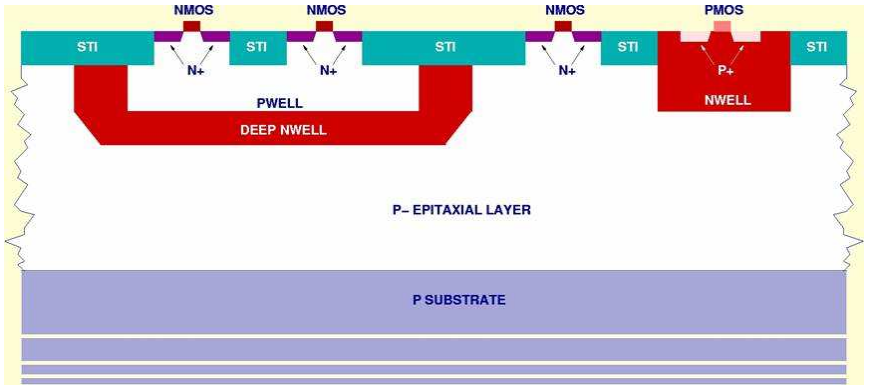
- Improving Charge Collection & Signal Proc. Capabilities

▶ **Increase collected charge by enlarging depleted volume:**

- **increasing N-well potential (very limited possibilities)**
- **enlarging surface of N-wells inside pixels ($\mapsto$ increases capacitance noise)**

  $\hookrightarrow$ **use standard N-well to integrate P-MOS T for signal processing**

▶ **Ex: triple-well technology (STM 0.13 $\mu m \rightarrowtail$ 0.09 μm)**
(Univ. Bergamo, Pavia, Pisa) :



▷ **Buried n-channel electrode:**

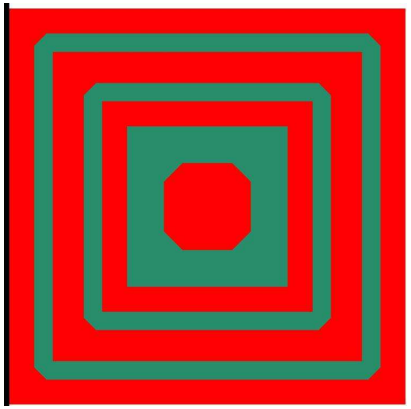
◇ **Try integrating signal processing μcircuits**

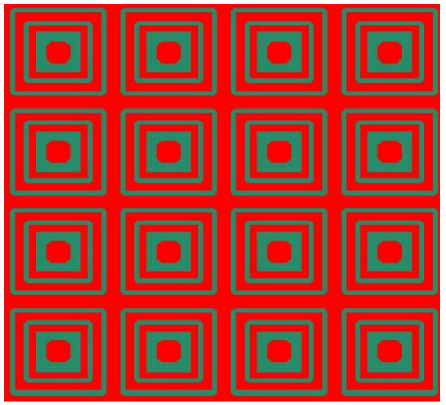
$\hookrightarrow$ **self triggered pixels (?)**

◇ **Test structures (43 μm pitch) fab. & tested**

$\hookrightarrow$ **next step: $\sim$ twice smaller pitch**

▶ **Ex: unidepleted active pixel sensors**
(P.Rehak et al.) :





▷ **Pixels composed of concentric rings of n-wells:**

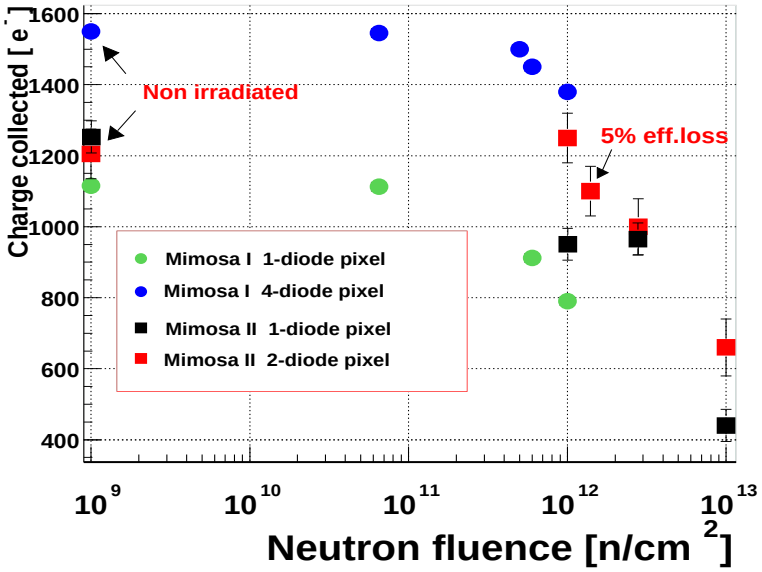
◇ **Can they host P-MOS T for signal processing ?**

◇ **Can they provide time stamping ?**

Radiation Tolerance: Non-Ionising Radiation

- **Neutrons of O(1 MeV) at JINR (Dubna):**
  irradiation with up to 10^{13} n_{eq}/cm^2

- **Tests with 2 sensors (T = + 10°C)**
  from different fabrication processes:
  - ◇ **AMS-0.6 ($\lesssim$ 14 μm epitaxy)**
  - ◇ **AMI-0.35 ($\sim$ 4 μm epitaxy)**
    - ↪ **charge loss for $\lesssim 10^{12}$ n_{eq}/cm^2**
      & modest increase of I_{leak} & noise ($\lesssim$ 10 %)



- **AMS-0.35 OPTO ($\sim$ 11 μm epitaxy) ▷ S/N (MPV) vs fluence and T (tests at CERN-SPS):**

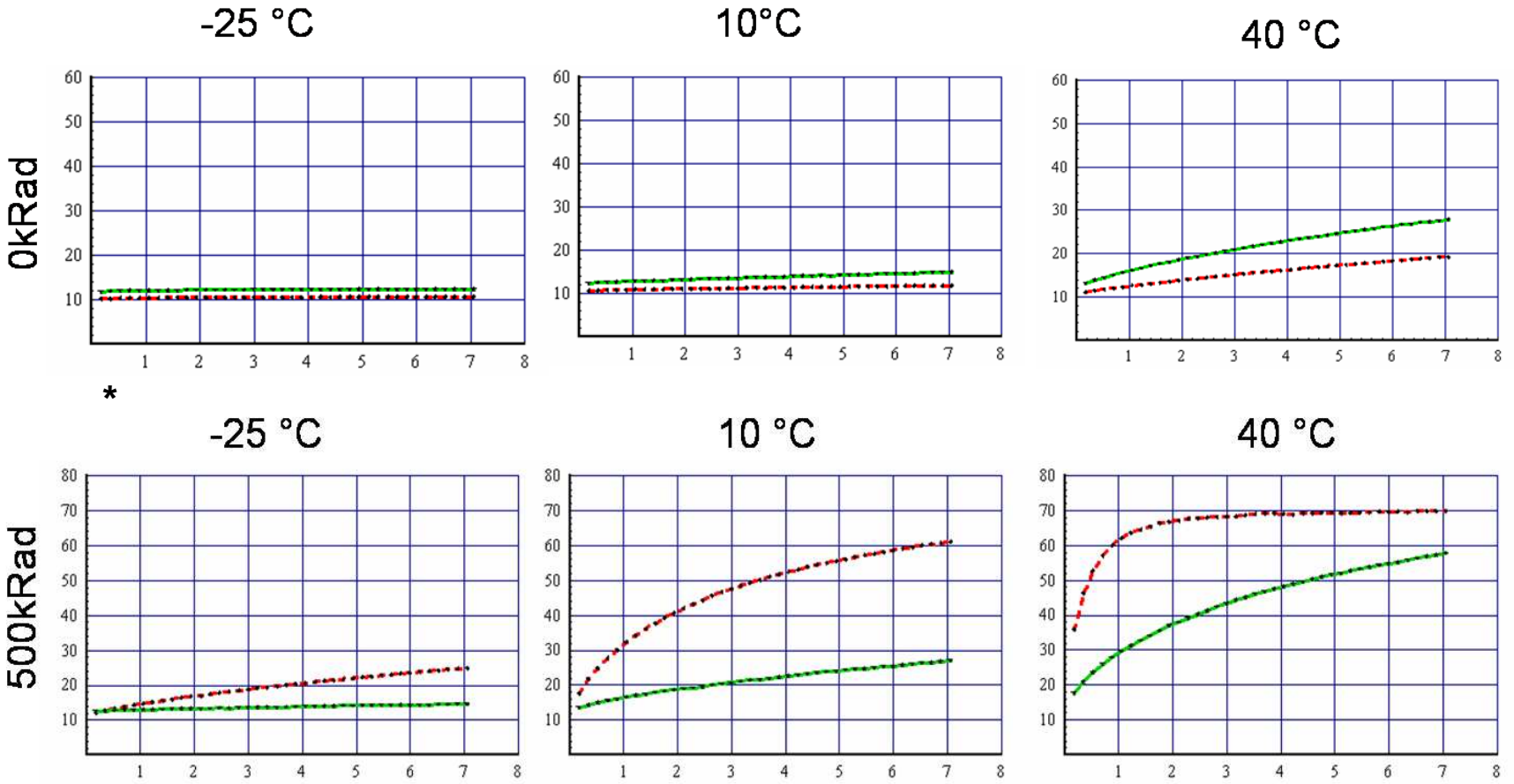
Fluence	T = -20°C	T = 0°C
0	28.4 ± 0.2	26.3 ± 0.2
10^{11} n_{eq}/cm^2	25.3 ± 0.2	24.5 ± 0.4
$3{\cdot}10^{11}$ n_{eq}/cm^2	—	23.0 ± 0.2
10^{12} n_{eq}/cm^2	**18.7 ± 0.2**	—

Conclusion: fluences of $\gtrsim 10^{12}$ n_{eq}/cm^2 affordable
(room temperature operation compatible with ILC neutron bg)
$\rightarrowtail \epsilon_{det} \sim 99.74 \pm 0.08$ % **(10^{12} n_{eq}/cm^2; T = -20°C)**

✳ **Fluences $\gtrsim 1{\cdot}10^{13}$ n_{eq}/cm^2 can presumably be accomodated**

Radiation Tolerance : Ionising Radiation

- **Modified pixel design to accomodate ionising radiation (e.g. 10 keV X-Rays):**
  - **removal of thick oxide nearby the N-well (against charge accumulation)**
  - **implantation of P+ guard-ring in polysilicon around N-well (against leakage current)**
- **Noise (e^- ENC) vs Integration time (ms) for Ordinary and Radiation Tolerant pixels (T = - 25°C, + 10 °C, + 40°C)**



▷▷▷ **500 kRad tolerance demonstrated at T_{room}**

Radiation Tolerance : Low Energy Electrons

- **Investigation of sensitivity to $\sim$ 10 MeV electrons (NIEL factor $\sim$ 1/30)**

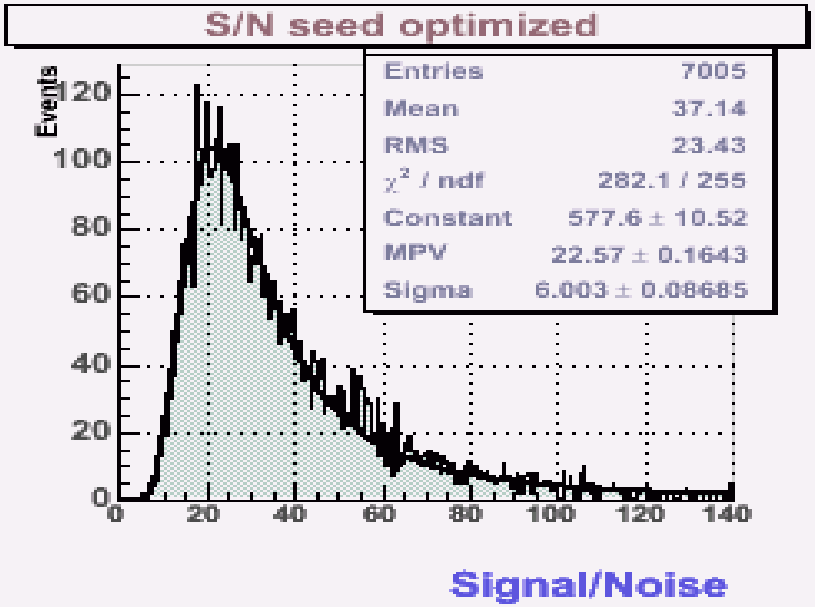
  $\hookrightarrow$ **similar to beamstrahlung $e^{\pm}$ in 4 T field at 15 mm radius**

1) MIMOSA-9 exposed to $10^{13} e^{-}_{9.4MeV}$/cm^2 in Darmstadt :
equivalent to $\lesssim$ 300 kRad/cm^2 and $\sim 3 \cdot 10^{11} n_{eq}$/cm^2

2) Irradiated chip tested with $\sim$ 6 GeV e^- at DESY

$\hookrightarrow$ **Test result at -20°C : S/N $\sim$ 23 $\rightarrowtail \epsilon_{det} > 99.3\%$**

(before irradiation: S/N $\sim$ 28 and ϵ_{det} = 99.93 $\pm$ 0.03 %)



▷ **Sensors still need to be tested at room temperature (compatible with very light cooling system)**

MAIN REQUIREMENTS OF THE ILC VERTEX DETECTOR

Constraints from Required $\sigma_{i.p.}$ (1/2)

- $\sigma_{\mathbf{IP}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \mathbf{sin}^{\mathbf{3/2}}\theta$ with $\mathbf{a} < 5\ \mu m$ and $\mathbf{b} < 10\ \mu m$

  ▷ limits on $\mathbf{a}$ and $\mathbf{b}$ are still "very educated guesses"

  ▷ SLD: $\mathbf{a}$ = 8 μm and $\mathbf{b}$ = 33 μm

- Upper bound on $\mathbf{a}$ drives the pixel pitch and the inner and outer layer radii

- Upper bound on $\mathbf{b}$ drives radius and material budget of inner layer (& beam pipe)

- Constraint on σ_{IP} satisfies simultaneoulsy requirement on double hit separation in inner most layer ($\sim$ 30 – 40 μm)

Constraints from Required $\sigma_{i.p.}$ (2/2)

- **Constraint on a :** $z_{IP} \approx \frac{z_0 \cdot R_4 - z_4 \cdot R_0}{R_4 - R_0} \rightarrowtail a = \sigma_{IP} \approx \frac{(R_4^2 \cdot \Delta z_0^2 + R_0^2 \cdot \Delta z_4^2)^{1/2}}{R_4 - R_0}$

  - Numerical examples based on $R_4 = 4 \cdot R_0$ (ex: R_4/R_0 = 60 / 15 mm or 64 / 16 mm)

    - $\Delta z_4 = \Delta z_0 = \sigma_{sp} = 3\,\mu m \Rightarrow a \approx 1.37 \cdot 3\,\mu m \approx 4.1\,\mu m$

    - $\Delta z_4 = 5\,\mu m$ and $\Delta z_0 = 2.5\,\mu m \Rightarrow a \approx 1.5 \cdot 2.5\,\mu m \approx 3.8\,\mu m$

  $\Rightarrow$ Twice larger pitch in outer layer than in inner most layer satisfies constraint $a < 5\,\mu m$

- **Constraint on b :** $b \approx 0.0136 \cdot (1 + 0.038 \cdot \ln t/\sin\theta) \cdot R_0 \cdot \sqrt{t}$ where $t = \frac{e_{pipe}}{X_0^{Be}} + t_{L0}$

  - $b < 10\,\mu m \Rightarrow t \lesssim 0.4\,\%$

  - $e_{pipe} \approx 400 - 500\,\mu m \rightarrowtail \frac{e_{pipe}}{X_0^{Be}} \sim 0.11 - 0.14\,\% \rightarrowtail t_{L0} \lesssim 0.25\,\%$

  - Ladders equipped with CMOS sensors & developed for STAR HFT reach already $\sim$ 0.3 % X_0

Constraints from Beamstrahlung

- **1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor**
  $\rightarrowtail \lesssim$ 1.8·10^{12} e$^{\pm}$/cm^2/yr (safety factor of 3)
  - **2nd layer: 8 times less**
  - **3rd layer: 25 times less**

- **Consequences on Occupancy in 1st layer (L0): $\lesssim$ 0.9 % hit occupancy in 50 μs (r.o. time of TESLA TDR)**
  $\hookrightarrow$ signal spread on $\lesssim$ 4.5–9 % pixels (cluster multiplicity $\sim$ 5-10)

  $\Rrightarrow$ 1) aim for shorter read-out time in L0 than in TDR $\rightarrowtail$ typically $\lesssim$ 25 μs
  (compromise with power dissipation, multiple scattering, ...)

  2) aim for shorter read-out time in L1 than in TDR $\rightarrowtail$ typically $\sim$ 50 μs (vs 250 μs)
  and presumably smaller radius (e.g. $\sim$ 20 – 22 mm)
  (use tracks extrapolated from L1-4 down to L0)

  3) aim for relaxed read-out time in L2, L3, L4: $\sim$ 100 – 200 μs (vs 250 μs)
  $\hookrightarrow$ depends on backscattered e$^{\pm}$ rate

- **Consequences on Radiation Tolerance in L0 :**
  - ✳ **dose integrated over 3 years: $\lesssim$ 5.4·10^{12} e/cm^2 $\longrightarrow$ $\lesssim$ 2·10^{11} n$_{eq}$/cm^2 (NIEL $\sim$ 1/30)**
  - ◇ **neutron dose integrated over 3 years much smaller : $\lesssim$ 3·10^{10} n$_{eq}$/cm^2 (safety factor of 10)**

Consequences on Inner Layer Design

- $\lesssim$ 25 μs in L0:

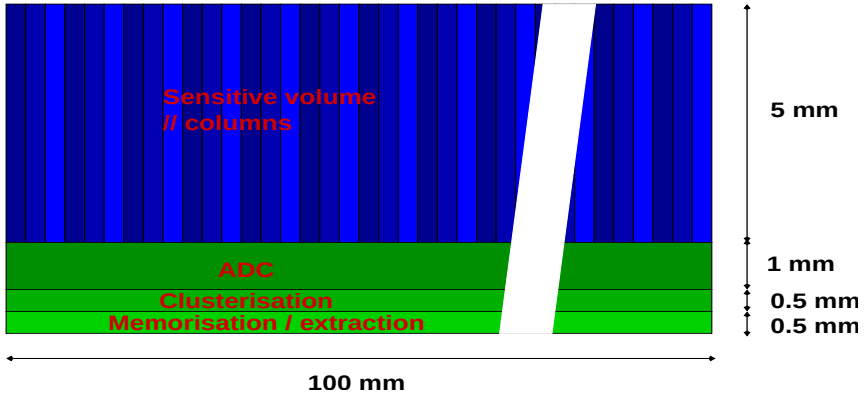
  columns of 256 pixels (20 μm pitch) $\perp$ beam axes

  read out in // at $\sim$ 10 MHz $\longrightarrow$ 5 mm depth

- $\sim$ 50 μs in L1:

  columns of 512 pixels (25 μm pitch) $\perp$ beam axes

  read out in // at $\sim$ 10 MHz $\longrightarrow$ 13 mm depth



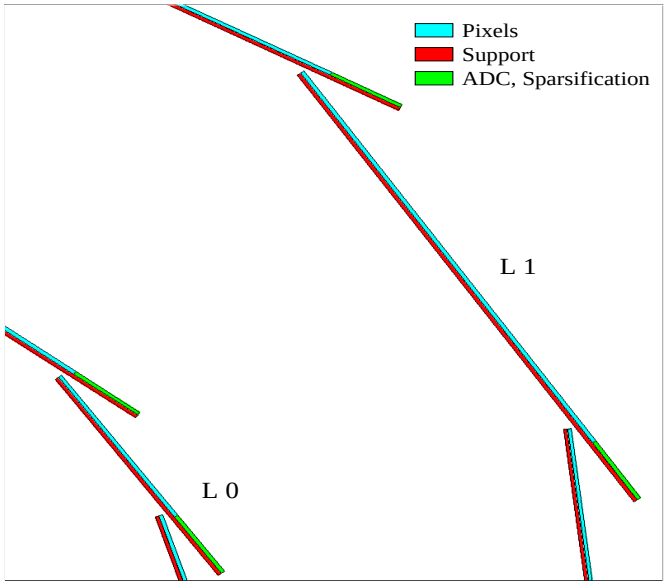
- $\lesssim$ 2 mm wide side band hosting ADC, sparsification, ...

  $\hookrightarrow$ effect on material budget SMALL :

  b increases by $\sim$ 5 – 10 %

- Option with discriminator instead of ADC :

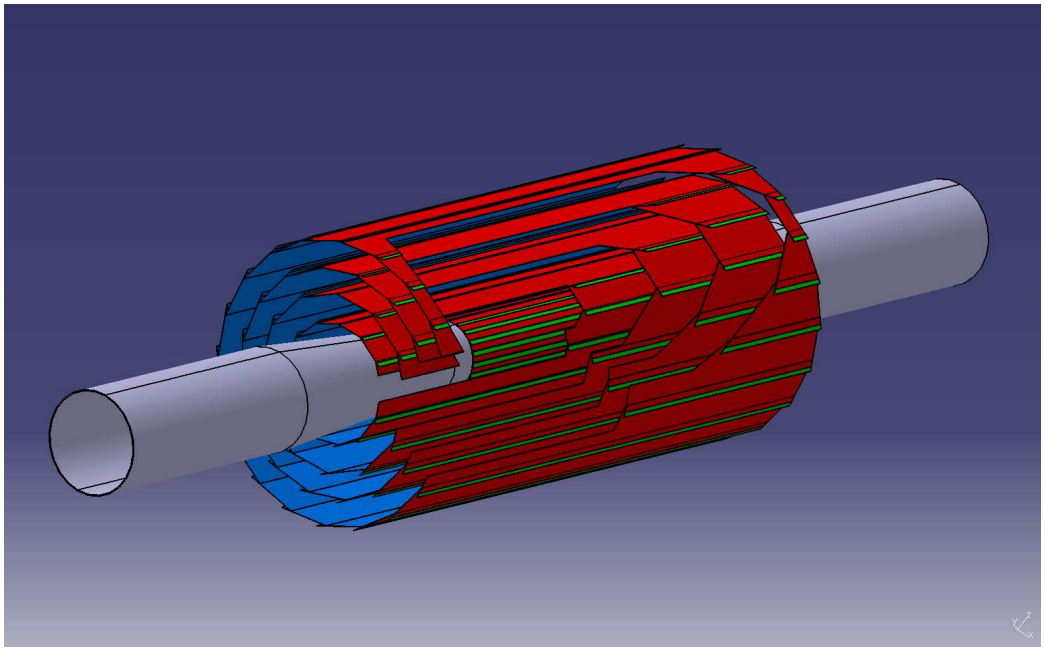
  $\sim$ 1 mm wide side band $\Rightarrow$ effect on $\mathrm{b} < 5$ %



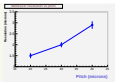
Basic Vertex Detector Design features

- Geometry : 5 cylindrical layers (R = 15 – 60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96
- L0 and L1 : fast col. // architecture
- L2, L3 and L4 : multi-memory pixel architecture (?)
- Pixel pitch varied from 20 μm (L0) to 40 μm (L4) by 5 μm steps $\rightarrowtail$ minimise P_{diss}

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	$<$100	$<$5
L1	$\leq$ 25	25	50	$\leq$26	$\leq$ 65	$<$130	$<$7
L2	37	30	$<$200	24	75	$<$100	$<$5
L3	48	35	$<$200	32	70	$<$110	$<$6
L4	60	40	$<$200	40	70	$<$125	$<$6
Total				142	**305**	$<$565	$<$3–30



- Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; 35 μm thick sensors)
- Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5} \rightarrowtail$ whole detector $\cong$ 100 MB/s (mainly from $e^{\pm}_{BS}$)

  -

Summary of Performances Obtained vs Requirements

- **Impact parameter resolution :**
  - $\mathbf{a} < 5\ \mu m$ ✓
  - $\mathbf{b} < 10\ \mu m$ ✓ ⟶ **thinning** ✓ **, ladder design** ✓ **(from STAR), stitching not yet investigated**

- **Radiation tolerance at room temperature :**
  - **neutrons** ✓
  - **X-Rays** ✓
  - **10 MeV electrons** ✓ ⟶ **only assessed at T** $\lesssim 0^\circ$**C**

- **Fast, low power, integrated signal processing :**
  - **read-out speed** ✓
  - **integrated ADC** ⟶ **under developement**
  - **integrated sparsification** ⟶ **studies starting**
  - **power dissipation** ✓ **(duty cycle** $<$ **1/20)** ⟶ **pulsed powering not fully assessed for this duty cycle**

What is already Achievable from Existing Devices ...

Minimal option $\Rightarrow$ // columns providing binary output after pixel discrimination at the column ends

⁂ Motivations :

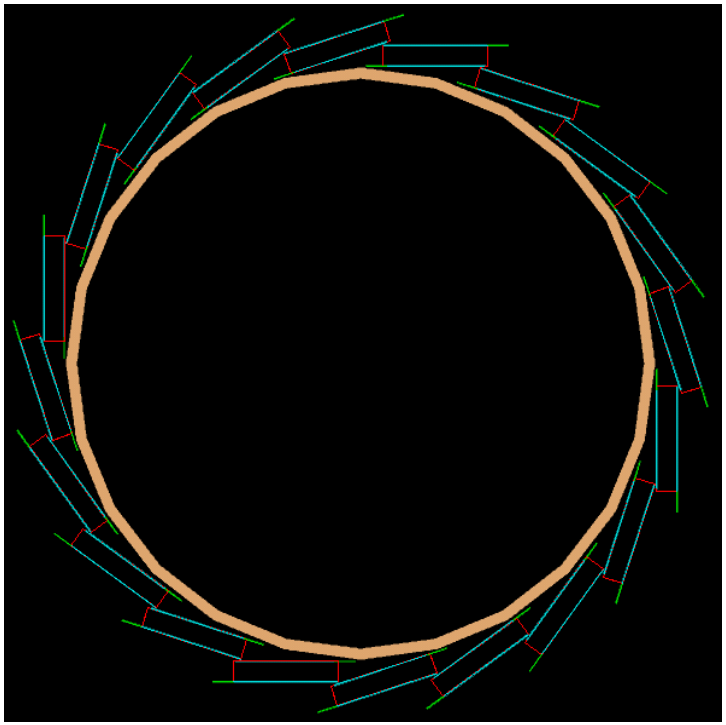
- existence of well working prototype $\Rrightarrow$ MIMOSA-8 : det.eff. $\sim$ 99.3 % , fakes $\sim 10^{-3}$, r.o. time $\sim$ 50–100 μs
  - $\Rrightarrow$ translation in AMS-0.35 OPTO (with rad. tol. pixel) under way $\Rrightarrow$ large proto. in '07 (256 x 256 pixels) ?
    - $\Rrightarrow \sim$ 1000 hits/BX in whole detector (mainly $e^{\pm}_{BS}$, $\sim$ no fake hits) $\Rrightarrow 14 \cdot 10^6$ hits/s
      - $\Rrightarrow \sim$ 100 MB/s for whole detector (2-3 Bytes / addressed hit ; $\leq$ 3 addressed hits / cluster)
- simplicity w.r.t. 4- or 5-bit ADC design
- almost twice less power dissipated per column
- CMOS band on chip periphery shrinks to $\sim$ half size ($\lesssim$ 1 mm) $\Rrightarrow$ mat. budget slightly reduced

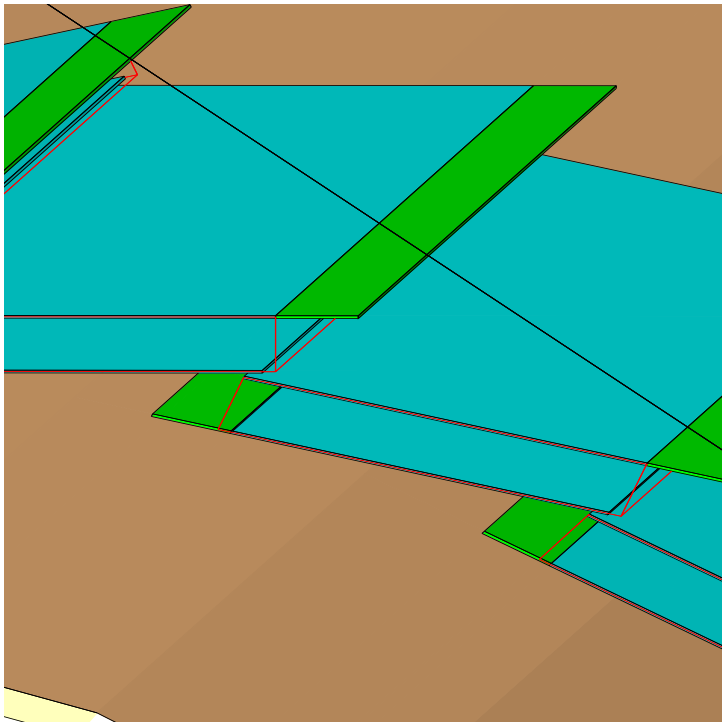
⁂ Drawbacks :

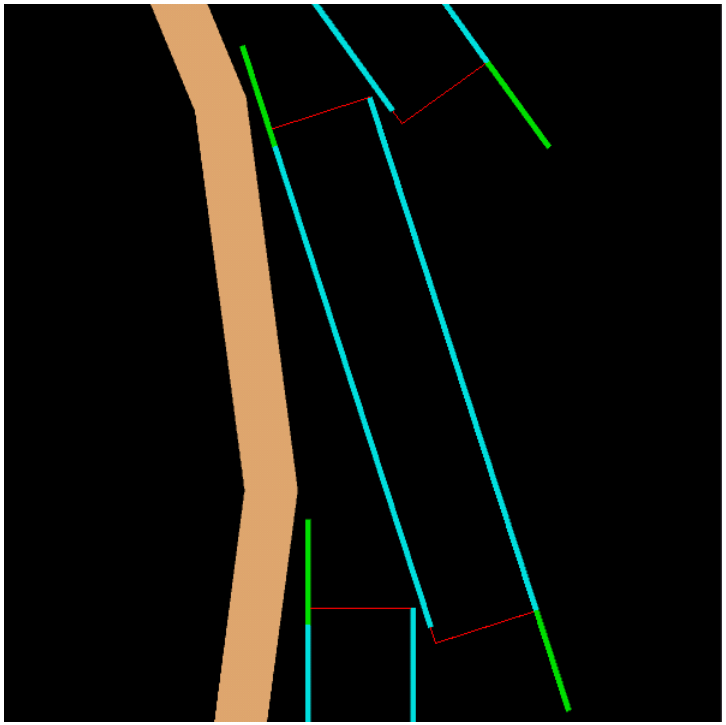
- need smaller pitch in order to keep high single point resolution
  - ▷ ex: 15 μm pitch $\longrightarrow$ 4.3 μm binary resolution $\longrightarrow$ resolution of clusters of 3 - 4 pixels ?
- smaller pitch $\longrightarrow$ more pixels per column $\longrightarrow$ slower frame r.o. (ex: 34 μs instead of 25 μs)
- slimmer columns $\longrightarrow$ sensor subdivided in more columns $\longrightarrow$ increased power dissipation
  (recovers what was won from avoiding ADCs)
- less beamstrahlung electron identification capabilities ?

Adapting the Inner Most Layer to High Background

- Design inner most layer (L0) to minimise its sensitivity to (unexpected) high occupancy ($\gtrsim$ 10 %)
- Double sided layer $\longrightarrow \sim$ 1 mm long mini-vectors connecting impacts on both sides of layer
  - ▷ Needs a detailed feasibility (engineering) study ....

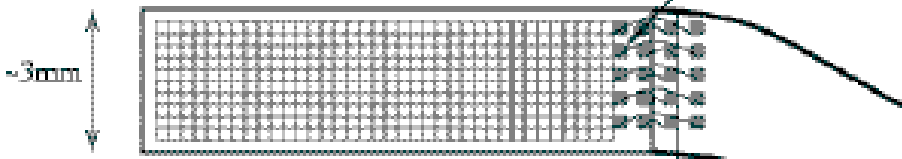






Integration of CAP in (Super)BELLE

CAP3

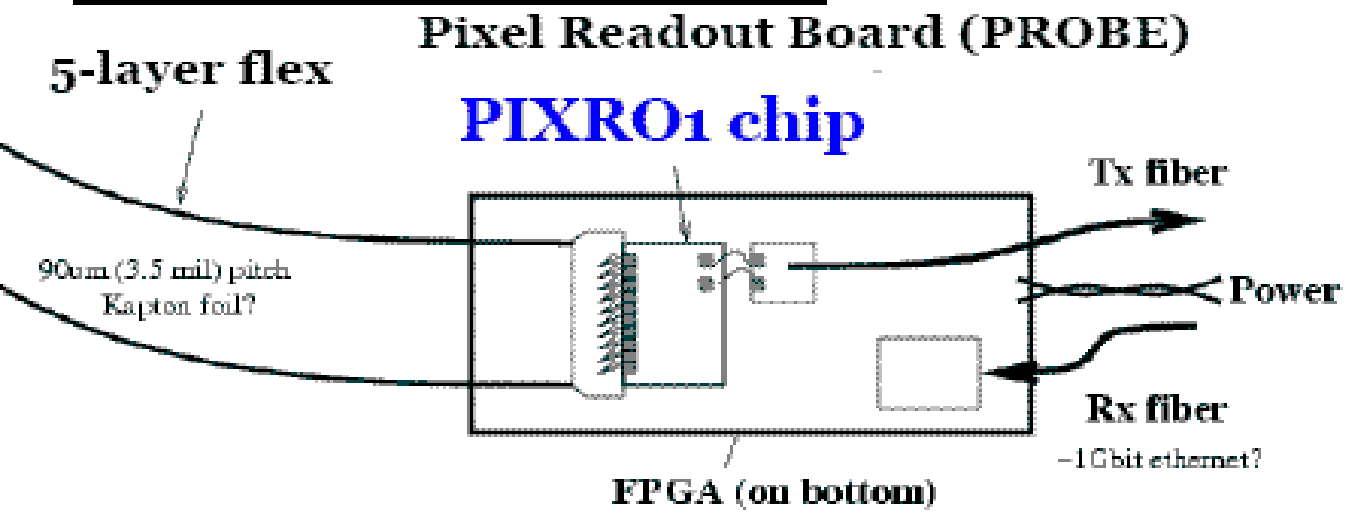


128 x 928 pixels, 22.5μm²

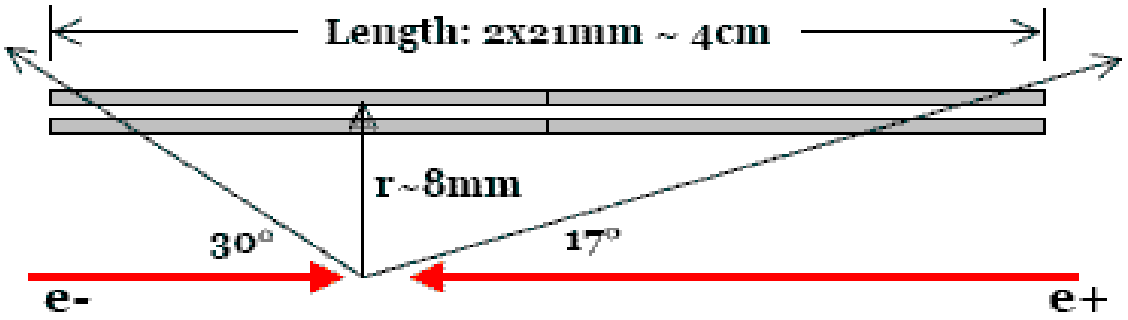
~120 Kpixels / CAP3

0.25 μm process

Half ladder scheme

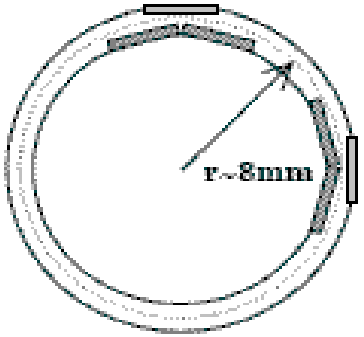


Side view



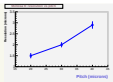
End view

Double layer, offset structure



# of Detector / layer ~ 32

PLANS FOR 2006 – 2009



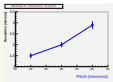
- Mid-Term Applications of CMOS Sensors

▷▷ **CMOS sensors will be operated in real (less demanding) experiments before end of decade**

⟶ **opportunity to assess their performances for the ILC running conditions**

- **MIMOSA sensors will equip STAR Heavy Flavour Tagger:**
  - ✳ **2008: analog output, 4 ms frame r.o. time**
  - ✳ **2011: digital output, $\lesssim$ 200 μs frame r.o. time**
    - ▷ **similar sensors will equip EUDET (FP-6) beam telescope:**
      - ✳ **2007: demonstrator with analog output**
      - ✳ **2008: final device with digital output**

- **CMOS sensors are also developed for BELLE Vertex Detector ⟼ R&D in Hawaï**

  -

Mid-Term Objectives of CMOS Sensor Development

2006 :

- ✳ **Production (engineering run) :** STAR demonstrator final proto., EUDET Beam Telescope demonstrator
  ↪ studies : yield, ”20 μm” option, thinning, perfo. with inclined tracks, ...
- ✳ **Prototyping :** various ADCs, col. // discri. archi., FAPS, high-resol. array, new fab. techno.

2007 :

- ✳ **Production (engineering run):** final chip for STAR demonstrator (analog output)
- ✳ **Prototyping :** small array with integ. ADC/col. , medium size fast array with integ. discri.,
  $\emptyset$ μcircuits, new fab. techno., stitching (?)

2008 :

- ✳ **Production (engineering run):** EUDET Beam Telescope final sensor (digital output)
- ✳ **Prototyping :** medium size pixel array with integ. ADC & $\emptyset$, new fab. techno.,
  1st ladder equipped with fast sensors (?), ...

2009 :

- ✳ **Production (engineering run):** final STAR-HFT sensors (digital output), etc.

SUMMARY

- **CMOS sensor technology R&D started in 1999 :**
  - ⇛ **now assessed quite extensively ⟼ attractive vertexing performances well established**
    - ⇛ **1st detector made of CMOS sensors should be commissioned in a few years :**
      - **STAR-HFT : 1) 2008, 2) 2011**
      - **BELLE-VD ($\lesssim$ 2010 ?)**
      - **EUDET beam telescope : 1) 2007, 2) 2008**
        - ⟼ **baseline architecture quite close to ILC requirements**

- **Wide spectrum of CMOS sensor potential still poorly explored/exploited (even if not crucial for ILC) :**
  - ▷ **Growing R&D community undertaking the challenge (e.g. integrated signal processing) :**
    - **$\sim$ 10 groups involved in chip design**
    - **$\gtrsim$ 10 groups concentrating on tests and integration issues (still poorly covered).**

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⇛ **Main R&D efforts in the coming years:**

- **Fast col. // architecture with integ. ADC & sparsification**
- **Fab. proc. with feature size $<$ 0.25 μm**
- **More in-pixel functionnalities : FAPS, self-triggered, time stamping , ...**
- ◇ **Complete radiation tolerance studies (T $\gg 0^{\circ}$C)**
- ◇ **Complete thinning $\sim$ 50 μm & try $\lesssim$ 35 μm**
- **Develop ladder concept equiped with CMOS sensors**
- ◇ **Investigate stitching**

▷▷ **Full L0 prototype ladder satisfying $\sim$ all requirements should be ready $\lesssim$ 2010**

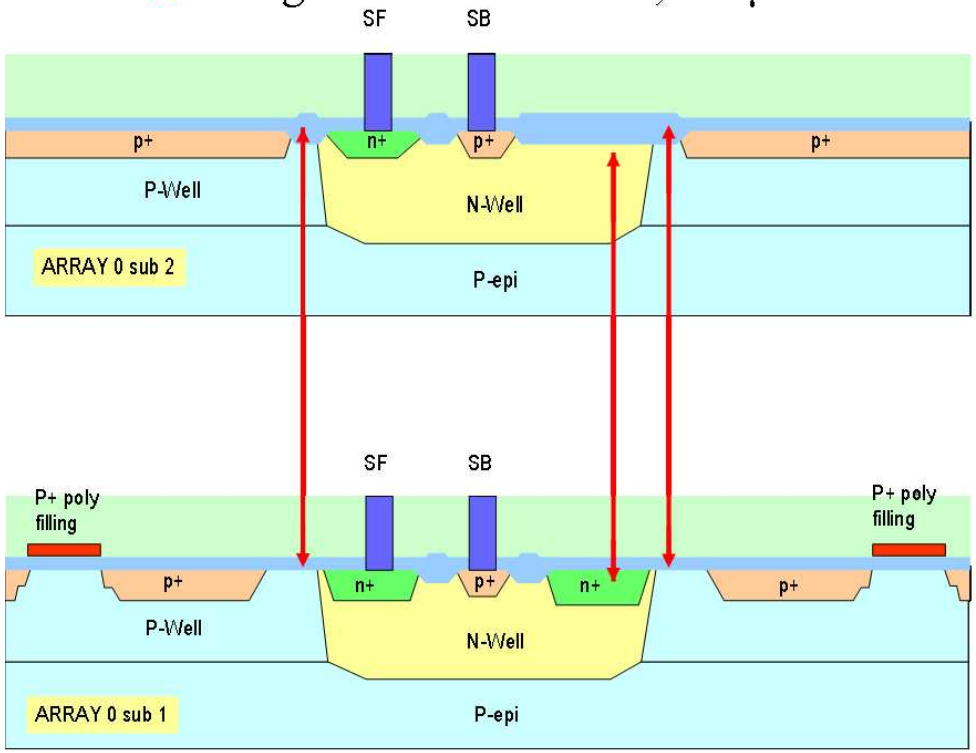
Improving Tolerance to Ionising Radiation

Modified pixel design:

- removal of thick oxide nearby the N-well (against charge accumulation)
- implantation of P+ guard-ring in polysilicon around N-well (against leakage current)

Beamtest on MIMOSA11

Running conditions: +40°C, 700µs readout time



	New	After 20kRad
Standard pixel (A0 Sub 2)		
S/N (MPV):	23.9	10.3
Det Eff [%]:	99.9	97.7
Noise [e⁻]:	10.7	23.5
Hardened pixel (A0 Sub 1)		
S/N (MPV):	14.9	15.1
Det Eff [%]:	99.5	99.6
Noise [e⁻]:	16.1	16.1