CMOS Monolithic Pixels R&D at LBNL

A Vertex Detector for the ILC

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Outline

- Introduction
- Summary of results from 1st prototype
  - Beam-test with 1.5 GeV electrons
  - Laser scan for position resolution studies
  - Irradiation with 30 MeV protons
- Design of 2nd prototype
- Outlook: future plans

Introduction: Silicon Pixel R&D at LBNL

- ILC Silicon Pixel R&D supported by 3-year Laboratory Directed R&D funding started in October 2004

- R&D directions:
  - sensor design and characterization
  - readout development
  - back-thinning tests
  - pixel module engineering

  } → **see talk in Session on Integration**

- Synergy with other on-going LBNL activities on CMOS pixels: STAR VXD upgrade, electron microscopy, existing infrastructure from ATLAS pixels

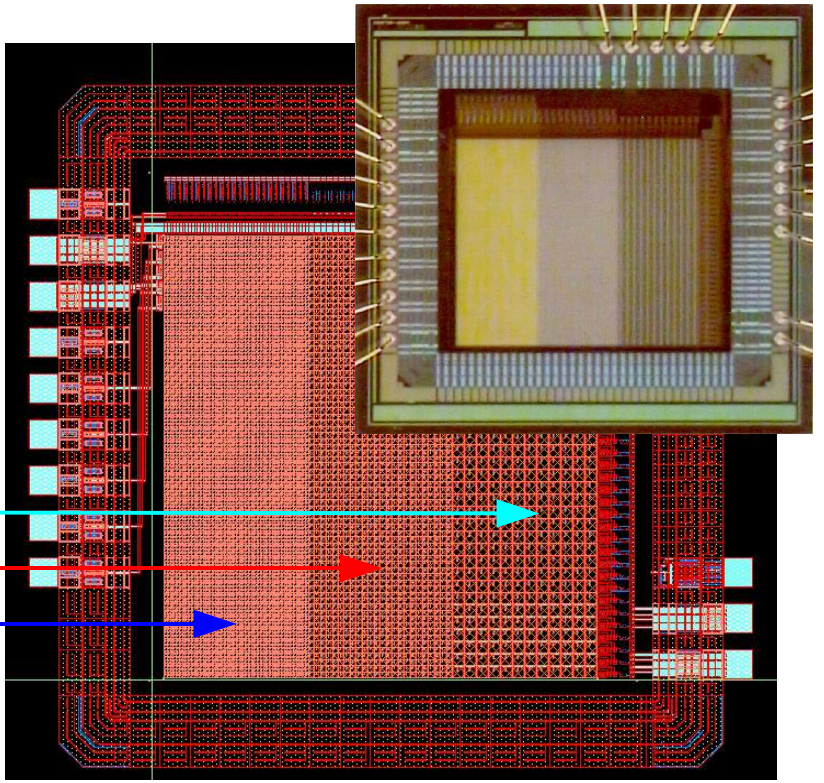
- Availability of test facilities on site:
  - Advanced Light Source: beam-tests with 1.5 GeV e^-
  - 88-inch Cyclotron: irradiations with 30-50 MeV p, neutrons
  - National Center for Electron Microscopy (NCEM)

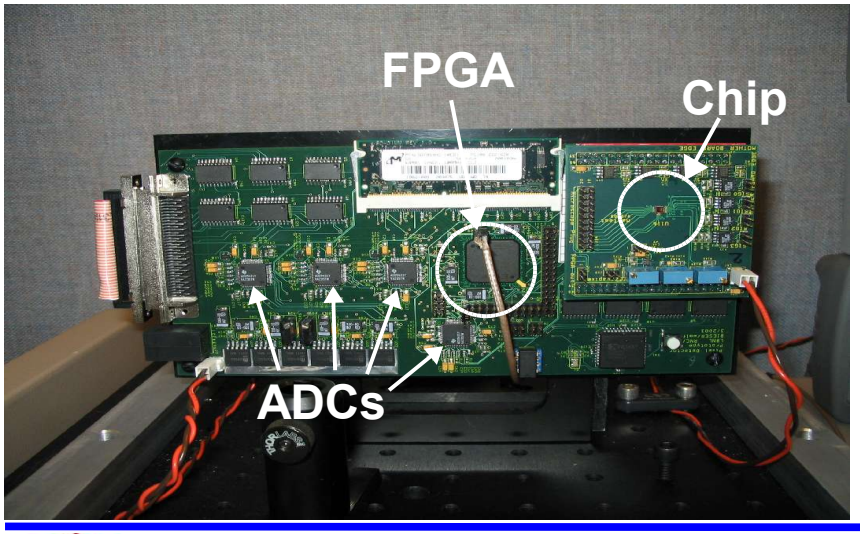
The first CMOS pixel test structure @ LBNL

- LDRD-1: first CMOS pixel test structure developed and fabricated (through MOSIS) in 2005 in collaboration with LBNL Engineering Division

- 0.35 μm OPTO AMS prototype, 3-T pixels, serial analog readout

- Three pixel geometries
  - 12 x 36 40 μm pixels
  - 24 x 72 20 μm pixels
  - 48 x144 10 μm pixels





- Xilinx FPGA based readout board (LBNL development)

- 14 bit digitization, interface with PC with LabView program for data acquisition and on-line event display

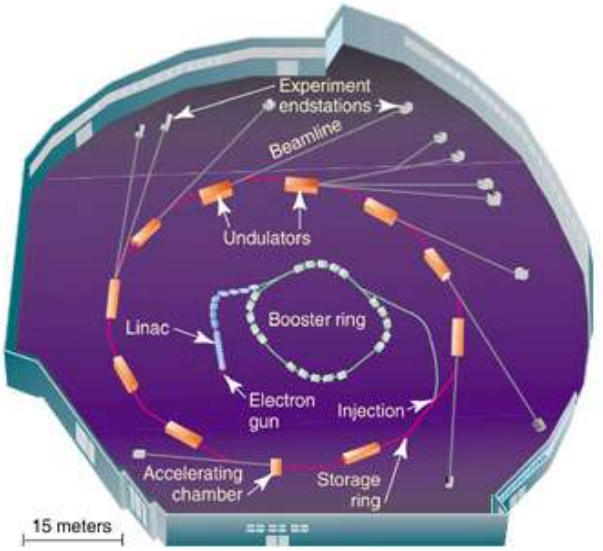
- C++/ROOT based off-line data analysis

Beam-test at the Advanced Light Source

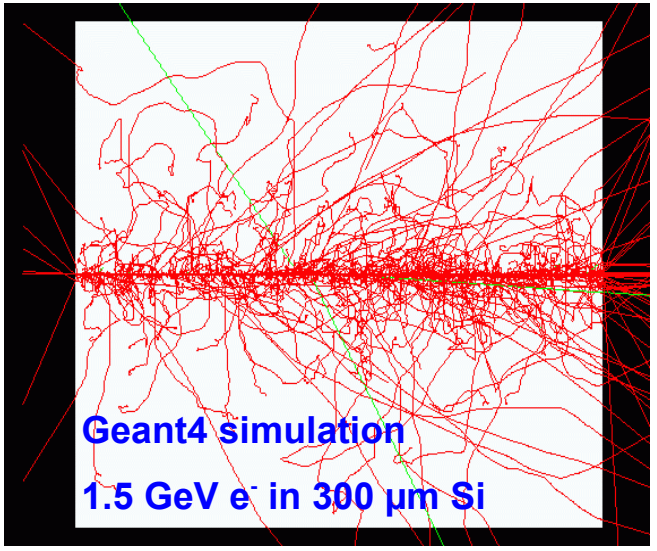
- Test performed at the BTS beam line of the Advanced Light Source (ALS)

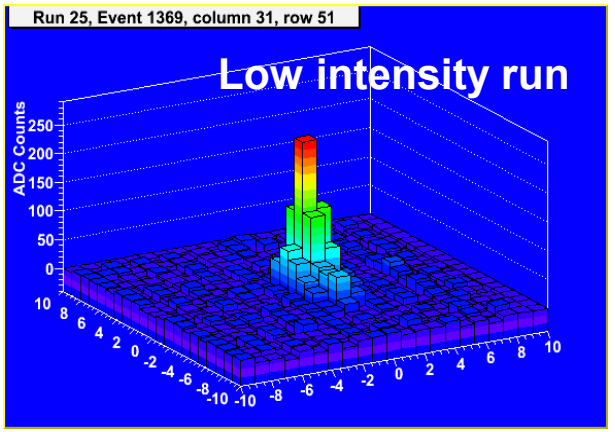
- Single bunch of primary 1.5 GeV e^- @ 1 Hz, tunable particle flux

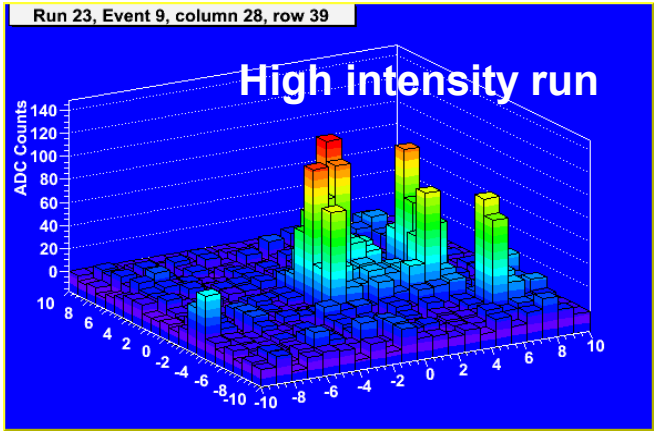
- Readout sequence:
  - detector kept in reset between 2 bunches
  - trigger on beam pick-up signal, read 4 frames, timing tuned to record signal on 3rd frame
  - readout with 1 ms integration time



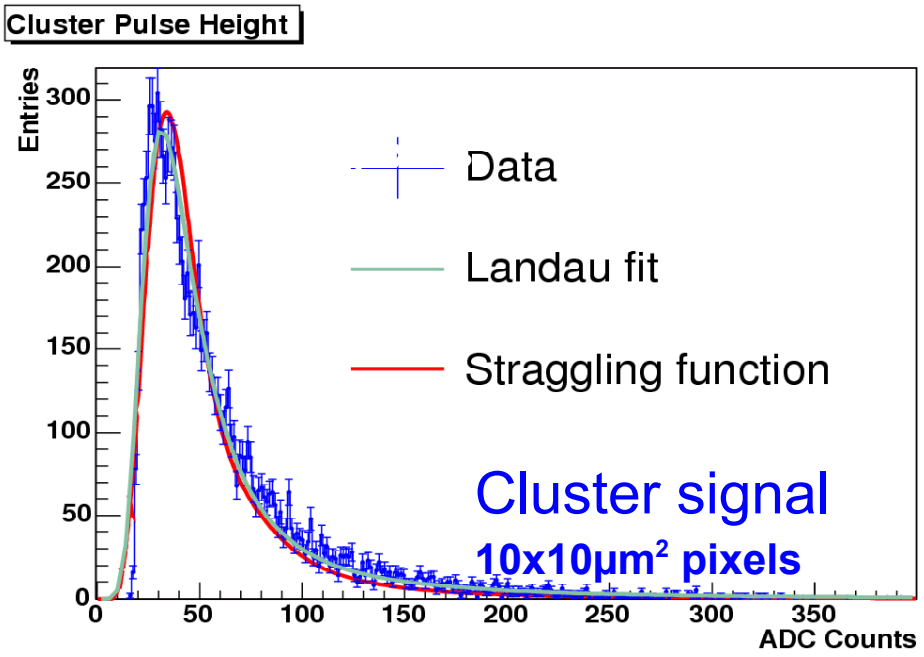
- Pixel noise and pedestals initialized with beam off, update during run on empty frames

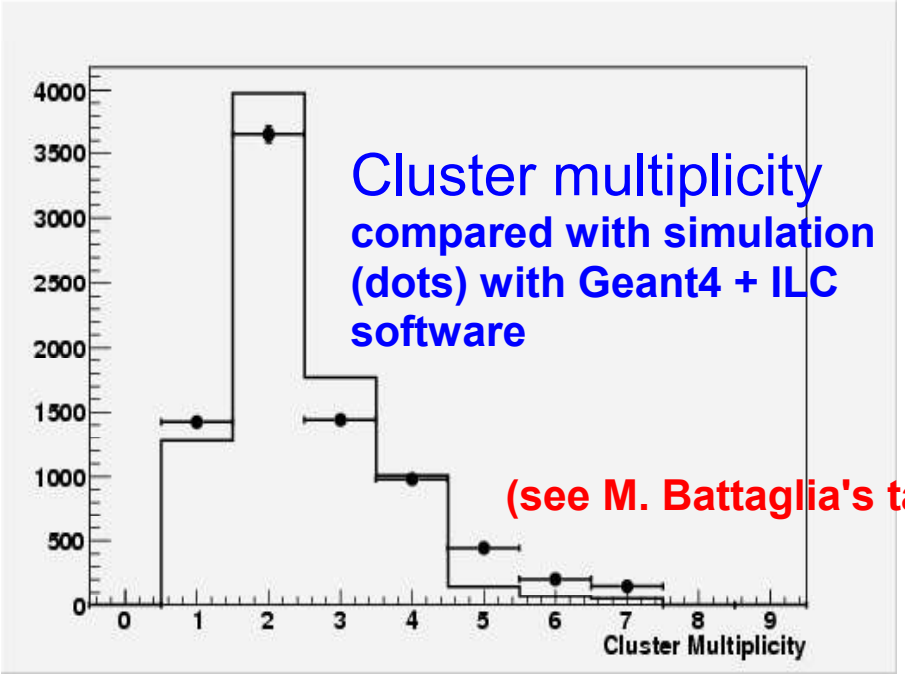






Beam-test results

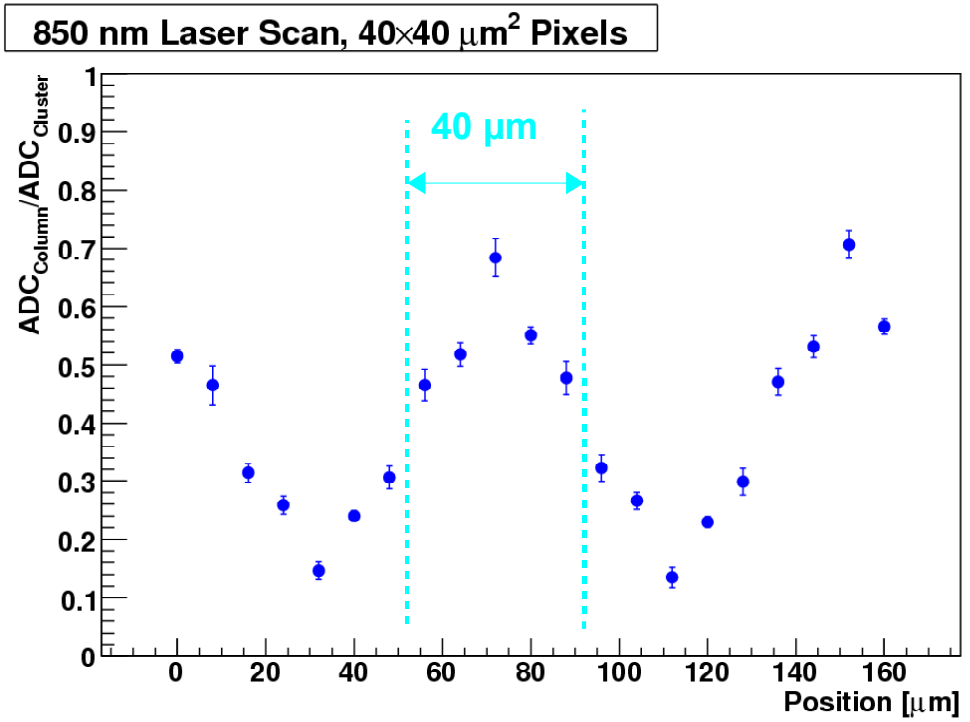




- Measurements performed at room T (24ºC)
- Compare width of Landau fit to e^- data to thin straggling function prediction for different active volume thicknesses
- Best agreement for 10 μm of Si, corresponding to MPV energy loss of 1.86 keV → 505 e^-

Pixel pitch	10 μm	20 μm	40 μm
<Nb Pixels>	2.71	2.67	2.37
<S/N>	14.1	14.5	15.4

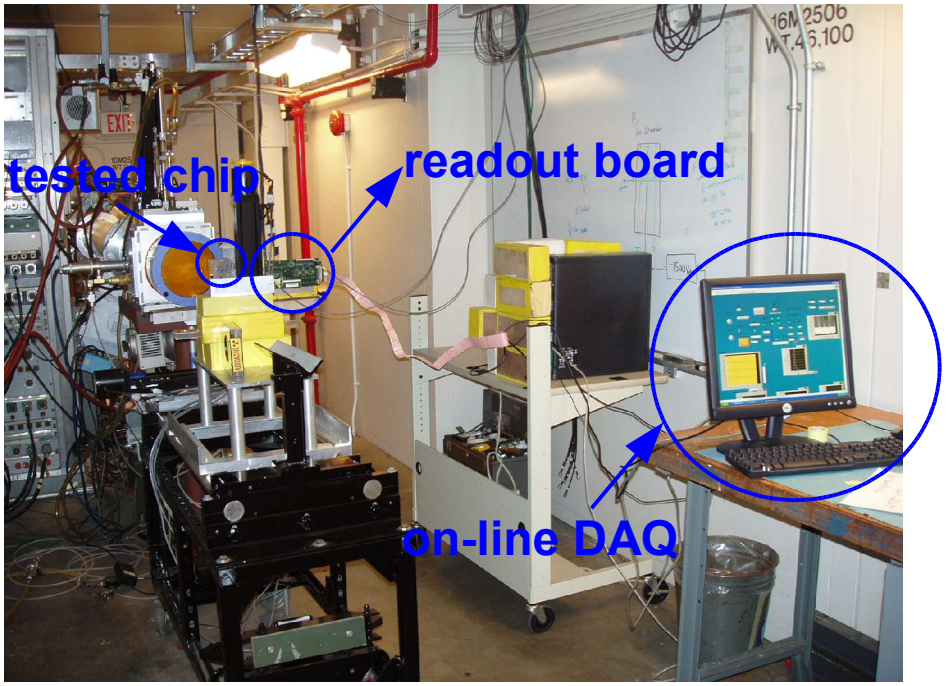
Position resolution studies

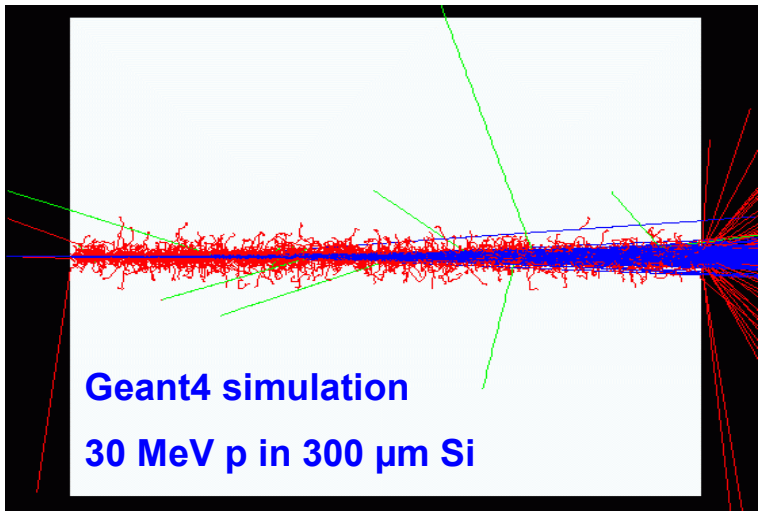


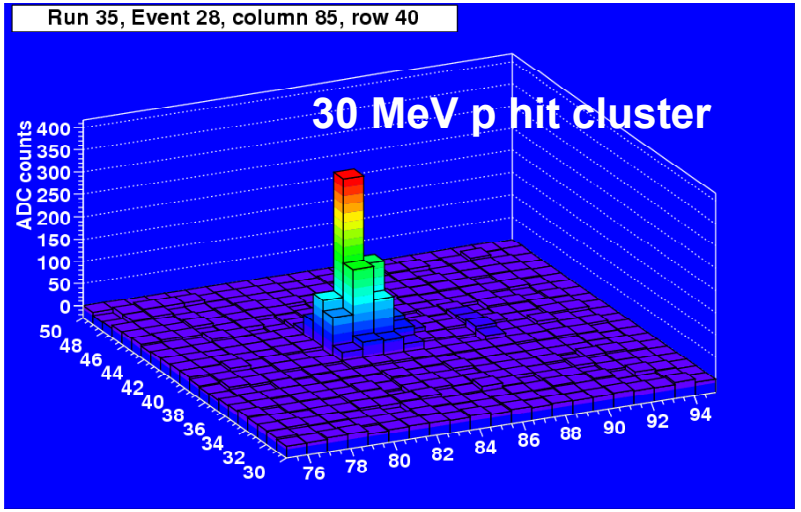
- Pixel scan with focused (~10 μm) 850 nm laser spot
- Plot $\eta = PH^{i}_{column}/PH_{cluster}$ versus laser spot position
- From variation of signal fraction vs position along the pixels and S/N estimation of spatial resolution: ~2.0, 3.3, 5.1 μm for 10, 20, 40 μm pitch pixels
- Uncertainty on measurement on 10 μm pitch pixels due to size of laser spot comparable with pixel size

Irradiations at the 88” Cyclotron

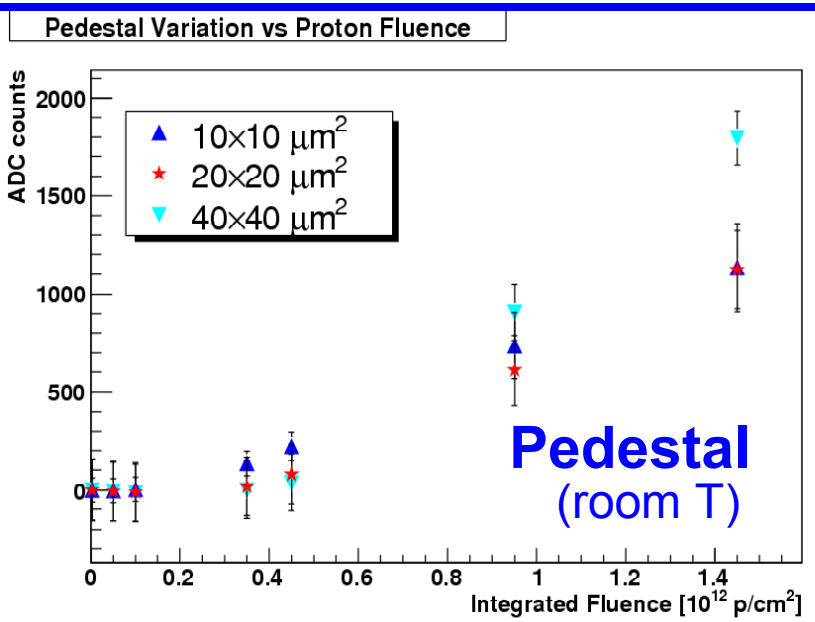
- Irradiation with 30 MeV protons up to 1.4×10^{12} p/cm^2 at the BASEF facility
- Facility available to users, irradiation of DEPFET single pixel prototype in Summer
- Proton flux ~7×10^{7} p/cm^2/s
- Irradiation in steps: pedestal noise recorded after each step
- Detector powered on and kept in readout mode during irradiations

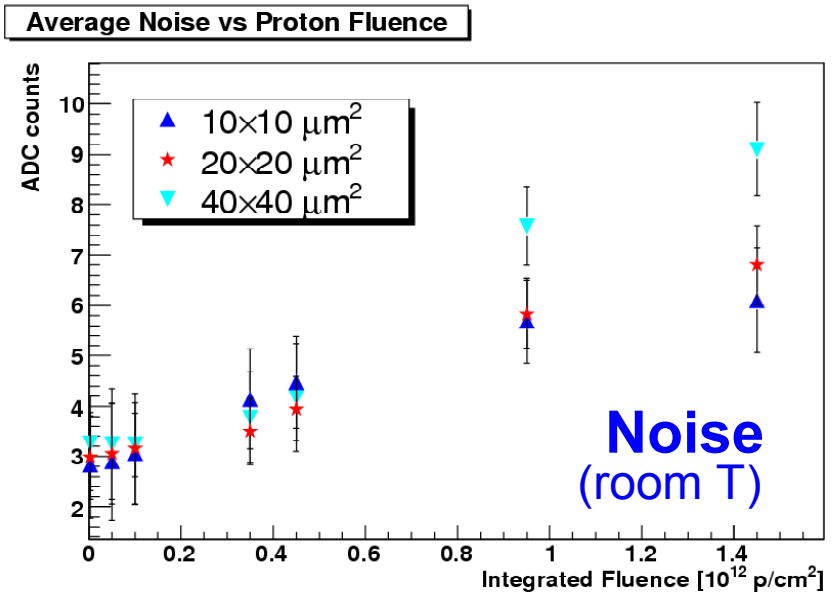




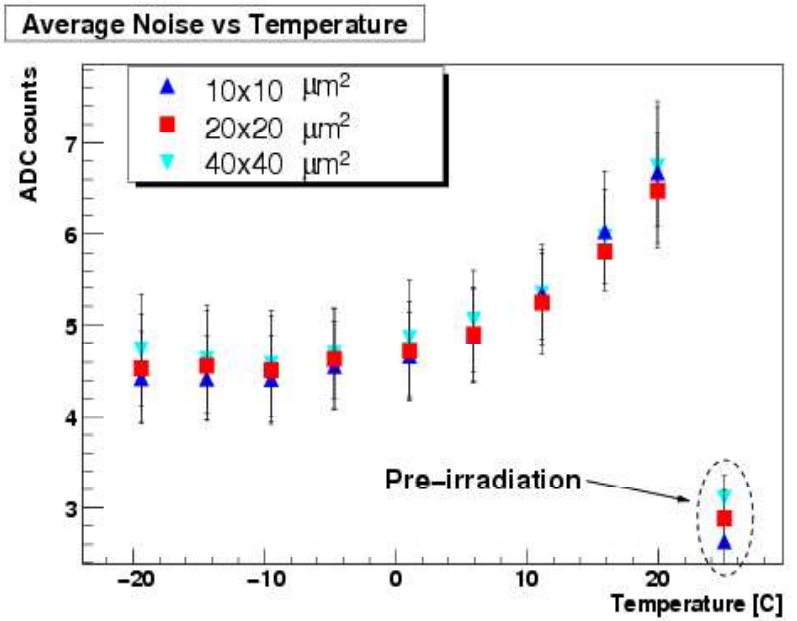


Test of irradiated prototype



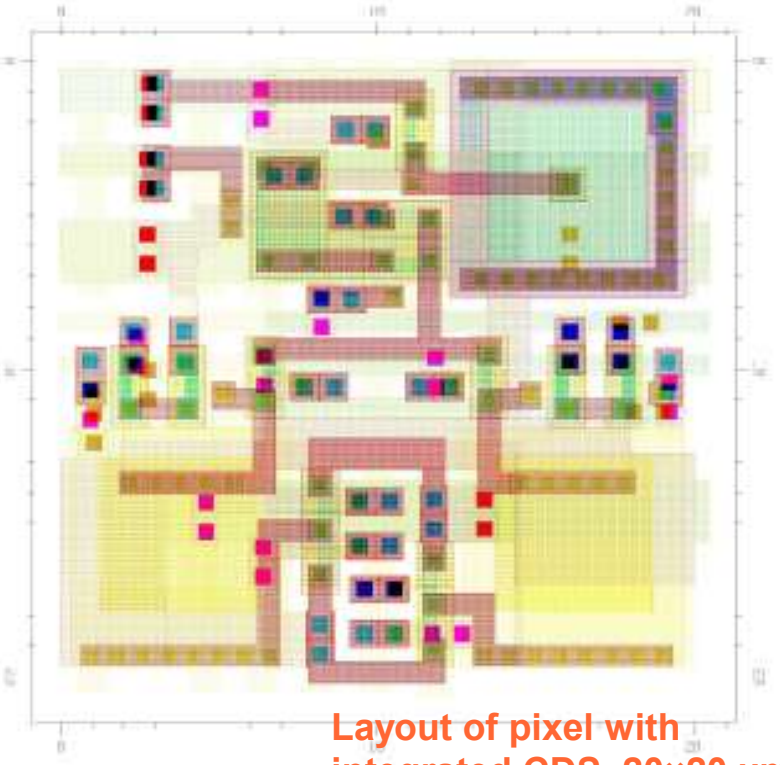


- Linear increase of leakage current with fluence
- Better performance of smaller pixels
- Increase in noise correlated with increase in leakage current, noise performance partially recovered by cooling
- Corresponding degradation of S/N performance for mips, decrease of cluster multiplicity



Outlook: next prototype submission

- LDRD-2: second prototype chip submission in Summer
- AMS 0.35 μm OPTO technology through CMP
- Larger size ~3×3 mm^2, different sectors, all with 20×20 μm^2 pitch
- Explore different architectures/parameters in different sectors:
  - In-pixel CDS
  - 3-T vs self-bias architecture
  - Size of charge collecting diodes (3×3 μm^2, 5×5 μm^2)
- High speed output line option



Layout of pixel with integrated CDS, 20×20 μm^2

- Includes circuitry for charge injection tests: plan to study capacitive coupling between pixels
- Started design of 5-bit ADC with low power consumption matching a 15 μm pixel pitch

→ larger scale prototype including CP readout and on-chip ADC foreseen in 2007

Outlook: future plans

- Completed first iteration of design/fabrication/characterization of prototype CMOS pixel sensor; two further chips under design to explore CDS and ADC functionalities

- Further tests:
  - Neutron irradiation at new line at 88-inch Cyclotron in Summer
  - Small tracker with reference 50 μm thin sensors for efficiency studies at ALS beam-test

- Next prototype to be available after Summer: readout development starting soon

- Extend back-thinning studies to 35 μm: test of all steps of the procedure needed (handling, mounting, bonding, etc...)

- Proposal for CMOS pixel telescope (small version of EUDET one) for beam-tests at FNAL