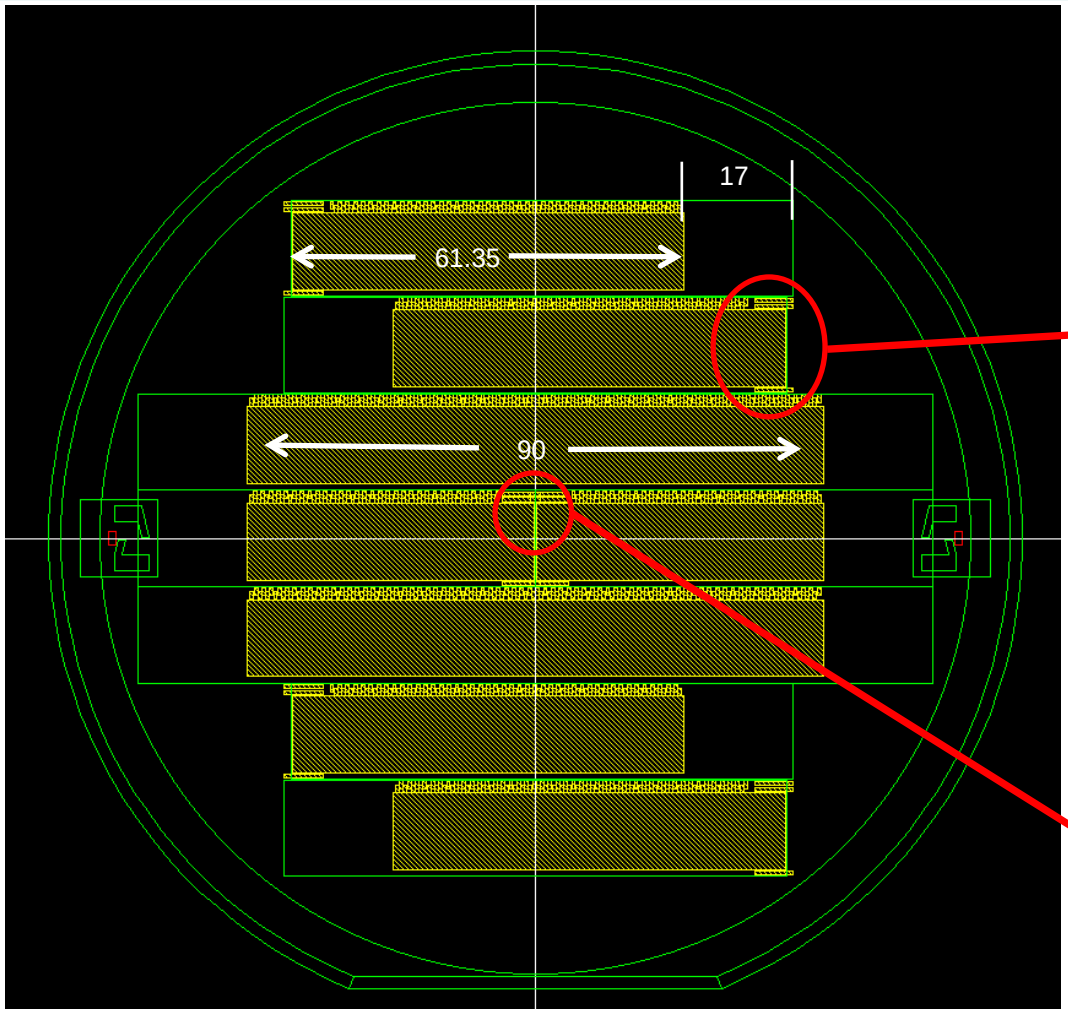
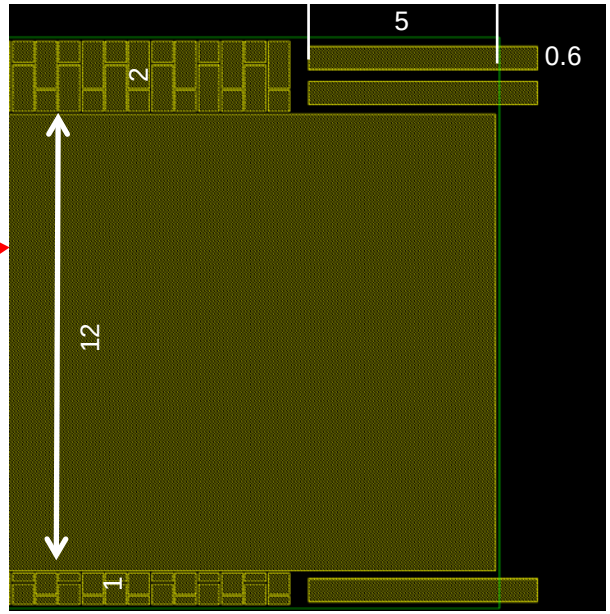
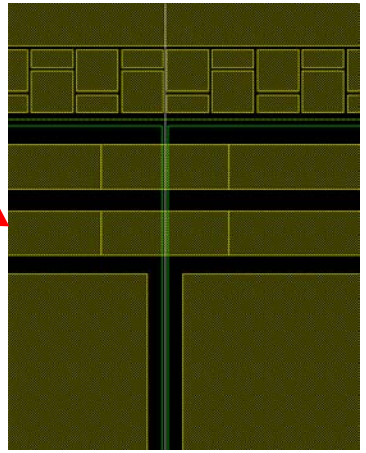
Layout for the mechanical dummies on SOI

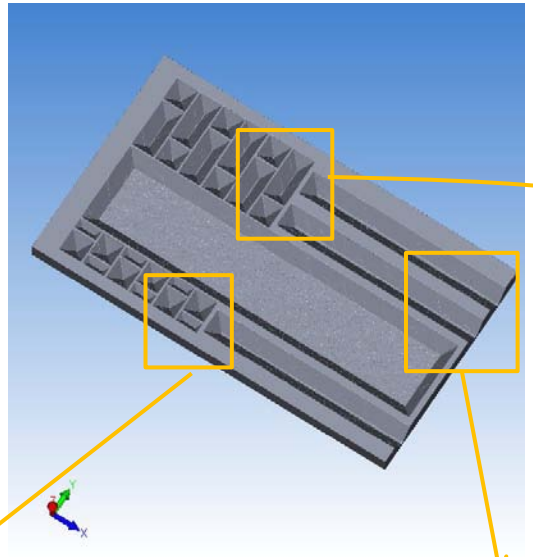






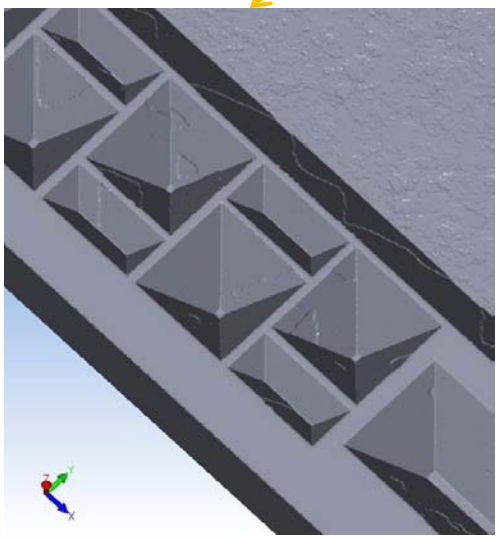
-: Status: Dimensions agreed, mask designed, wafer available
→ order mask

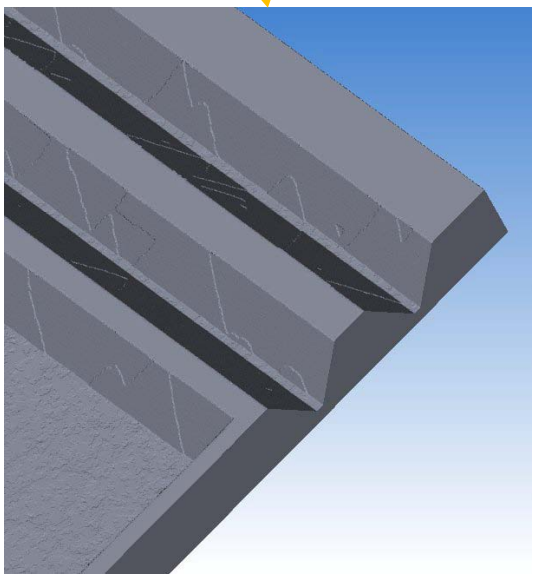
Frame perforation, low mass joint

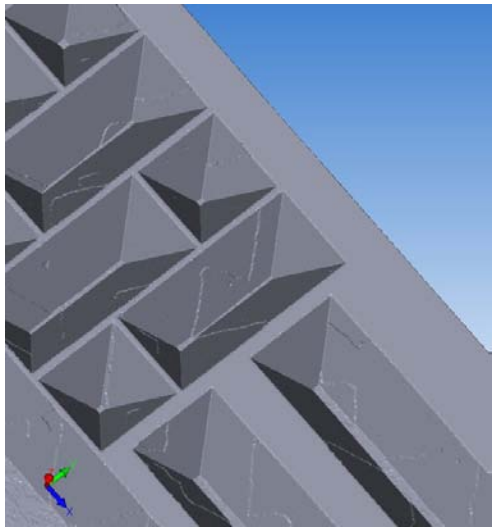


-: mask layout → etch simulator

-: material reduction on the order of 30%







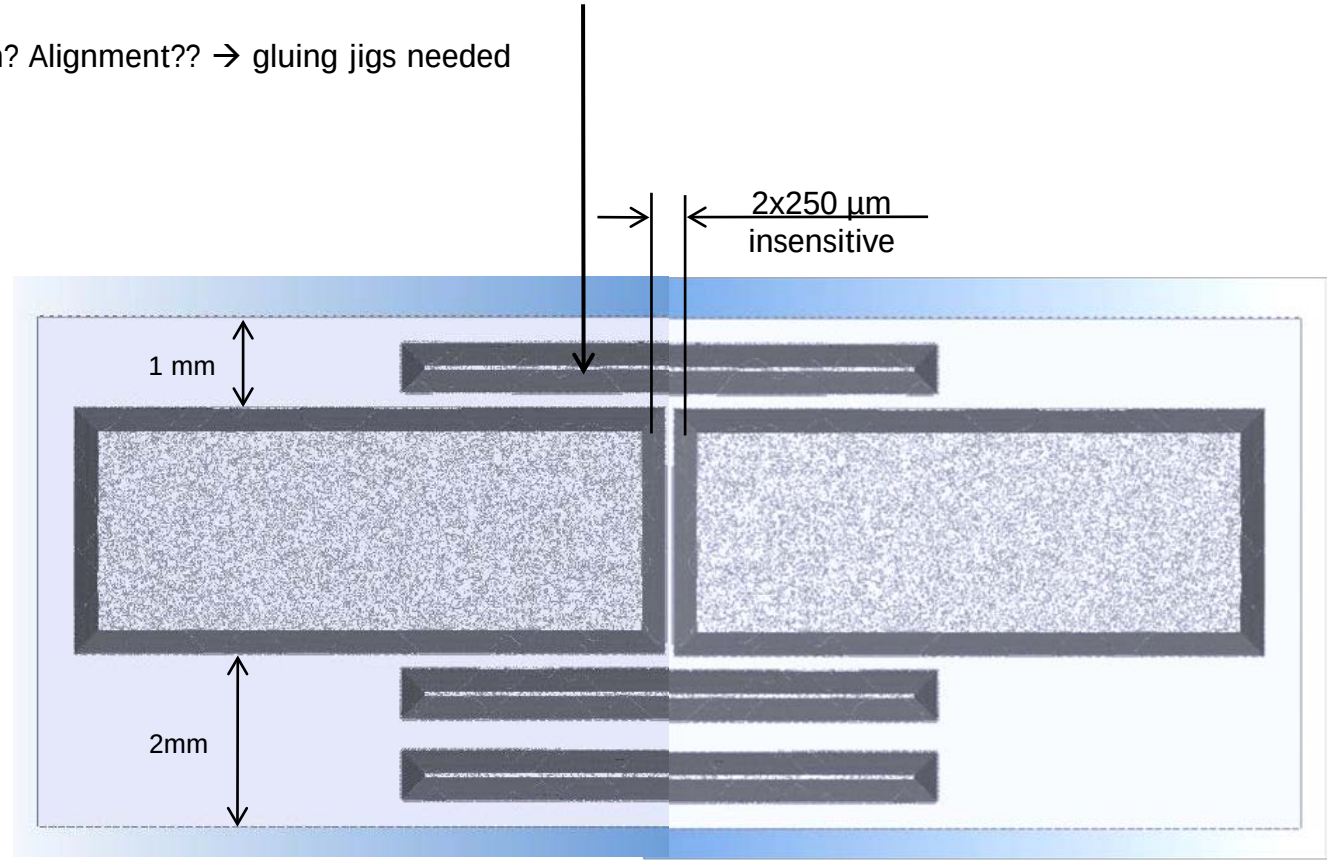
joint in layer 2 (and 1?)

-: Low-mass joint between two ladder halves

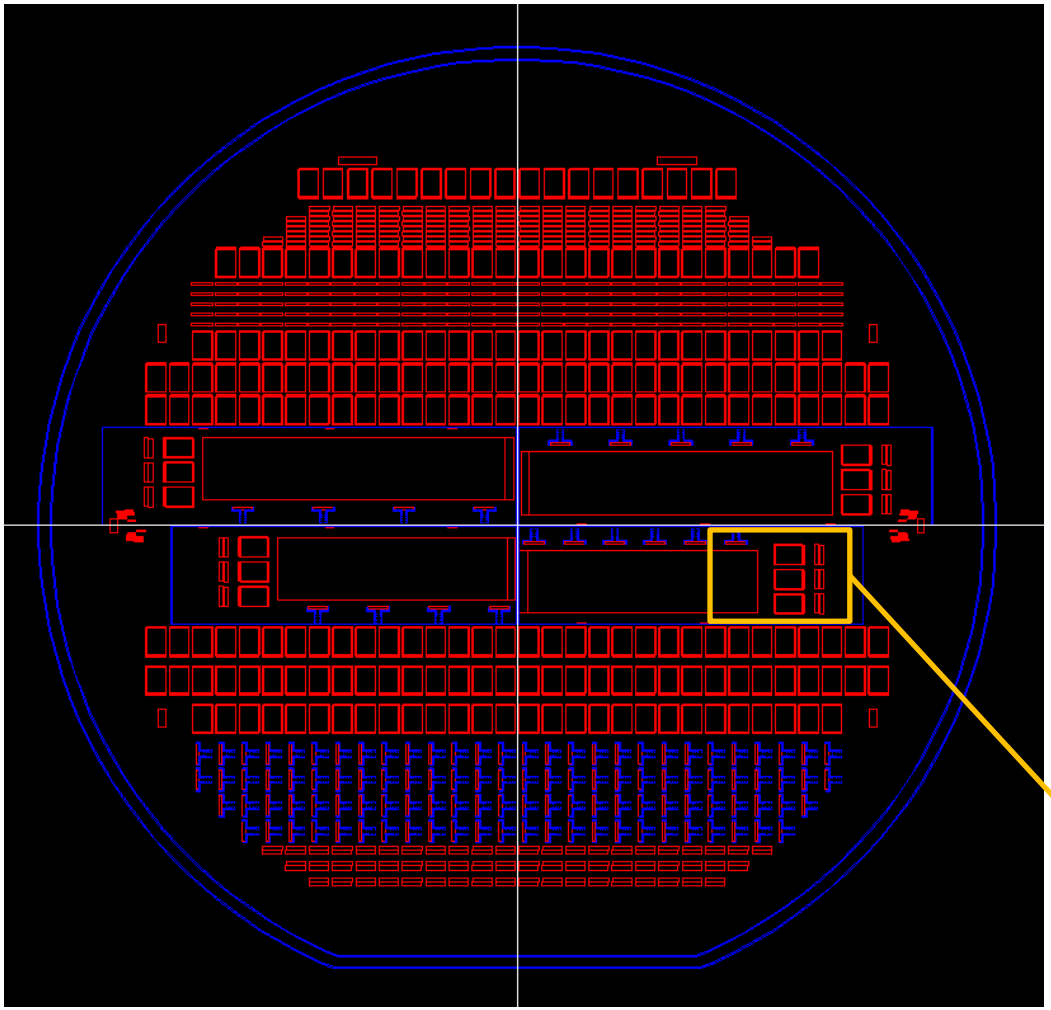
-: butt-joint (glueing, Araldite??)

-: insert 5-10 mm long pin, cylindrical, ceramic??, AlN??

-: precision? Alignment?? → gluing jigs needed



Bump Bond Dummies



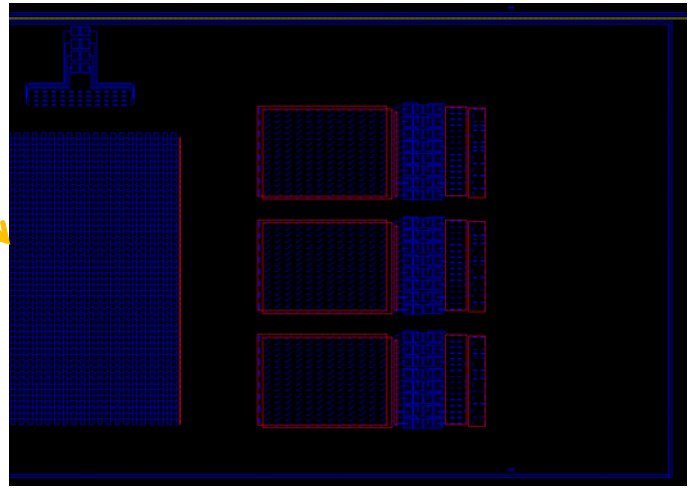
-: 450 micron thick Wafer
-: single Al layer on 230 nm oxide

-: Alu traces designed by Christian Kreidl
→ Chips (footprint) and landing pattern for
-: DCDs
-: Switchers
-: DCDROs

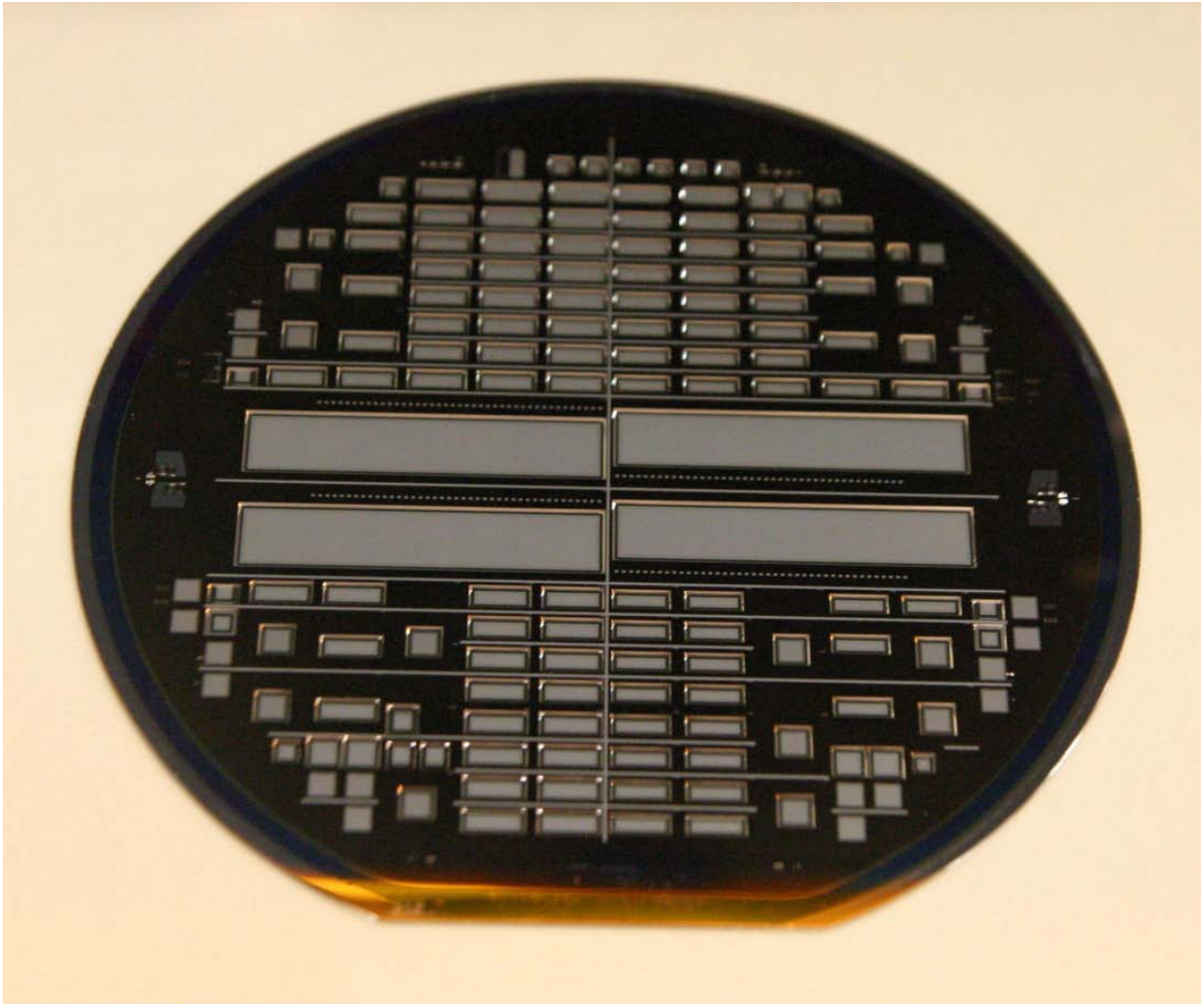
-: landing pattern for PXD6 large ladders

-: Al etching at HLL, Dicing at Disco

-: Status: define dicing streets,
→ order mask



PXD6 Back Side Dummy



-: etched back side of a PXD6 Wafer, showing the thinned sensitive areas, contacts, and metallization
-: second wafer (electrically active, diodes) with PXD6 metal on top in preparation

PXD6 Back Side Dummy